National Semiconductor

microCMOS

MM54HC4049/MM74HC4049 Hex Inverting Logic Level Down Converter
MM54HC4050/MM74HC4050 Hex Logic Level Down Converter

General Description

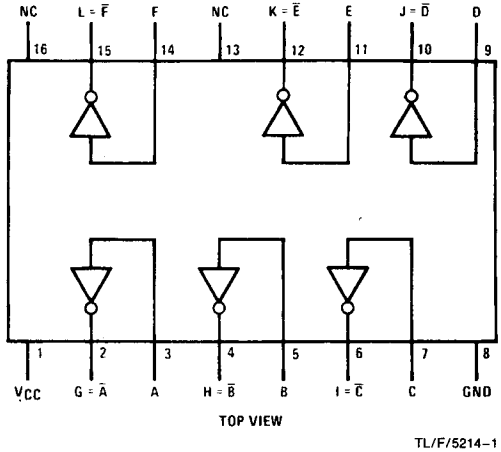
The MM54HC4049/MM74HC4049 and the MM54HC4050/MM74HC4050 utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC}, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. The MM54HC4049/MM74HC4049 is pin and functionally compatible to the CD4049BM/CD4049BC and the MM54HC4050/MM74HC4050 is compatible to the CD4050BM/CD4050BC

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA maximum (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagrams

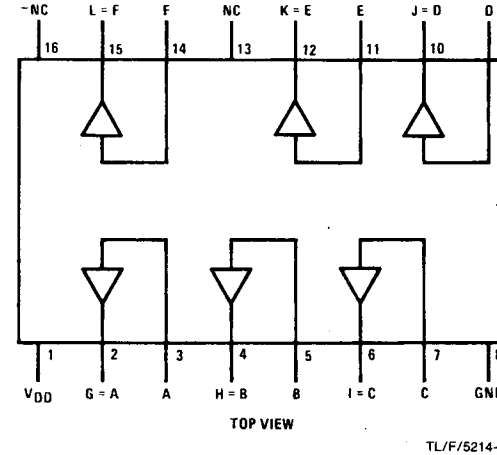
Dual-In-Line Package



TOP VIEW

TL/F/5214–1

Dual-In-Line Package



TOP VIEW

TL/F/5214–2

Order Number MM54HC4049J, MM54HC4050J, MM74HC4049J,N or MM74HC4050J,N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to +18V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{ZK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temp. Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input Voltage (V_{IN})	0	15	V
DC Output Voltage (V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to 85°C	54HC T_A = −55°C to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	60V		±0.1	±1.0	±1.0	μA
		V_{IN} = 15V	6.0V		±0.5	±5	±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40°$ to $85°C$		54HC $T_A=-55°$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	85	100	130	ns
			4.5V	10	17	20	26	ns
			6.0V	9	15	18	22	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.