

CMOS Digital decoding IC for Compact Disc

SAA7341

FEATURES

- Analog front end (data slicer, phase detector, VCO)
- Demodulator and EFM decoding
- Subcoding microprocessor handshaking protocol
- Integrated programmable motor speed control
- Single/four wire motor operation option
- Bidirectional data bus to external SRAM (8k x 8 bits)
- Error correction and concealment functions
- IEC/EBU digital output
- 192 x oversampling via 2-stage digital filter
- 2nd order noise shaping
- One-bit DAC with 1.4 V (RMS)
- Attenuation, mute and de-emphasis functions
- Power-on reset and standby functions

GENERAL DESCRIPTION

The SAA7341 incorporates the functions of decoding, digital filtering, and differential Digital-to-Analog conversion all on one CMOS IC. The device is specifically aimed at the mid-low end CD market, suitable for portable and car type applications.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|--------------------|-------------------------------------|-------|---------|-------|------|
| V _{DD} | supply voltage range | 4.5 | 5.0 | 5.5 | V |
| I _{DD} | supply current | - | 60 | - | mA |
| f _{X TAL} | crystal frequency range | 15.24 | 16.9344 | 18.63 | MHz |
| T _{amb} | operating ambient temperature range | -40 | - | +85 | °C |
| T _{stg} | storage temperature range | -55 | - | +150 | °C |

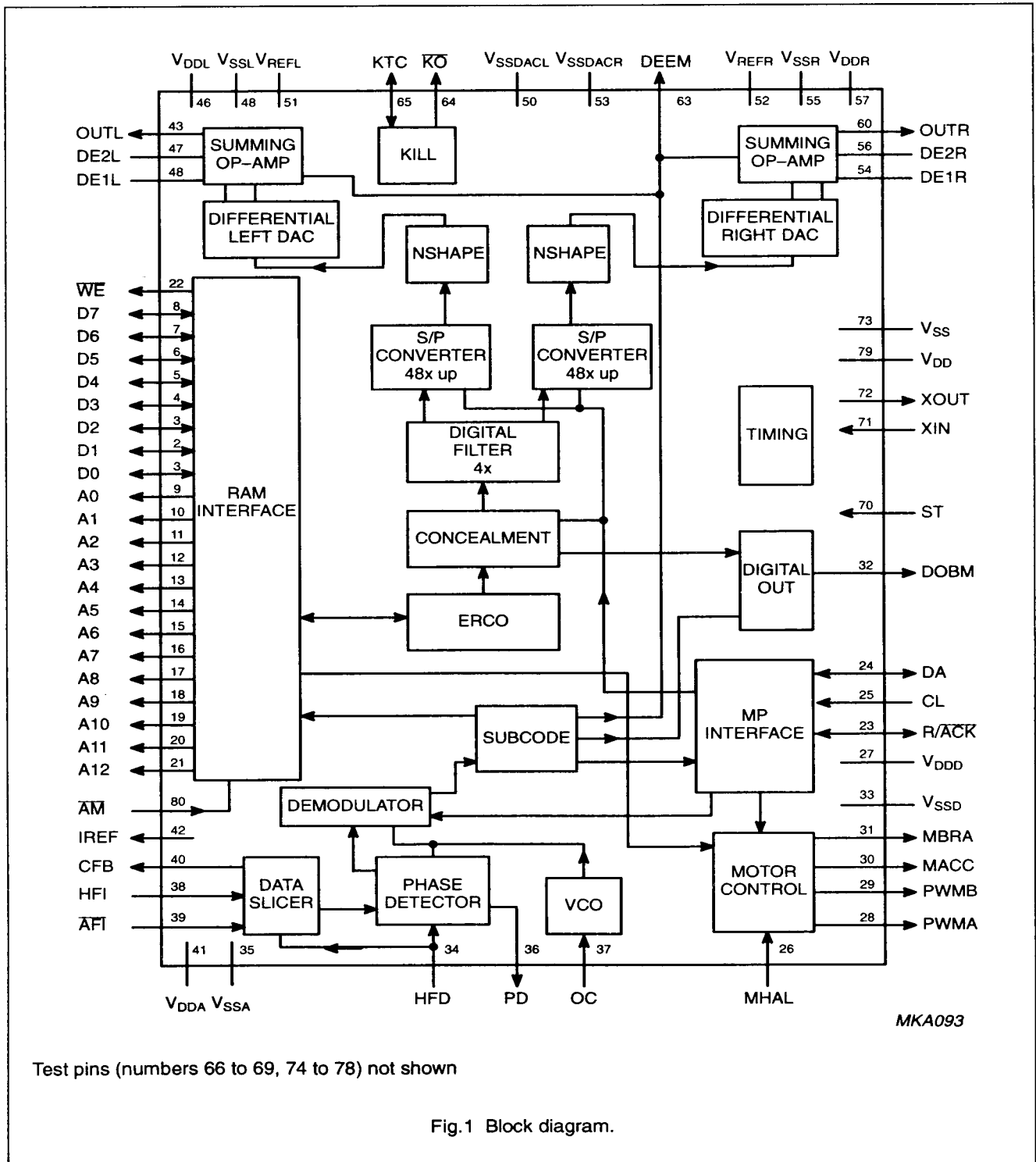
ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|----------------------|---------|--------------|----------|--------|
| | PINS | PIN POSITION | MATERIAL | CODE |
| SAA7341GP | 80 | QPF | plastic | SOT219 |

November 1991

CMOS Digital decoding IC for Compact Disc

SAA7341



MKA093

Test pins (numbers 66 to 69, 74 to 78) not shown

Fig.1 Block diagram.

CMOS Digital decoding IC for Compact Disc

SAA7341

PINNING

| SYMBOL | PIN | DESCRIPTION |
|--------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D0 to D7 | 1 to 8 | data inputs/outputs to external RAM |
| A0 to A12 | 9 to 21 | address outputs to external RAM |
| \overline{WE} | 22 | write enable: output signal to external RAM (active LOW) |
| $\overline{R/ACK}$ | 23 | request/acknowledge: input/output microprocessor interface; this pin has an open drain output with internal pull-up of 50 k Ω ; input is debounced by two 4.2336 MHz clock cycles |
| DA | 24 | microprocessor interface data input/output line; input is debounced by two 4.2336 MHz clock cycles |
| CL | 25 | microprocessor interface clock input debounced by two 4.2336 MHz clock cycles |
| MHAL | 26 | Hall effect detector for motor: input for motor reversal, with internal pull-up of 50 k Ω |
| V _{DDD} | 27 | +5 V supply for digital audio output (DOBM) and motor speed control (MSC) output buffers |
| PWMA | 28 | pulse width modulated motor control acceleration signal: output active during acceleration; single ended mode output |
| PWMB | 29 | pulse width modulated motor control brake signal: output active during braking |
| MACC | 30 | motor accelerate signal output |
| MBRA | 31 | motor brake signal output |
| DOBM | 32 | biphase-mark digital audio output: this output conforms to the format defined by IEC 958 |
| V _{SSD} | 33 | ground for digital audio output (DOBM) and motor speed control (MSC) outputs |
| HFD | 34 | high-frequency detector: when HIGH this input enables the fine frequency and phase detector outputs and also the feedback from the data slicer; this input has an internal pull-up of 50 k Ω |
| V _{SSA} | 35 | analog ground for front end |
| PD | 36 | phase detector: the phase detector output and fine/coarse frequency outputs are combined internally and the resultant signal controls the VCO frequency |
| OC | 37 | VCO control input |
| HFI | 38 | non-inverting data slicer input; normally AC-coupled to EFM data source |
| \overline{HFI} | 39 | inverting data slicer input; normally connected via external capacitor to ground of EFM data source |
| CFB | 40 | data slicer feedback output to capacitor: disabled when a data run length violation is detected or HFD is LOW to stop the slicing level from drifting |
| V _{DDA} | 41 | +5 V analog supply for front end |
| IREF | 42 | current reference output: reference current for internal current sources, nominally 114 μ A, requires external resistor connected to ground |

November 1991

3

CMOS Digital decoding IC for Compact Disc

SAA7341

| SYMBOL | PIN | DESCRIPTION |
|---------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OUTL | 43 | left channel output |
| n.c. | 44 | not connected |
| n.c. | 45 | not connected |
| V _{DDL} | 46 | +5 V analog supply for left channel integrator and operational amplifier |
| DE2L | 47 | pin 2 for external de-emphasis capacitor and resistor (left channel) |
| V _{SSL} | 48 | analog ground for left channel integrator and operational amplifier |
| DE1L | 49 | pin 1 for external de-emphasis capacitor and resistor (left channel) |
| V _{SSDACL} | 50 | analog ground for DAC (left channel) |
| V _{REFL} | 51 | internal reference voltage node for DAC left channel requiring an external decoupling capacitor |
| V _{REFR} | 52 | internal reference voltage node for DAC right channel requiring an external decoupling capacitor |
| V _{SSDACR} | 53 | analog ground for DAC (right channel) |
| DE1R | 54 | pin 1 for external de-emphasis capacitor and resistor (right channel) |
| V _{SSR} | 55 | analog ground for right channel integrator and operational amplifier |
| DE2R | 56 | pin 2 for external de-emphasis capacitor and resistor (right channel) |
| V _{DDR} | 57 | +5 V analog supply for the right channel integrator and operational amplifier |
| n.c. | 58 | not connected |
| n.c. | 59 | not connected |
| OUTR | 60 | right channel output |
| n.c. | 61 | not connected |
| n.c. | 62 | not connected |
| DEEM | 63 | output for external de-emphasis switches |
| \overline{KO} | 64 | output pulse (LOW) used to activate external kill circuit during power on/off |
| KTC | 65 | input/output connection to external capacitor used for the timing of the kill pulse at power on |
| TEST1 to 4 | 66 to 69 | these output pins should be left open-circuit |
| \overline{ST} | 70 | standby mode, input active LOW. Internal 50 k Ω pull-up resistor |
| XIN | 71 | input from crystal oscillator or external clock input (16.9344 MHz typ.) |
| XOUT | 72 | output to clock crystal |
| V _{SS} | 73 | ground for digital section |
| TEST5 | 74 | this output pin should be left open-circuit |
| TEST6 to 9 | 75 to 78 | these input pins should be tied HIGH |
| V _{DD} | 79 | +5 V supply for digital section |
| \overline{AM} | 80 | this input pin is normally held HIGH; should track loss occur this pin should be taken LOW and then the data is corrupted before the FIFO stage; this pin has an internal 50 k Ω pull-up resistor |

CMOS Digital decoding IC for Compact Disc

SAA7341

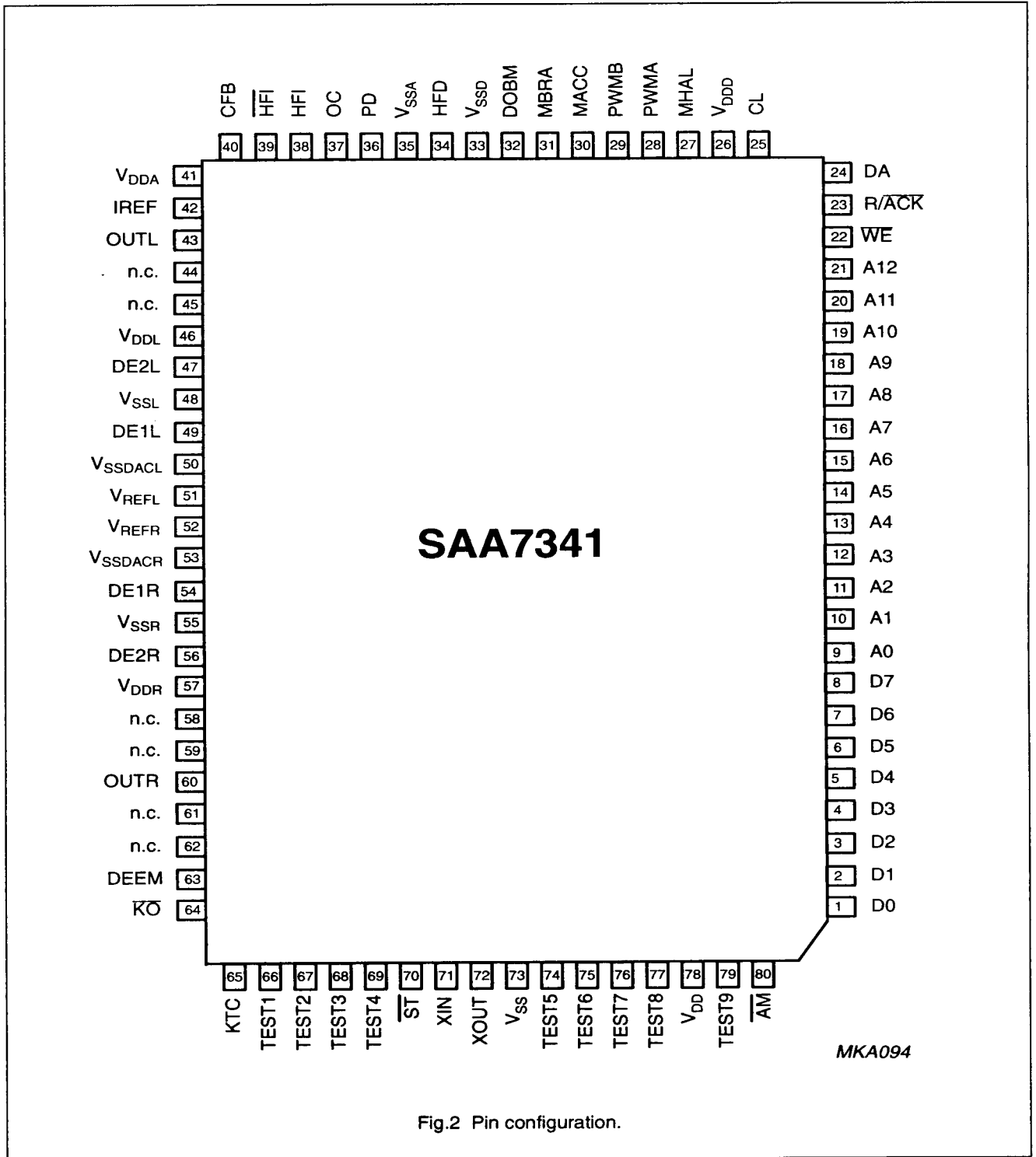


Fig.2 Pin configuration.

November 1991

5

CMOS Digital decoding IC for Compact Disc

SAA7341

FUNCTIONAL DESCRIPTION

Analog Front-End

The analog front-end contains the following functions: a data slicer, a VCO clock generator, fine and coarse frequency current switches and a current reference circuit.

The HFI input signal is converted to a digital signal by the data slicer. This is an adaptive level detector which relies on the DC-free nature of the modulation system to determine the optimum slicing level. When a signal drop-out is detected either externally via the HFD input or internally via the data run length violation detector, the feedback around the data slicer is disabled to stop the slicing level drifting.

Two (digital) frequency detectors and the phase detector provide coarse and fine control signals for the internal phase-locked-loop (PLL). The voltage controlled oscillator (VCO) is totally integrated, the frequency being dependent on the voltage at the OC pin. A coarse frequency detector compares the VCO frequency with the crystal clock and if necessary pulls the VCO to within the capture range of the fine frequency detector. This second detector uses data run length violations to pull the VCO further to within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled.

A separate current reference circuit is built in. An external resistor is needed at pin IREF (connected to V_{SS}).

Demodulator

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected master counter is only reset if a sync

pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the master counter. During track jumping it is necessary to allow the master counter to free run to minimise interference to the motor speed controller. An out-of-lock signal indicates that no sync coincidences are found within a certain period. This signal enables the fine frequency detector when the HFD input is HIGH. When HFD is LOW the working of the fine frequency detector is disabled.

The EFM (eight-to-fourteen modulation) decoder converts each symbol into one of 256 8-bit binary words which are passed across the clock interface to the subcode section. An additional output from the EFM decoder senses both extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe is also passed across the clock interface.

Subcoding

The subcode section runs on a clock divided from the crystal clock while the demodulator uses the VCO clock.

The demodulator output word and timing signals are latched on an enable signal derived from the demodulator data sync. The output of this latch either goes to the subcode processor (first byte of frame) or goes to the external RAM during a WRITE1 cycle. Due to the extended accessibility of the external RAM for the WRITE1 cycles compared to previous decoders a pre-FIFO is not needed. There are 72 time slots to write an EFM data frame of 32 bytes. The nominal period between two bytes delivered by the EFM decoder is

3.93 μ s. the longest period between two WRITE1 slots is 2.13 μ s.

The Q-channel processor of the subcoding section accumulates a subcoding word of 96 bits from the Q-bit of the subcoding symbol. It performs a cyclic redundancy check (CRC) using up 16 bits. If the CRC is good and the data is requested by the external processor the remaining 80 bits are put on the DA output on an external clock (CL).

The de-emphasis control signal is derived from 1 bit of the CRC checked Q-channel. This goes to DEEM output. A de-bounce is added for extra protection.

Subcode words (without the P-bit) are clocked to the digital output section together with a sync flag and a CRC result flag. They are fed into the user channel of the DOBM output signal. The control bits of a Q-frame are also copied to the first four bits of a channel status block. Conforms to Annex A of IEC 958.

Microprocessor Interface

The SAA7341 interfaces with a microprocessor by means of a 3-line bus consisting of a request/acknowledge line (R/ACK), a clock line (CL) and a data line (DA). The microprocessor can request Q-data from the SAA7341 or send control data for the motor speed control section.

Q-FRAME OUTPUT PROTOCOL

As long as the R/ACK line is held LOW by the microprocessor it can write control information to the SAA7341.

A Q-frame request is carried out when CL is HIGH by releasing the R/ACK line which should then go HIGH due to the pull-up resistor internal to the SAA7341. Figs 5 and 6 show the timing waveforms.

November 1991

6

**CMOS Digital decoding IC for
Compact Disc**

SAA7341

The SAA7341 is continually collecting Q-channel data and if it detects that $\overline{R/ACK}$ is HIGH it will hold the first frame of Q-data for which the CRC is good. It will then pull down $\overline{R/ACK}$ (acknowledge) and switch on the DA output. The microprocessor provides the clock to the CL input. After the first HIGH-to-LOW transition of CL, the SAA7341 will allow the $\overline{R/ACK}$ line to go HIGH. At the following HIGH-to-LOW transitions of CL the next Q-channel data bits will become available at the DA pin. As soon as the microprocessor has enough data (not necessarily 80 bits) it will pull $\overline{R/ACK}$ down again and the SAA7341 will disable DA and start collecting new Q-channel data.

If the microprocessor does not give a clock signal within 10.88 ms from the start of the acknowledge ($\overline{R/ACK}$

LOW) then the SAA7341 will reset the acknowledge signal and allow the $\overline{R/ACK}$ line to go HIGH again. After that the microprocessor still has 2.3 ms to accept the data. After a further 13.3 ms (typ.) the SAA7341 will have received a new Q-channel frame and if the CRC check is good a new acknowledge will be given.

**MICROPROCESSOR DATA WRITE
PROTOCOL**

The microprocessor can write data words into the 4-bit control registers of the SAA7341 when $\overline{R/ACK}$ is LOW. An 8-bit data burst on DA clocked with the positive edge of CL contains a 4-bit address (MSB first) and 4 bits of control data. It can be followed immediately by another burst of data without taking $\overline{R/ACK}$ HIGH.

Internally the receiver is reset when $\overline{R/ACK}$ is HIGH. The receiver will also be reset at stand-by and power-on. During the initialisation procedure the $\overline{R/ACK}$ line is held LOW by the SAA7341. When $\overline{R/ACK}$ becomes HIGH the SAA7341 is ready to receive data from the microprocessor.

A 2 bit debounce mechanism on CL and on the DA input protects the receiver against spikes.

INTERNAL CONTROL REGISTERS

A set of 8 control registers hold the different system parameters for all types of applications. One register is used to control the audio processing (e.g. mute, -12 dB attenuation). Other registers hold the parameters for the spindle motor control loop.

CMOS Digital decoding IC for Compact Disc

SAA7341

Table 1 Internal control registers; the initial values are loaded during power-on

| ADDRESS | | | | DATA | | | | INITIAL STATE | | | |
|---------|----|----|-----|-------|-------|-------|-------|---------------|---|---|---|
| msb | | | lsb | | | | | | | | |
| A3 | A2 | A1 | A0 | D3 | D2 | D1 | D0 | | | | |
| 0 | 0 | 0 | 0 | DIM | ANM | ATT | CRIB | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | TIM3 | TIM2 | TIM1 | TIM0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | OFS3 | OFS2 | OFS1 | OFS0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | OFS7 | OFS6 | OFS5 | OFS4 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | STOP | STRT | STPM | PWMM | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | LEV3 | LEV2 | LEV1 | LEV0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | VEL | POS | INT | INH | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | GAIN3 | GAIN2 | GAIN1 | GAIN0 | 0 | 0 | 0 | 0 |

Where:

| | | | | | |
|------|------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIM | Digital mute. When HIGH the DAC outputs and the sample data in the digital output (DOB M) will be muted. | OFS [3:0] | Low order nibble of accumulator offset. | POS | Position branch selection. When HIGH the output of the position branch is added with the output of other selected branches. |
| ANM | Analog mute. When HIGH only the DAC output is suppressed. The digital output (DOB M) is not affected. | OFS [7:4] | High order nibble of accumulator offset. | INT | Position integrator branch selection. When HIGH the output of the integrator is added with the output of other selected branches. |
| ATT | Attenuate (-12dB). When HIGH the DAC outputs and sample data in the digital output (DOB M) are attenuated. | STOP | STOP signal. | IHB | Integrator hold. Signal to switch off the input of the integrator. When IHB is LOW the position information is added to the contents of the accumulator once per frame. |
| CRIB | Counter reset inhibit. When CRIB is LOW the Demodulator master counter will free run. | STRT | START signal. | GAIN [3:0] | Loop gain selection. The loop gain can be selected according to the application. |
| | | STPM | STOP Mode selection. | | |
| | | PWMM | PWM mode selection. | | |
| | | LEV [3:0] | Start/stop level selection. The selected level is the modulus of a constant value injected into the motor control output processor during start or stop. The sign is controlled by STRT/STOP (negative for STRT). | | |
| | | VEL | Velocity branch selection. When HIGH the output of the velocity branch is added with the output of other selected branches. | | |

The following signals are used in the motor control section:

TIM [3:0] Start time selector. The selected start time is loaded in a timer which determines the duration of the start pulse.

CMOS Digital decoding IC for Compact Disc

SAA7341

Error Correction (ERCO)

The error corrector (ERCO) carries out $t = 1$, $e = 0$ error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. The strategy $t = 1$, $e = 0$ means that the ERCO can correct one erroneous symbol per frame and detect all erroneous frames. As $e = 0$, no erasure corrections (to flagged symbols) are carried out.

The error corrector also contains the Flag Processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags. There are no input flags for C1.

Concealment

The concealment section performs the following functions:

- Up to 6 sample interpolation in each channel to conceal erroneous data flagged by the error corrector. When more than 6 samples are corrupted the last good value will be held.
- Attenuation of -12 dB.
- Digital mute.

- Signal conditioning for filter section.

RAM Interface

The RAM interface section generates addresses for the external RAM in order to carry out the processing necessary to supply data in the correct manner to ERCO (for both C1 and C2 correction processes) and subsequently to the concealment section.

The data path involves entering and leaving the external RAM 3 times.

These operations are:

- FIFO and "small d" de-interleaving between SUBCODE and C1.
- "Large D" de-interleaving between C1 and C2.
- De-scrambling between C2 and CONCEALMENT.

In addition to the data operations, flags generated by the C1 and C2 correction processes are also processed by the RAM interface section. C1 output symbol flags receive the same de-interleaving processing as C1 output data, before being supplied to C2. C2 flags are also passed through the de-scrambling process but receive one frame less delay than the

corresponding C2 output data before being supplied to the concealment section. This enables the concealment section to initiate a jump action by the RAM interface to fetch the next good sample from the RAM when the flagged data needs to be interpolated.

EXTERNAL RAM TIMING

The external RAM is an 8k x 8 static CMOS RAM. An SAA7341 RAM address cycle takes nominally 236.2 ns. The write cycles are \overline{WE} controlled. The RAM interface timing waveforms are shown in Fig.4.

Digital Audio Output (DOB M)

The biphase-mark digital output signal is according to the format defined by IEC 958. The clock frequency for this section is 5.6448 MHz (one third the crystal frequency).

FORMAT

The digital audio output consists of 32 bit words ("subframes") transmitted in biphase-mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384.

Each word contains information as shown in Table 2.

Table 2 Word information

| PARAMETER | BIT | DESCRIPTION |
|----------------|---------|-----------------------------------------------------------------------------------|
| sync | 1 to 4 | - |
| auxiliary | 1 to 4 | not used; always zero |
| audio sample | 9 to 28 | first 4 bits not used (always zero); two's compliment; LSB = bit 13, MSB = bit 28 |
| validity flag | 29 | valid = logic 0 |
| user data | 30 | used for subcode data (Q-W) |
| channel status | 31 | control bits and category code |
| parity bit | 32 | even parity for bits 5 to 31 |

CMOS Digital decoding IC for Compact Disc

SAA7341

| | | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>SYNC</p> <p>The sync word is formed by violation of the biphas rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns indicate the following situations:</p> <p>Sync B Start of a block (384 words), word contains left sample.</p> <p>M Word contains left sample (no block start).</p> <p>W Word contains right sample.</p> | <p>AUDIO SAMPLE</p> <p>Left and right samples are transmitted alternately. Audio samples are available for DOBM in the concealment section after interpolation, attenuation and muting.</p> <p>VALIDITY FLAG</p> <p>Audio samples are flagged when they are not the original samples after error correction. The validity flag is logic 1 when the audio sample is the result of interpolation, muting or attenuation.</p> | <p>USER DATA</p> <p>Subcode bits Q until W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.</p> <p>CHANNEL STATUS</p> <p>The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is as shown in Table 3.</p> |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Table 3 Bit assignment

| PARAMETER | BIT | DESCRIPTION |
|---------------|-----------|-----------------------------------------------|
| control | 1 to 4 | copy of CRC checked Q-channel |
| reserved mode | 5 to 8 | always zero |
| category code | 9 to 16 | CD: bit 9 = logic 1, all other bits = logic 0 |
| remaining | 17 to 192 | always zero |

| | | |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>DIGITAL FILTER</p> <p>The digital filter is a 4 times oversampling recursive interpolation filter. It is constructed of 2 cascaded bireciprocal wave low-pass filters operating on a clock frequency of 4.2336 MHz. The sampling rates are 44.1 kHz and 88.2 kHz respectively.</p> <p>The filter receives 16 bit samples from the concealment section. The output of the filter is scaled in such a</p> | <p>way that a sinewave with maximum amplitude at the input can never cause overflow in the noise shaper.</p> <p>The serial outputs of the digital filter contain 20 bit data samples at a rate of 176.4 kHz. Left and right samples are converted to parallel and held for 48 cycles of 8.4672 MHz.</p> <p>The analog mute signal set via a microprocessor control register is synchronized to a sample. When it</p> | <p>is HIGH the input of the converter is zero.</p> <p>The second order digital noise shaper operates at a rate of 8.4672 MHz which is 192 times the sampling frequency. Overflow is prevented by a clipping mechanism. The 1-bit output of the noise shaper is connected to the DAC. There are two noise shapers, one for each channel.</p> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Table 4 Filter characteristics

| PARAMETER | VALUE (dB) | FREQUENCY (kHz) |
|------------------------|------------|-----------------|
| passband ripple | -0.1 to 0 | 0 to 20 |
| transition band | monotonic | 20 to 26 |
| | -3 | 22.05 |
| | -14 | 24 |
| stopband attenuation | <-30 | 26 to 88.2 |
| | <-35 | 40 to 65 |
| roll off due to sinx/x | 0.18 | - |

November 1991



CMOS Digital decoding IC for Compact Disc

SAA7341

D/A Conversion

The 1-bit output of the noise shaper is converted to an analog signal by a 1-bit differential switched-capacitor integrator.

The differential outputs are summed by an internal operational amplifier.

Kill, Power-on Reset and Standby Functions

A kill signal is available from the \overline{KO} output to activate an external kill circuit when required.

A power-on reset signal is derived from the external capacitor on KTC to initialize some of the internal control signals.

The SAA7341 can be put in standby mode to achieve silence at the outputs (except for XOUT) when the CD function in a combination player (music centre) is switched off. Also interference and power consumption will be minimized in the standby mode.

Spindle Motor Control Section

The motor control section uses the FIFO phase information from the RAM addressing section and disc speed information to calculate the motor control output signals. This calculation is performed at a rate of 7.35 kHz. The master clock of this section is 4.2336 MHz.

The motor control loop contains three branches : velocity, position and integrated position. These branches can be switched off independently by the microprocessor.

The outputs that drive the motor are MACC, MBRA, PWMA and PWMB. MACC and MBRA are active (HIGH) when the motor has to be accelerated or braked respectively. PWMA and PWMB are pulse width modulated signals with a frequency of 22.05 kHz of which the duty cycle controls the strength of the acceleration (PWMA) or braking effect (PWMB). In a second

selectable PWM-mode only one output (PWMA) is used.

By means of a 4-bit control register the following 5 modes of operation are possible :

- PASSIVE (motor control loop switched off)
- START (accelerate for a set time before PLAY takes over)
- PLAY (PLL motor on)
- BRAKE (braking unit told otherwise by microprocessor)
- STOP1 (braking until disc stopped then PASSIVE)

A block diagram of the motor control loop, including the microprocessor registers, is shown in Fig.8.



CMOS Digital decoding IC for Compact Disc

SAA7341

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|--------------|-------------------------------------|-------|----------------|------|
| V_{DD} | supply voltage; note 1 | -0.5 | +6.5 | V |
| V_I | maximum input voltage | -0.5 | $V_{DD} + 0.5$ | V |
| I_{REFabs} | input current, IREF only | - | +2 | mA |
| I_{IK} | DE input diode current | - | ± 20 | mA |
| V_O | output voltage | -0.5 | +6.5 | V |
| I_O | output current | | ± 10 | mA |
| T_{stg} | storage temperature range | -55 | +150 | °C |
| T_{amb} | operating ambient temperature range | -40 | +85 | °C |
| V_{es} | electrostatic handling; note 2 | -1000 | +1000 | V |

Notes to the limiting values

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 k Ω series resistor with a rise time of 15 ns.

CHARACTERISTICS

 $V_{DD} = 5\text{ V}$; $V_{SS} = 0$; $T_{amb} = 25^\circ\text{ C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------------------------------------------|---------------------------|----------------------------|------|------|----------------|---------------|
| Supplies | | | | | | |
| V_{DD} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| I_{DD} | supply current | $V_{DD} = 5\text{ V}$ | - | 60 | - | mA |
| $V_{SS}, V_{SSD},$ $V_{SSA}, V_{SSL},$ V_{SSR} | ground | note 1 | 0 | - | 0 | V |
| $V_{DD}, V_{DDD},$ $V_{DDA}, V_{DDL},$ V_{DDR}, V_{DDR} | positive supply voltage | note 1 | 4.5 | 5 | 5.5 | V |
| Digital inputs | | | | | | |
| $\overline{AM}, \overline{ST}, \overline{MHAL}, \overline{HFD}$ | | | | | | |
| V_{IL} | input voltage LOW | | -0.3 | - | 0.8 | V |
| V_{IH} | input voltage HIGH | | 2.0 | - | $V_{DD} + 0.3$ | V |
| V_{PU} | pull-up voltage | $I_I = 0\ \mu\text{A}$ | 2.0 | - | $V_{DD} + 0.3$ | V |
| C_I | input capacitance | | - | - | 10 | pF |
| R_I | internal pull-up resistor | | 15 | 50 | 100 | k Ω |
| CL | | | | | | |
| V_{IL} | input voltage LOW | | -0.3 | - | 0.8 | V |
| V_{IH} | input voltage HIGH | | 2.0 | - | $V_{DD} + 0.3$ | V |
| I_{LI} | input leakage current | $V_I = 0\text{ to }V_{DD}$ | -10 | - | +10 | μA |

CMOS Digital decoding IC for Compact Disc

SAA7341

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|---------------------------|-----------------------|------|------|-----------------|------------|
| C_i | input capacitance | | - | - | 10 | pF |
| XIN (EXTERNAL CLOCK) | | | | | | |
| V_{IL} | input voltage LOW | | -0.3 | - | 1.5 | V |
| V_{IH} | input voltage HIGH | | 3.5 | - | $V_{DD} + 0.3$ | V |
| I_{LI} | input leakage current | | -10 | - | +10 | μ A |
| C_i | input capacitance | | - | - | 10 | pF |
| Digital Input/Output | | | | | | |
| D0 TO D7 | | | | | | |
| V_{OL} | output voltage LOW | $I_{OL} = +0.4$ mA | 0 | - | 0.4 | V |
| V_{OH} | output voltage HIGH | $I_{OH} = -0.2$ mA | 3.0 | - | V_{DD} | V |
| C_L | load capacitance | | - | - | 50 | pF |
| V_{IL} | input voltage LOW | | -0.3 | - | 0.8 | V |
| V_{IH} | input voltage HIGH | | 2.0 | - | $V_{DD} + 0.3V$ | V |
| I_{LI} | 3-state leakage current | $V_i = 0$ to V_{DD} | -10 | - | +10 | μ A |
| C_i | input capacitance | | - | - | 10 | pF |
| DA | | | | | | |
| V_{OL} | output voltage LOW | $I_{OL} = +0.4$ mA | 0 | - | 0.4 | V |
| V_{OH} | output voltage HIGH | $I_{OH} = -0.2$ mA | 3.0 | - | V_{DD} | V |
| C_L | load capacitance | | - | - | 100 | pF |
| V_{IL} | input voltage LOW | | -0.3 | - | 0.8 | V |
| V_{IH} | input voltage HIGH | | 2.0 | - | $V_{DD} + 0.3V$ | V |
| I_{LI} | 3-state leakage current | $V_i = 0$ to V_{DD} | -10 | - | +10 | μ A |
| C_i | input capacitance | | - | - | 10 | pF |
| R/ACK | | | | | | |
| V_{OL} | output voltage LOW | $I_{OL} = +0.4$ mA | 0 | - | 0.4 | V |
| C_L | load capacitance | | - | - | 100 | pF |
| R_i | internal pull-up resistor | | 15 | 50 | 100 | k Ω |
| V_{IL} | input voltage LOW | | -0.3 | - | 0.8 | V |
| V_{IH} | input voltage HIGH | | 2.0 | - | $V_{DD} + 0.3$ | V |
| V_{PU} | pull-up voltage | $I_i = 0$ μ A | 2.0 | - | $V_{DD} + 0.3$ | V |
| C_i | input capacitance | | - | - | 10 | pF |
| Digital Outputs | | | | | | |
| A0 TO A12 | | | | | | |
| V_{OL} | output voltage LOW | $I_{OL} = +0.4$ mA | 0 | - | 0.4 | V |
| V_{OH} | output voltage HIGH | $I_{OH} = -0.2$ mA | 3.0 | - | V_{DD} | V |
| C_L | load capacitance | | - | - | 50 | pF |
| I_{LO} | 3-state leakage current | $V_o = 0$ to V_{DD} | -10 | 0 | 10 | μ A |

November 1991

13

CMOS Digital decoding IC for Compact Disc

SAA7341

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------------|-----------------------------------------------------------|-----------------------------------|----------------|---------|----------|------|
| WE, DEEM | | | | | | |
| V_{OL} | output voltage LOW | $I_{OL} = +0.4 \text{ mA}$ | 0 | - | 0.4 | V |
| V_{OH} | output voltage HIGH | $I_{OH} = -0.2 \text{ mA}$ | 3.0 | - | V_{DD} | V |
| C_L | load capacitance | | - | - | 50 | pF |
| DOBM (SEE FIG. 3 FOR LOAD) | | | | | | |
| $V_{O(p-p)}$ | voltage across a 75 Ω load (peak-to-peak value) | | 0.4 | - | 0.6 | V |
| MACC, MBRA | | | | | | |
| V_{OL} | output voltage LOW | $I_{OL} = +50 \mu\text{A}$ | 0 | - | 0.3 | V |
| I_{OH} | output current HIGH (constant source current) | $V_O = 0 \text{ to } 2 \text{ V}$ | - | -1.5 | - | mA |
| PWMA, PWMB | | | | | | |
| V_{OH} | output voltage HIGH | $I_{OH} = -50 \mu\text{A}$ | $V_{DD} - 0.3$ | - | V_{DD} | V |
| I_{OL} | output current LOW (constant sink current) | $V_O = 3 \text{ to } V_{DD}$ | - | 1.5 | - | mA |
| Crystal Oscillator | | | | | | |
| XIN, XOUT | | | | | | |
| f_{XTAL} | crystal frequency | | 15.24 | 16.9344 | 18.63 | MHz |
| g_m | mutual conductance at 100 kHz | | 1.5 | - | - | mS |
| A_V | small signal voltage gain | $A_V = g_m \cdot R_O$ | 3.5 | - | - | V/V |
| C_I | input capacitance | | - | - | 10 | pF |
| C_{FB} | feedback capacitance | | - | - | 5 | pF |
| C_O | output capacitance | | - | - | 10 | pF |
| Reference Voltage outputs | | | | | | |
| VREFL, VREFR | | | | | | |
| V_R | voltage reference | | - | 2.5 | - | V |
| OUTPUT PERFORMANCE | | | | | | |
| $V_{AO(RMS)}$ | output level (RMS value) | note 2 | - | 1.4 | - | V |
| S/N | signal-to-noise ratio | 0 dB input | 90 | - | - | dB |
| THD | total harmonic distortion (plus noise) | 0 dB/1 kHz | - | - | -70 | dB |
| | | -10 dB/1 kHz | - | -80 | - | dB |
| | channel matching | 0 dB/1 kHz | -0.25 | 0 | +0.25 | dB |
| | crosstalk | | - | -90 | - | dB |
| PSRR | power supply rejection ratio | | - | 40 | - | dB |

CMOS Digital decoding IC for Compact Disc

SAA7341

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------------------------------|----------------------------------------------------------------------------|----------------------------------|----------------|--------|----------|------------|
| Kill Circuit | | | | | | |
| INPUT/OUTPUT: KTC | | | | | | |
| | KTC switching level | KTC rising | - | 3.0 | - | V |
| | | KTC falling | - | 2.0 | - | V |
| V_{OL} | output voltage LOW | $I_{OL} = 0$ | 0 | - | 0.4 | V |
| R_I | internal discharge resistor | KTC = LOW | - | 2 | - | k Ω |
| I_{OH} | output current HIGH | | - | 10 | - | μ A |
| OUTPUT: $\overline{K\bar{O}}$ | | | | | | |
| R_I | internal pull-down resistor | | - | 50 | - | k Ω |
| V_{OH} | output voltage HIGH | $I_{OH} = 0$ | $V_{DD} - 0.2$ | - | - | V |
| V_{TK} | supply threshold for power on | | - | 1 | - | V |
| V_{TPD} | supply threshold for power down | | - | 4.6 | - | V |
| V_{HPD} | hysteresis of V_{TPD} | | 0 | - | 200 | mV |
| Timing (note 3) | | | | | | |
| RAM INTERFACE (SEE FIG. 4) | | | | | | |
| t_{acc} | read access time (for external RAM) | | - | - | 150 | ns |
| t_{wp} | write enable pulse | | 100 | - | - | ns |
| t_{as} | address set-up time | | 0 | - | - | ns |
| t_{wz} | delay from falling edge of \overline{WE} to data bus going low impedance | XIN = 16.9 MHz XIN = 18.6 MHz | 35 30 | - - | - - | ns ns |
| t_{wr} | write recovery time from rising edge of \overline{WE} | | 20 | - | - | ns |
| t_{dw} | data valid before end of write | | 50 | - | - | ns |
| t_{dh} | data hold time from rising edge of \overline{WE} | | 5 | - | - | ns |
| MICROPROCESSOR INTERFACE (SEE FIGS 5, 6 AND 7) | | | | | | |
| t_{an} | access time normal mode | note 4 | 0 | - | n x 13.3 | ms |
| t_{ar} | access time refresh mode | note 4 | 13.3 | - | n x 13.3 | ms |
| t_{da} | CL to RA acknowledge delay | | - | 0.9 | 2.0 | μ s |
| t_{th} | CL to RA request hold time | | 2.0 | - | - | μ s |
| t_{cl} | CL input LOW time | | 2.0 | - | - | μ s |
| t_{ch} | CL input HIGH time | | 2.0 | - | - | μ s |
| t_{dd} | CL to DA delay time | | - | 0.9 | 2.0 | μ s |
| t_{ak} | acknowledge time | note 5 | - | - | 10.88 | ms |
| t_{ah} | data hold time after acknowledge | note 6 | 2.31 | - | - | ms |
| t_{ds} | microprocessor data set-up time to positive edge of CL | | 1.0 | - | - | μ s |

CMOS Digital decoding IC for Compact Disc

SAA7341

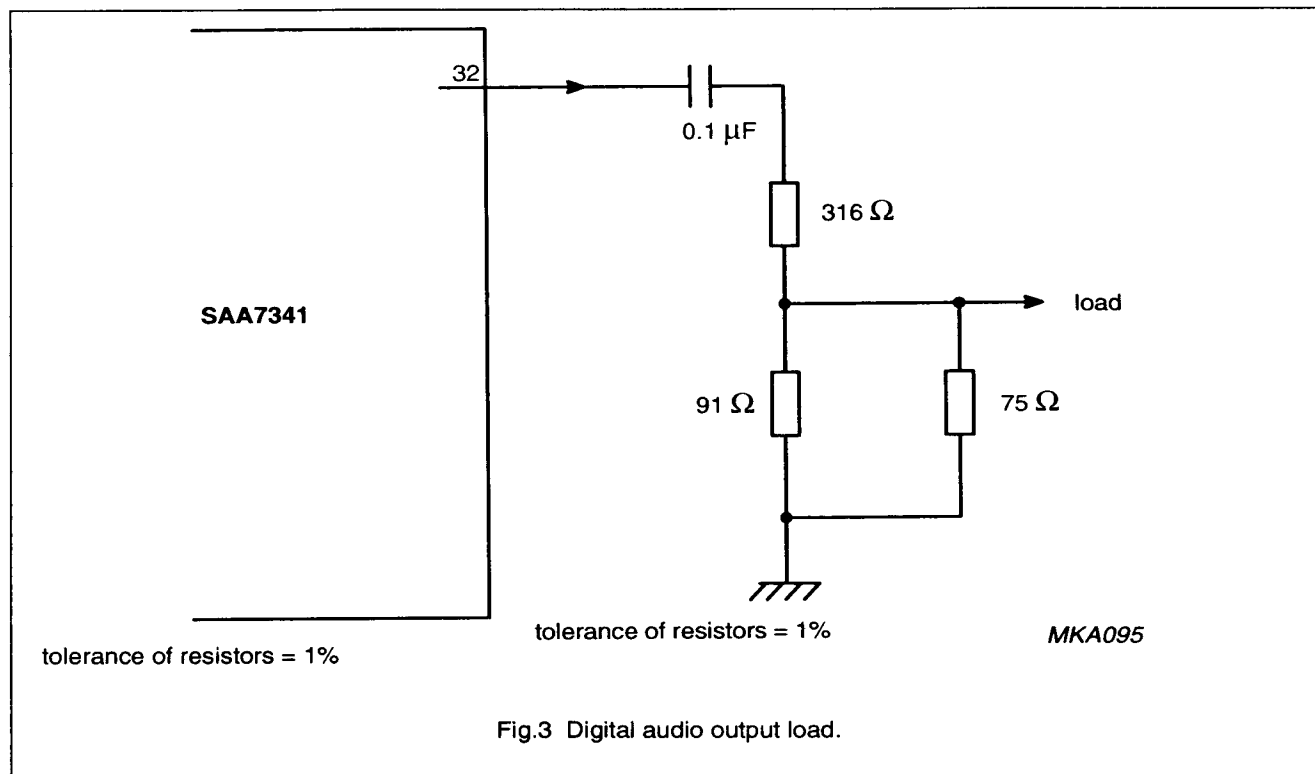
CHARACTERISTICS

$V_{DD} = 5\text{ V}$; $V_{SS} = 0$; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|---------------------------------------------------------|------------|------|------|------|---------------|
| t_{dh} | microprocessor data hold time after positive edge of CL | | 2.0 | - | - | μs |
| t_{drw} | delay to write after read | | 2.0 | - | - | μs |
| t_{dwr} | delay to read after write | | 2.0 | - | - | μs |

Notes to the characteristics

1. All V_{SS} s and all V_{DD} s must be connected back to the ground and positive terminals of a single supply, respectively.
2. Maximum load recommended on OUTL, OUTR, is 5 k Ω , 100 pF. Device measured with external components shown in recommended application diagram (Fig.9). Maximum digital code.
3. Timing reference voltage levels are 0.8 V and 2.0 V.
4. Q-channel access times are dependent on the parity check on the Q channel data frame; n = the number of cycles until data is valid.
5. The acknowledge time is the time for which the SAA7341 will hold $\overline{\text{R/ACK}}$ LOW without the microprocessor driving CL LOW. The time is related to the frequency of the incoming data, and is therefore dependent on the frequency of the demodulation section. The value given is for demodulator operating at a nominal frequency of 4.32 MHz.
6. This is the amount of time for which the microprocessor can still successfully access the Q channel data after the SAA7341 has released $\overline{\text{R/ACK}}$ without CL going LOW. Again the time given is for demodulator operating at a nominal frequency of 4.32 MHz.



CMOS Digital decoding IC for Compact Disc

SAA7341

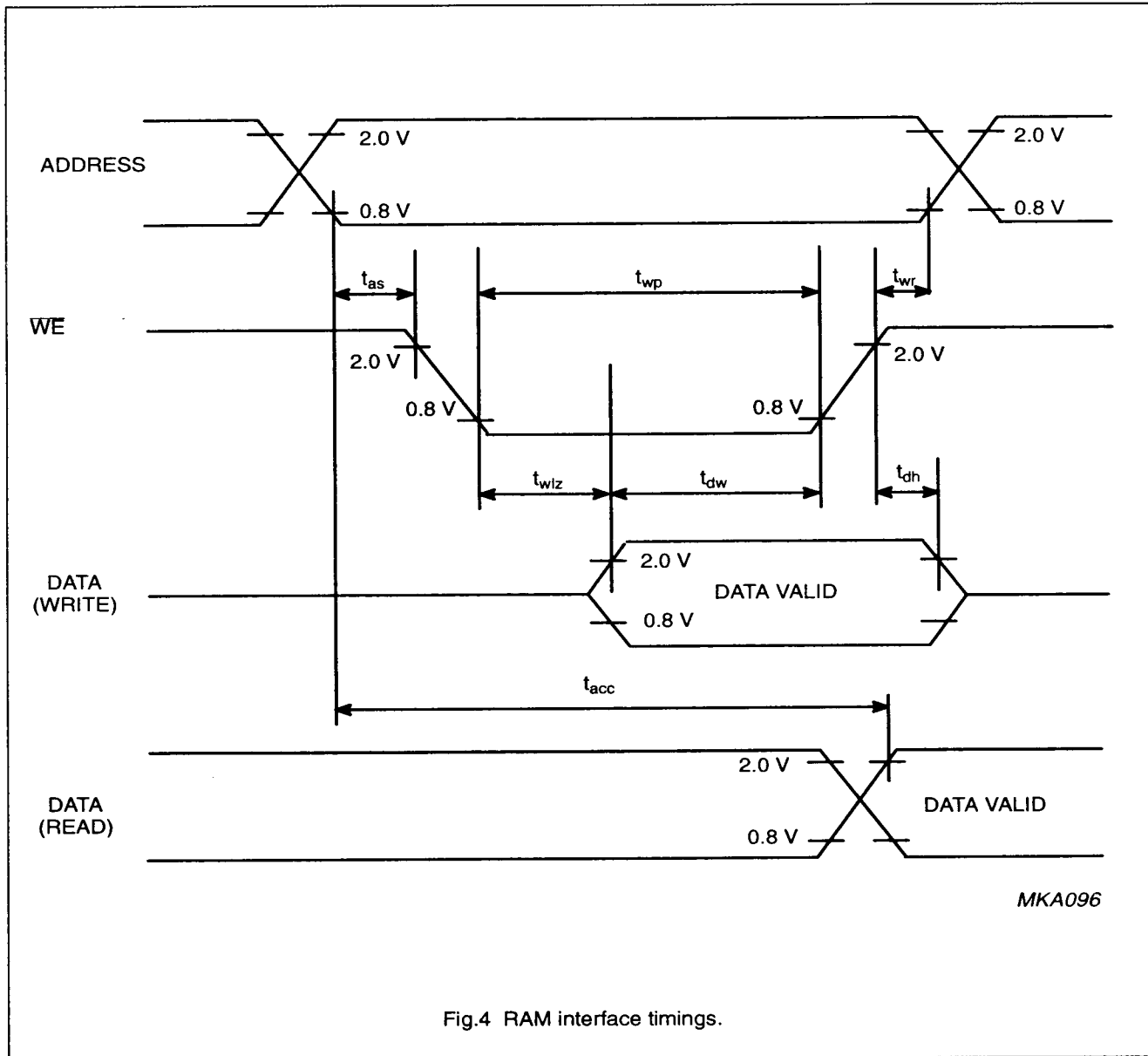


Fig.4 RAM interface timings.

CMOS Digital decoding IC for Compact Disc

SAA7341

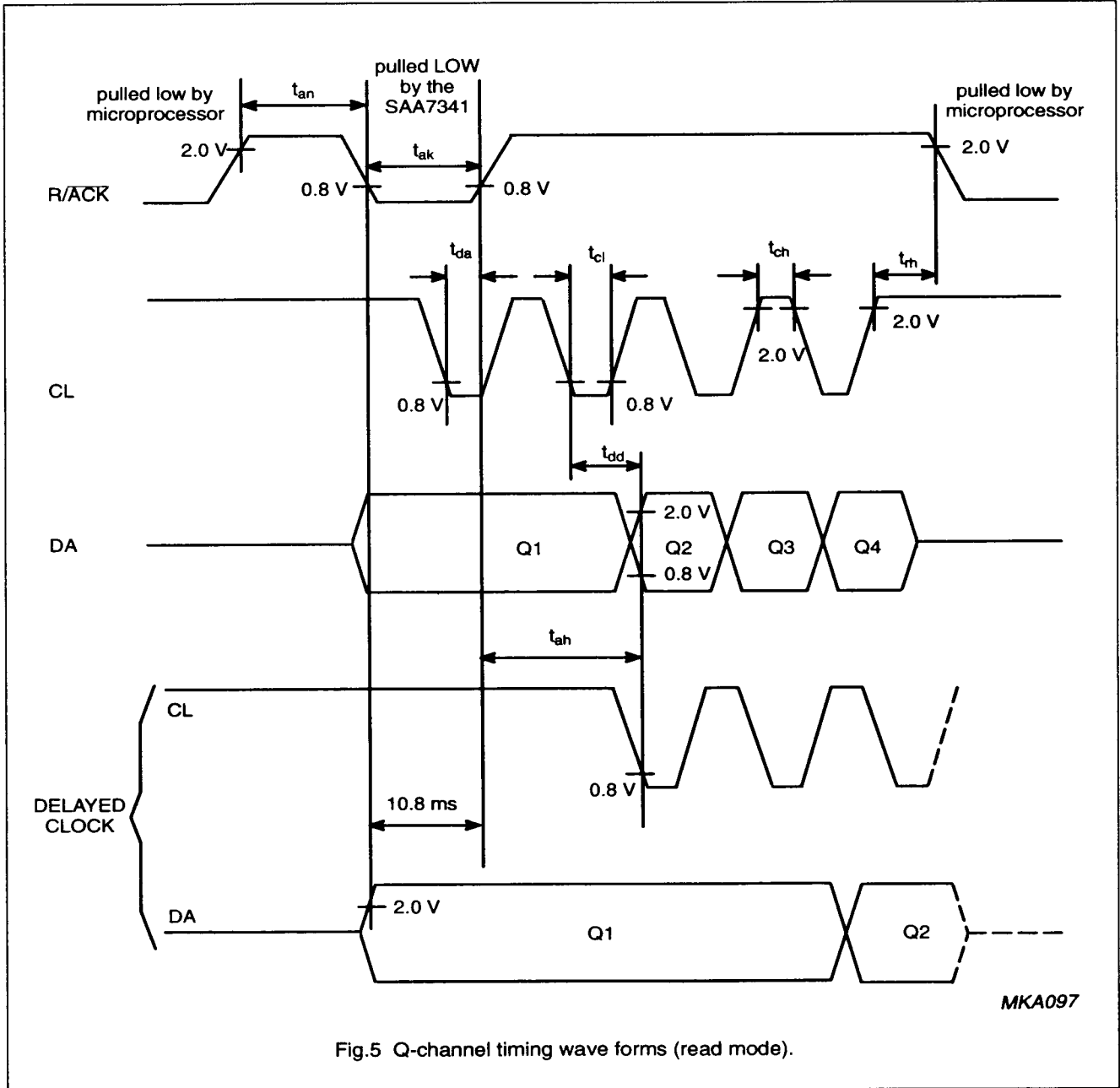


Fig.5 Q-channel timing wave forms (read mode).

CMOS Digital decoding IC for Compact Disc

SAA7341

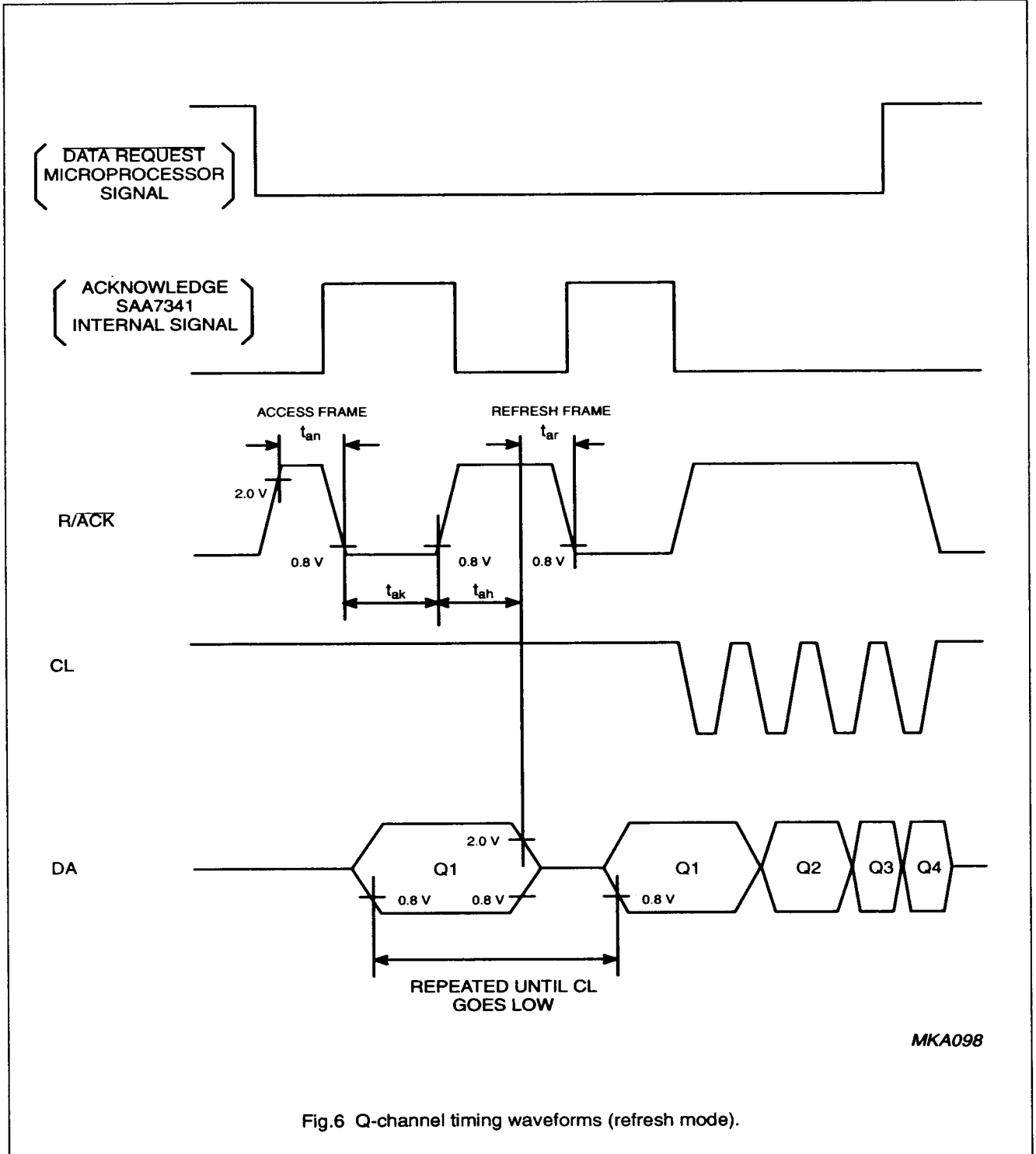


Fig.6 Q-channel timing waveforms (refresh mode).

CMOS Digital decoding IC for Compact Disc

SAA7341

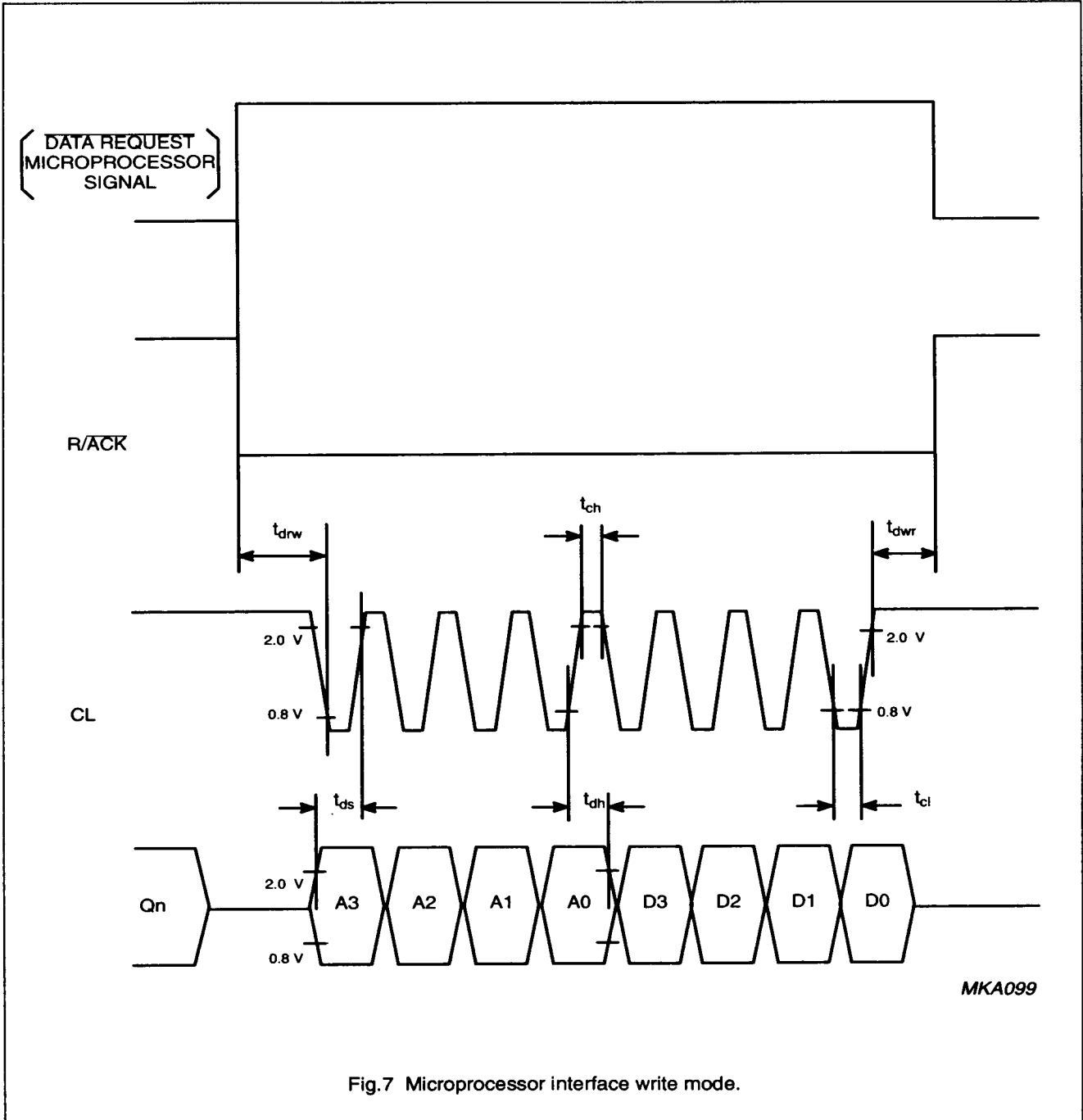


Fig.7 Microprocessor interface write mode.

CMOS Digital decoding IC for Compact Disc

SAA7341

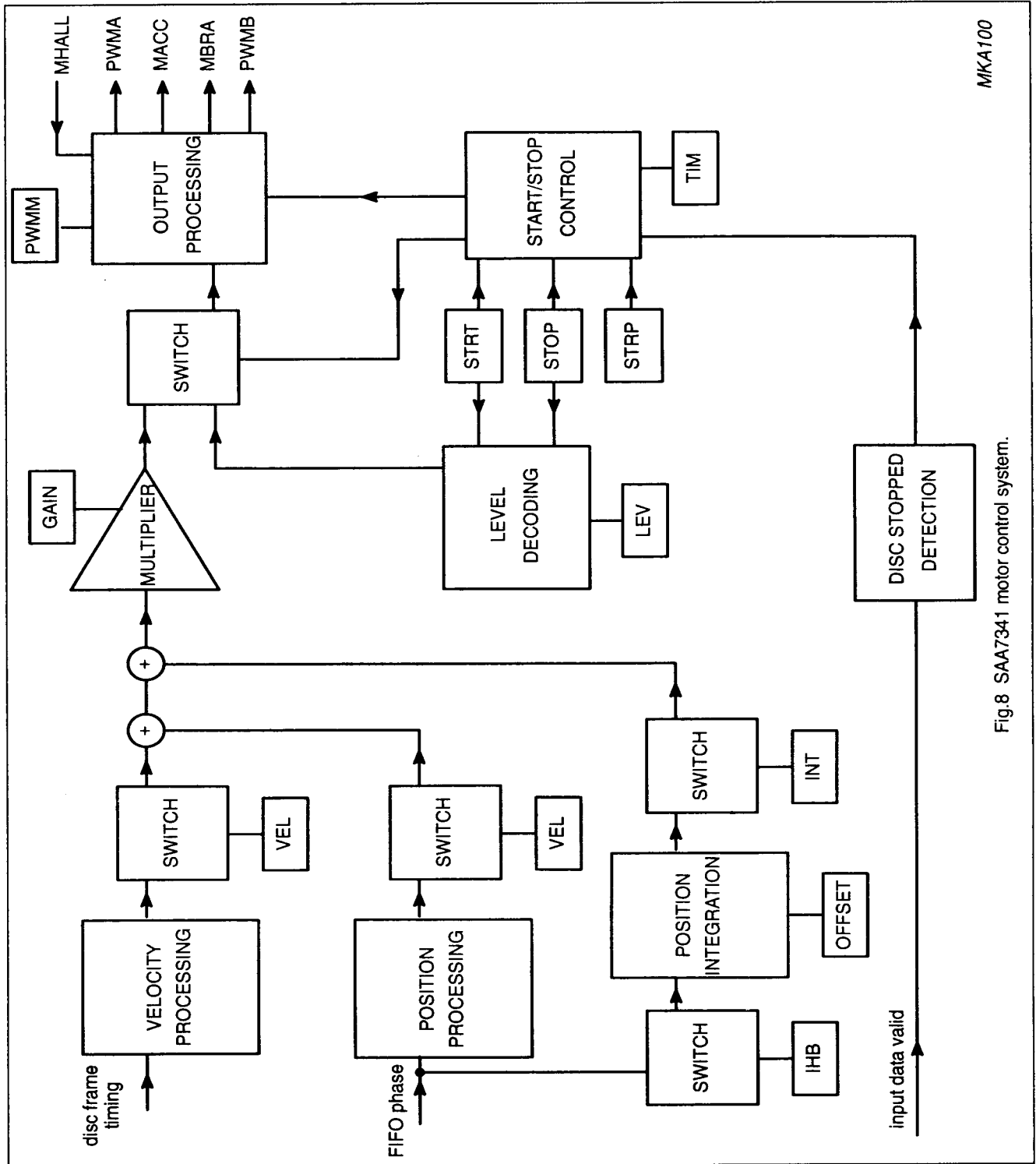


Fig.8 SAA7341 motor control system.

November 1991

21

CMOS Digital decoding IC for Compact Disc

SAA7341

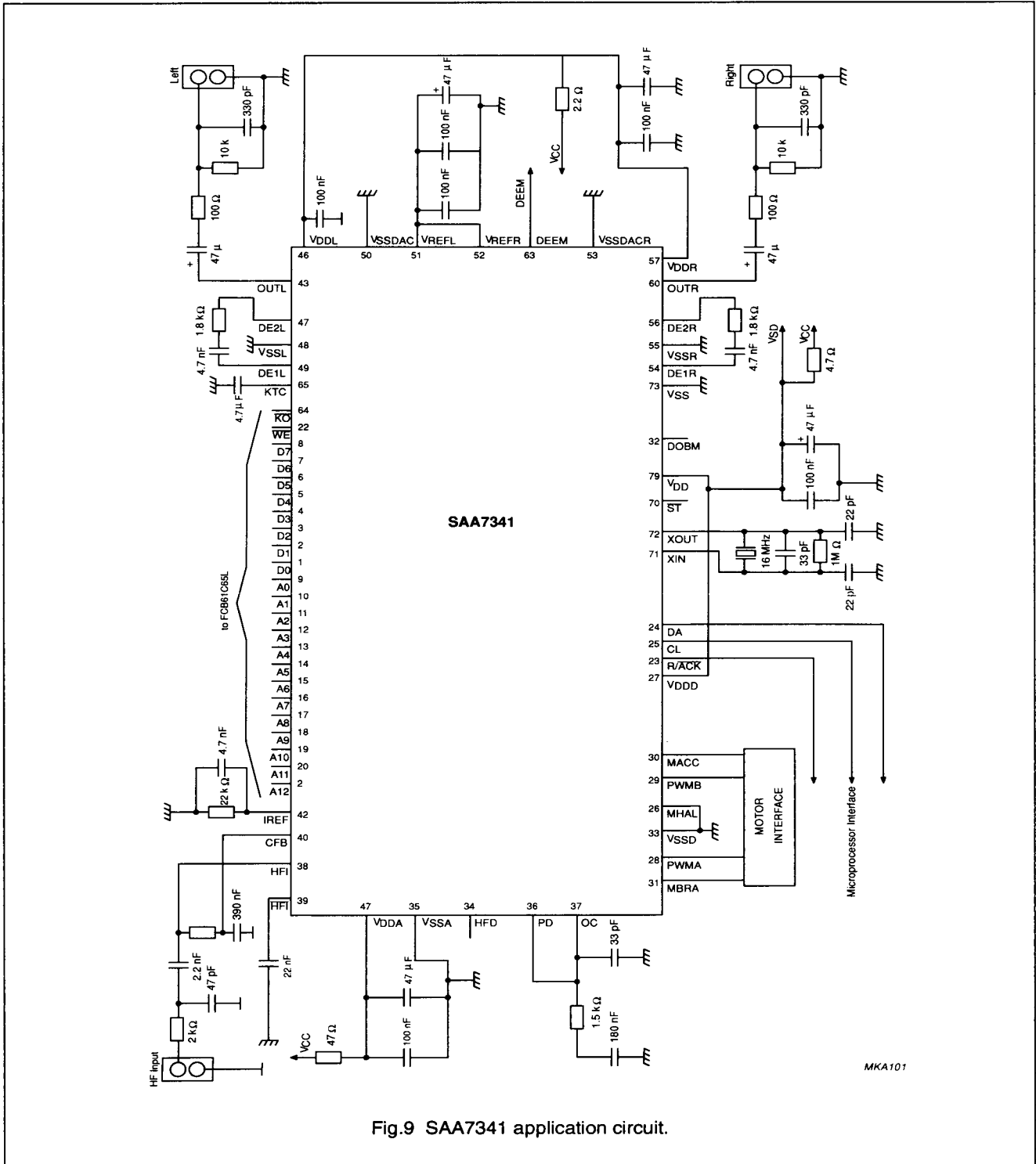


Fig.9 SAA7341 application circuit.

CMOS Digital decoding IC for
Compact Disc

SAA7341

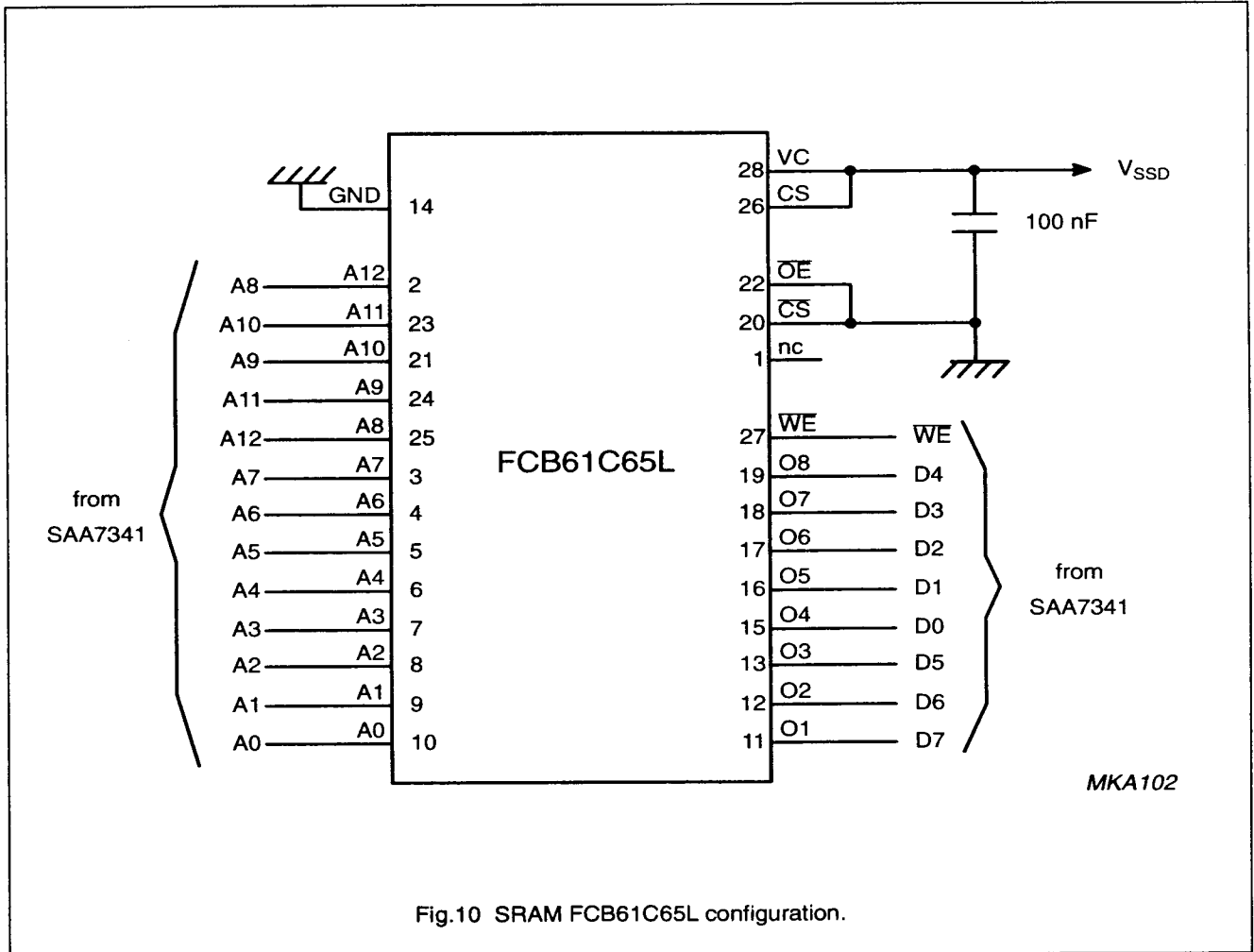
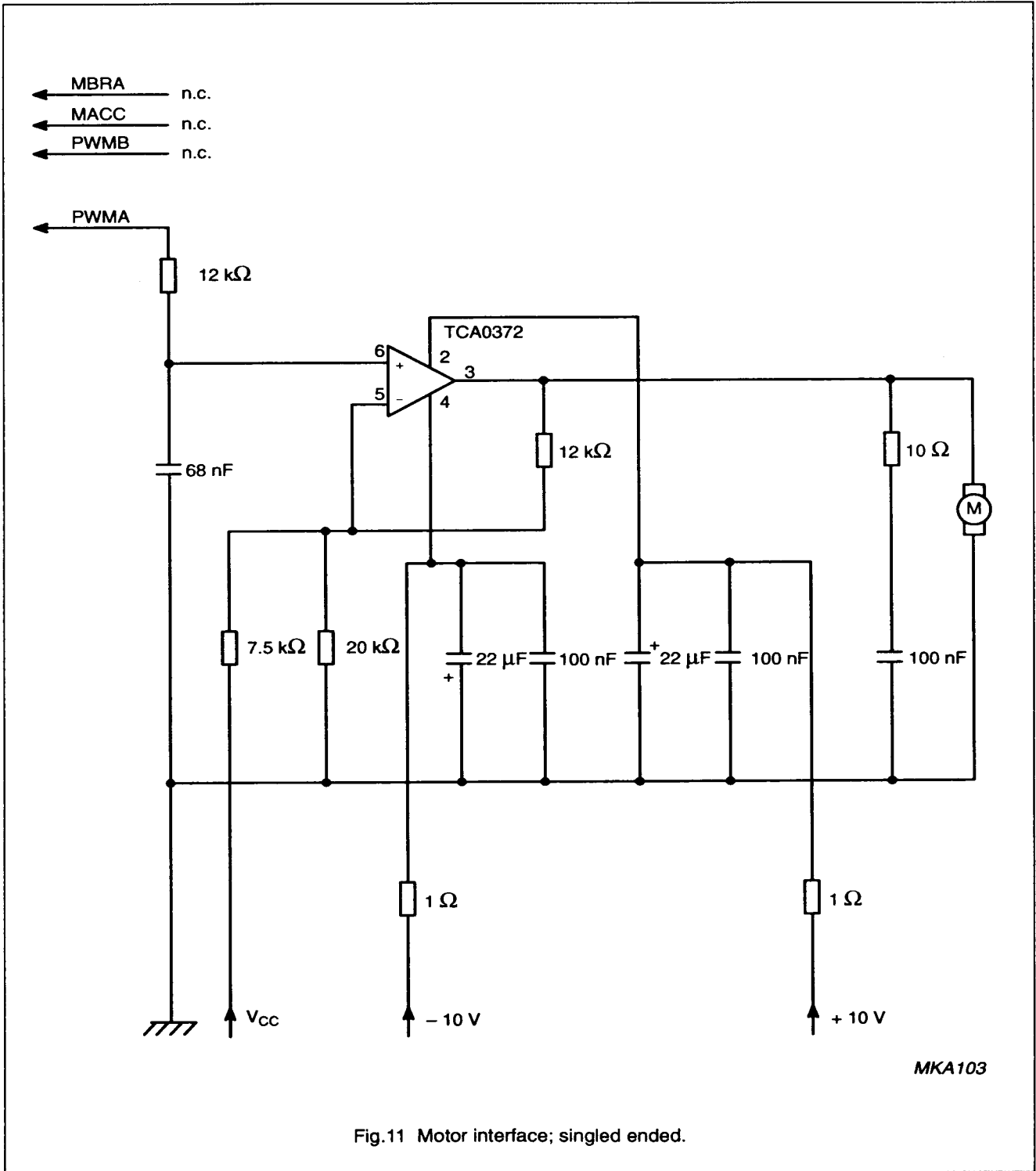


Fig.10 SRAM FCB61C65L configuration.

CMOS Digital decoding IC for Compact Disc

SAA7341



CMOS Digital decoding IC for Compact Disc

SAA7341

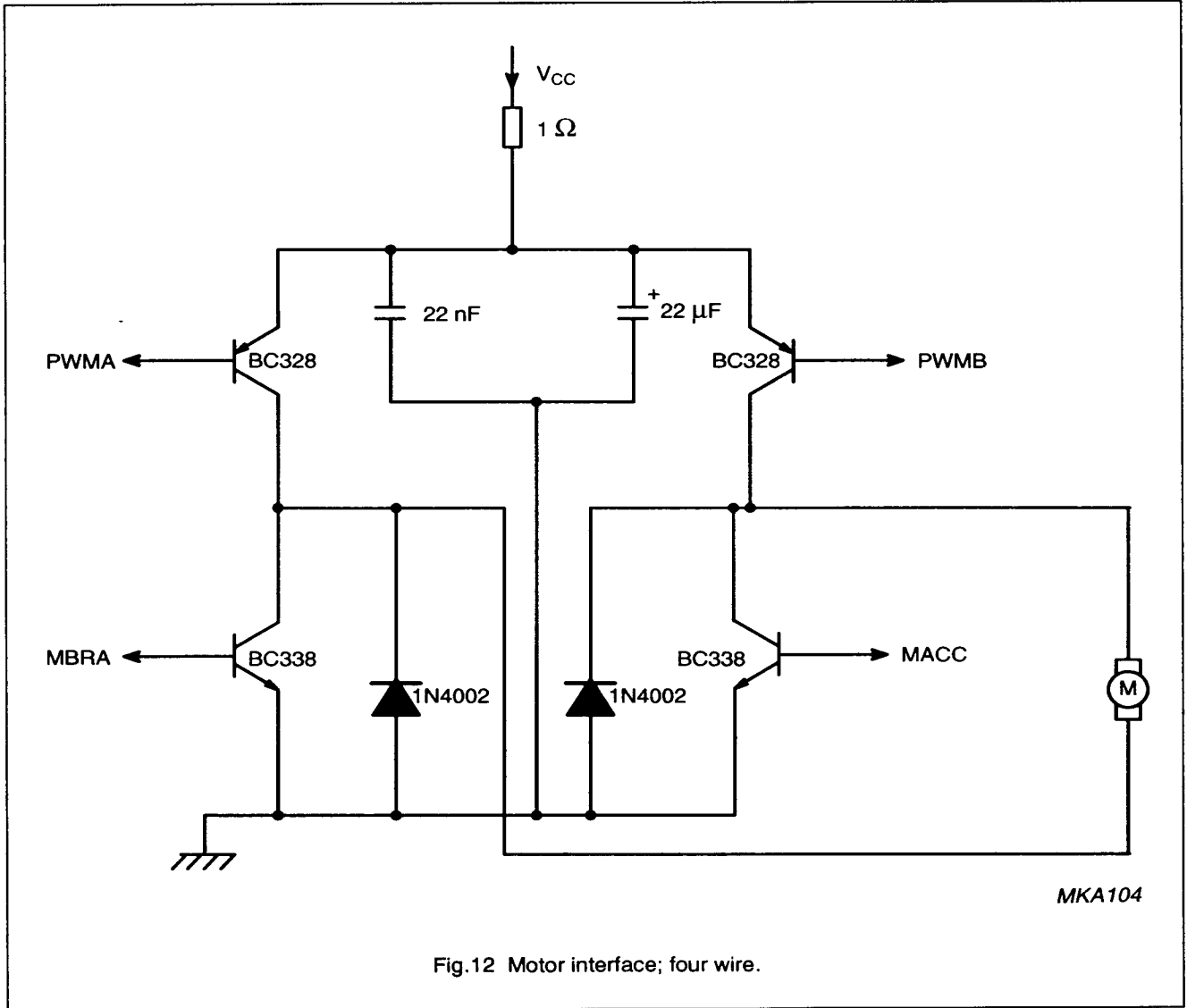
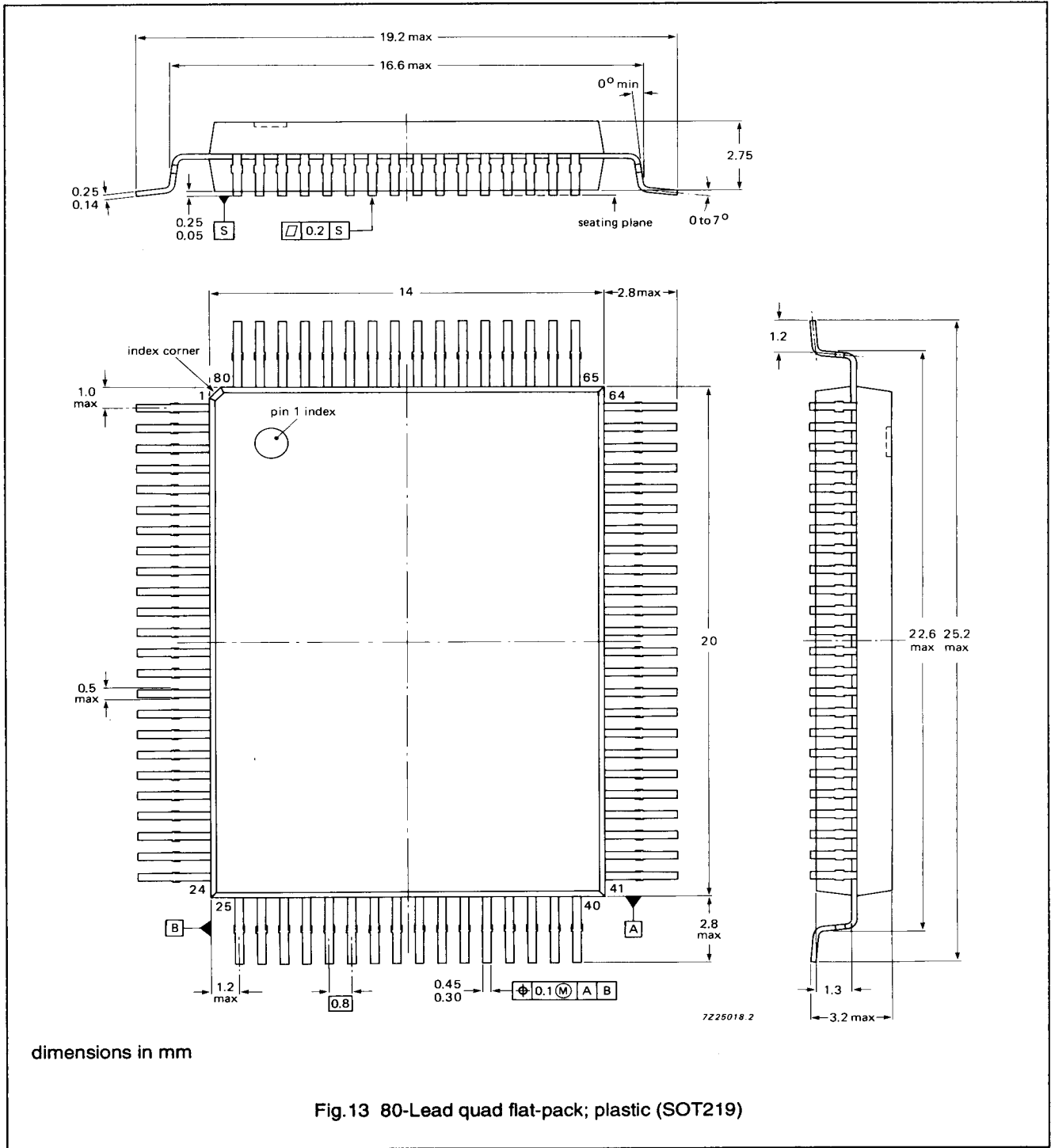


Fig.12 Motor interface; four wire.

CMOS Digital decoding IC for Compact Disc

SAA7341

PACKAGE OUTLINE



CMOS Digital decoding IC for Compact Disc

SAA7341

SOLDERING

Plastic quad-flat pack

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

| Data sheet status | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

Philips – a worldwide company

Argentina: PHILIPS ARGENTINA S.A., Div. Philips Components, Vedia 3892, 1430 BUENOS AIRES, Tel. (01)541-4261.

Australia: PHILIPS COMPONENTS PTY Ltd, 34 Waterloo Road, NORTH RYDE NSW 2113, Tel. (02)805 4455. Fax. (02)805 4466.

Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, 1101 WIEN, Tel. (0222)60 101-820.

Belgium: N.V. PHILIPS PROF. SYSTEMS – Components Div., 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02)52 56 111.

Brazil: PHILIPS COMPONENTS (Active Devices & LCD) Rua do Rocio 220, SAO PAULO-SP, CEP 4552, P.O. Box 7383, CEP 01051, Tel. (011)829-1166. Fax. (011)829-1849. PHILIPS COMPONENTS (Passive Devices & Materials) Av. Francisco Monteiro 702, RIBEIRAO PIRES-SP, CEP 09400, Tel. (011)459-8211. Fax. (011)459-8282.

Canada: PHILIPS ELECTRONICS LTD., Philips Components, 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. (416) 292-5161. (IC Products) PHILIPS COMPONENTS – Signetics Canada LTD., 1 Eva Road, Suite 411, ETOBICOKE, Ontario, M9C 4Z5, Tel. (416) 626-6676.

Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 77 38 16.

Colombia: IPRELENCO LTDA., Carrera 21 No. 56-17, BOGOTA, D.E., P.O. Box 77621, Tel. (01) 2 49 76 24.

Denmark: PHILIPS COMPONENTS A/S, Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. 32-88 33 33.

Finland: PHILIPS COMPONENTS, Sinkiallontie 3, SF-2630 ESPOO, Tel. 358-0-50261.

France: PHILIPS COMPOSANTS, 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01)40938000, Fax. 01 409 38692.

Germany: PHILIPS COMPONENTS UB der Philips G.m.b.H., Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040)3296-0, Fax. 040 329 69 12.

Greece: PHILIPS HELLENIQUE S.A., Components Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01)4894 339/4894 911.

Hong Kong: PHILIPS HONG KONG LTD., Components Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-42 45 121. Fax. 0 480 69 60.

India: PEICO ELECTRONICS & ELECTRICALS LTD., Components Dept., Shivasagar Estate 'A'Block, P.O. Box 6598, 254-D Dr. Annie Besant Rd., BOMBAY – 40018, Tel. (022) 49 21 500-49 21 515. Fax. 022 494 190 63.

Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Components Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan, JAKARTA 12910, Tel. (021)51 79 955.

Ireland: PHILIPS ELECTRONICS (IRELAND) LTD., Components Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01)69 33 55.

Italy: PHILIPS S.p.A., Philips Components, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02)6752.1, Fax. 02 675 226 42.

Japan: PHILIPS JAPAN LTD., Components Division, Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. (03)813-3740-5030. Fax. 03 813 3740 0570.

Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD. Components Division, Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02)794-5011.

Malaysia: PHILIPS MALAYSIA SDN BHD, Components Div., 3 Jalan SS15/2A SUBANG, 47500 PETALING JAYA, Tel. (03)7345511.

Mexico: PHILIPS COMPONENTS, Paseo Triunfo de la Republica, No 215 Local 5, Cd Juarez CHI HUA HUA 32340 MEXICO Tel. (16) 18-67-01/02.

Netherlands: PHILIPS NEDERLAND B.V., Marktgroep Philips Components, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 78 37 49.

New Zealand: PHILIPS NEW ZEALAND LTD., Components Division, 2 Vagener Place, C.P.O. Box 1041, AUCKLAND, Tel. (09)894-160, Fax. (09)897-811.

Norway: NORSK A/S PHILIPS, Philips Components, Box 1, Manglerud 0612, OSLO, Tel. (02) 74 10 10.

Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 72 57 72.

Peru: CADESA, Carretera Central 6.500, LIMA 3, Apartado 5612, Tel. 51-14-35 00 59.

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc., 106 Valero St. Salcedo Village, P.O. Box 911, MAKATI, Metro MANILA, Tel. (63-2)810-0161. Fax. 63 2 817 3474.

Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019)68 31 21.

Singapore: PHILIPS SINGAPORE, PTE LTD., Components Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 35 02 000.

South Africa: S.A. PHILIPS PTY LTD., Components Division, 195-215 Main Road, JOHANNESBURG 2000, P.O. Box 7430, Tel. (011)470-5434. Fax. (011)470 54 94.

Spain: PHILIPS COMPONENTS, Balmes 22, 08007 BARCELONA, Tel. (03)301 63 12. Fax. 03 301 42 43.

Sweden: PHILIPS COMPONENTS, A.B., Tegeluddsvägen 1, S-11584 STOCKHOLM, Tel. (08)78 21 000.

Switzerland: PHILIPS A.G., Components Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 488 22 11.

Taiwan: PHILIPS TAIWAN LTD., 581 Min Sheng East Road, P.O. Box 22978, TAIPEI 10446, Taiwan, Tel. 886-2-509 76 66. Fax. 886 2 500 58 99.

Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. (02)233-6330-9.

Turkey: TÜRK PHILIPS TICARET A.Ş., Philips Components, Talatpasa Cad. No. 5, 80640 LEVENT/ISTANBUL, Tel. (01) 179 27 70.

United Kingdom: PHILIPS COMPONENTS LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (071)580 6633, Fax. (071)436 21 96.

United States: (Colour picture tubes – Monochrome & Colour Display Tubes) PHILIPS DISPLAY COMPONENTS COMPANY, 1600 Huron Parkway, P.O. Box 963, ANN ARBOR, Michigan 48106, Tel. 313/996-9400. Fax. 313 761 2886. (IC Products) PHILIPS COMPONENTS – Signetics, 811 East Argue Avenue, SUNNYVALE, CA 94088-3409, Tel. (800) 227-1817. (Passive Components, Discrete Semiconductors, Materials and Professional Components & LCD) PHILIPS COMPONENTS, Discrete Products Division, 2001 West Blue Heron Blvd., P.O. Box 10330, RIVIERA BEACH, Florida 33404, Tel. (407)881-3200.

Uruguay: PHILIPS COMPONENTS, Coronel Mora 433, MONTEVIDEO, Tel. (02) 70-4044.

Venezuela: MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, CARACAS 1074A, App. Post. 78117, Tel. (02)241 75 09.

Zimbabwe: PHILIPS ELECTRICAL (PVT) LTD., 62 Mutare Road, HARARE, P.O. Box 994, Tel. 47211.

For all other countries apply to: Philips Components, Marketing Communications, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Telex 35000 phctnl, Fax. +31-40-724825

ADS92

© Philips Export B.V. 1991

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

9397 330 90011

Philips Semiconductors



28

JAN 13 1992

027406 ✓ - R