Section 1

Company Overview

Company Overview

About QLogic

Rapid developments in CPU architecture coupled with ever increasing levels of silicon integration continue to push today's information systems to new cost and performance levels. Furthermore, the rapid acceptance of multimedia in desktop applications requires today's PC to move ever increasing amounts of data in real time. As a result, I/O bandwidth frequently becomes a performance limiting factor.

In addition, today's powerful operating systems place massive demands on CPU power and real time response. Consequently, I/O controllers must increasingly strive to off-load I/O overhead from the CPU.

To meet this challenge, QLogic designs and supplies a wide range of silicon and board-level I/O solutions for peripheral and host applications.

By combining extensive experience in workstation, server, and midrange host and peripheral storage solutions with strong VLSI engineering expertise, QLogic continues to lead in SCSI product evolution and innovation. Recently, QLogic leveraged its expertise to expand product offerings to include Fibre Channel and enhanced Ultra integrated drive electronics (IDE) I/O solutions.

QLogic owns patents for its products and receives royalties from major industry suppliers for use of its technology.

Our Products

The company's products can be categorized into the following application areas:

- SCSI, IDE (ATA), and Fibre Channel hard drive controllers
- General purpose SCSI controllers
- PCI and SBus, SCSI and Fibre Channel controllers
- Host adapter boards

These products are described in the following sections.

SCSI, IDE (ATA), and Fibre Channel Hard Drive Controllers

The QLogic triple embedded controller (TEC) family provides single-chip, SCSI, Fibre Channel, and AT attachment (ATA) controller solutions for hard disk drive (HDD) applications. By integrating a disk formatter; buffer controller; and a SCSI, Fibre Channel, or ATA interface controller, these products reduce cost and space requirements in the increasingly competitive HDD marketplace, while providing the speed and throughput demanded by ongoing rapid advances in HDD technology.

TEC products address high-performance SCSI applications. ATEC products provide enhanced, Ultra IDE functionality for personal computer hard disk drives. FTEC products address very high-performance Fibre Channel applications.

QLogic hard disk drive controllers are sold to manufacturers of hard disk, removable disk, and optical disk drives.

General Purpose SCSI Controllers

The fast architecture SCSI (FAS) family has become an industry standard for stand-alone SCSI applications and is used in more SCSI applications world wide than any other SCSI architecture. FAS products provide the flexibility and performance required for 8- and 16-bit SCSI applications in tape drives, CD-ROMs, digital video disks (DVDs), HDDs, redundant array of inexpensive disks (RAID) storage boards, host adapters, and other peripheral products.

PCI and SBus, SCSI and Fibre Channel Controllers

The intelligent SCSI processor (ISP) family combines a 12-MIPS RISC processor and a high-performance I/O protocol engine (with versions for parallel SCSI and embedded transceiver Fibre Channel) on a single chip. These products are designed for PCI and SBus applications in high performance PCs, servers, workstations, and disk arrays.

The RISC processor allows communication with the host to take place at a very high level using the QLogic I/O control block (IOCB) command structure. This architecture dramatically simplifies driver software requirements while also ensuring driver transparency through new product generations. Therefore, once developed, drivers remain largely unchanged between 8-bit Fast SCSI, 16-bit Fast SCSI, Ultra SCSI, and Fibre Channel QLogic products.

Additionally, the RISC architecture significantly reduces host CPU involvement in I/O transfers, requiring a maximum of only one interrupt per I/O operation. Supporting full multithreading capability, ISP family products can handle over 1,000 concurrent I/O operations and execute up to 10,000 I/O operations per second (actual performance varies with system configuration and I/O transfer size).

The ISP Fibre Channel product (ISP2100) is especially notable for its integrated copper-media transceivers, enabling significant reductions in design cost and real estate requirements.

QLogic supplies host silicon products, and their supporting software drivers and firmware, to OEM system manufacturers and host adapter board manufacturers.

Host Adapter Boards

The QLA series of products provide high-performance single- and dual-channel SCSI and Fibre Channel connectivity for PCI host bus applications. QLogic also provides driver software for a wide range of operating systems. QLA products in both standard and customized versions are supplied to OEM system and subsystem manufacturers in the workstation, server, and high-performance PC marketplaces.

Support

Leveraging over 10 years of SCSI experience, QLogic also supplies firmware development support and code to chip product customers. This service reduces customer development risks while at the same time ensuring timely introduction of their product to the marketplace. By also providing cross-generation and cross-I/O platform firmware compatibility throughout the product range, QLogic further reduces customer development time and risk.

Product Leadership

QLogic has long been a leader in SCSI applications and has consistently supplied leading edge products. Continuing this positioning, new Fibre Channel products are currently available and allow transparent, drop-in silicon and board solutions that support data rates up to 100 Mbytes/sec. QLogic also intends to retain its leadership position by evolving its Fibre Channel products to support additional protocols such as IP (Internet Protocol).

The company enjoys a large base of leading OEM customers in both host and peripheral target applications areas. This base provides a wealth of market input, which in turn ensures ongoing expert product leadership. By adding responsive, expert technical support, QLogic continues to maintain its strong position in the industry.

QLogic Corporation Quality Program

QLogic Corporation is a fabless manufacturer of CMOS ASIC (SCSI solution) devices whose objectives are to exceed industry standard quality requirements. With this goal in mind, QLogic achieved ISO9001 and TickIt certification (BSI-FM29583) in the fall of 1994.

The quality program's primary focus is to continuously improve its processes and to deliver high-quality products to all customers. Under this program, QLogic works closely with its suppliers to achieve these objectives.

QLogic's Quality Program covers all aspects of manufacturing, from design to finished product. Internal audits are performed at scheduled intervals to meet both ISO9001 requirements and the company's quality objectives.

The quality program uses statistical methods to monitor and measure improvements in all areas of the company. Training provides continuous growth to all employees to enable them to be proactive.

The key aspects of the quality program are design control, auditing, reliability, failure analysis, and total customer satisfaction.

- **Design Control.** QLogic's design control meets the special requirements of ISO9001, TickIt, and ISO900-3, and implements continuous design improvements.
- **Auditing.** QLogic has a comprehensive internal auditing program using highly trained auditors who continuously employ new approaches to ensure that the organization's quality objectives are met.
- **Reliability.** QLogic's reliability program covers a full complement of qualification testing and ongoing monitoring and control of suppliers through a comprehensive failure analysis and corrective action system.
- **Failure Analysis.** QLogic maintains full failure analysis capability in-house. Failure analysis determines the root cause and establishes closed-loop corrective action.
- **Total Customer Satisfaction.** QLogic logs and interprets performance and quality inputs from customers, along with requests for special requirements. This information further improves all aspects of the quality system.

Section 2

Product Overview

Chip Family

SCSI Interface Processors	Single Ended	Differential	8-bit DMA	16-bit DMA	8-bit SCSI/Narrow	16-bit SCSI/Wide	Fast SCSI (10 Mxfer/sec)	Ultra SCSI (20Mxfer/sec)	SCAM	Parity Pass Through	Active Negation	Block Commands	Package	Additional Information
FAS101	✓	✓	✓		✓		✓						68-pin PLCC	ESP100A pin compatible
FAS201	✓	✓	✓		✓		✓			✓			68-pin PLCC	ESP200 pin compatible
FAS209[a]	✓		✓		✓		✓		✓		✓		64-pin PQFP	Also 64-pin TQFP
FAS216[a]	✓		✓	✓	✓		✓			✓			84-pin PLCC	ESP216 pin compatible
FAS216U[a]	✓		✓	✓	✓		✓	✓	✓	✓	✓		84-pin PLCC	FAS216 pin compatible, Ultra SCSI
FAS226[a]		✓	✓	✓	✓		✓			✓			84-pin PLCC	ESP226 pin compatible
FAS236[a]	✓	✓	✓	✓	✓		✓			✓			100-pin PQFP	ESP236 pin compatible
FAS236U[a]	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓		100-pin PQFP	FAS236 pin compatible, Ultra SCSI
FAS246A	✓		✓	✓	✓		✓			✓	✓		80-pin PQFP	
FAS366	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	128-pin PQFP	32-bit transfer counter
FAS366U[a]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	128-pin PQFP	FAS366 pin compatible, Ultra SCSI
Intelligent SCSI Processors														
ISP1000	✓	✓			✓	✓	✓			n/a	✓	n/a	208-pin PQFP	SBus
ISP1000U	✓	✓			✓	✓	✓	✓		n/a	✓	n/a	208-pin PQFP	SBus, Ultra SCSI
ISP1040B	✓	✓			✓	✓	✓	✓		n/a	✓	n/a	208-pin PQFP	PCI, Ultra SCSI
ISP1080	✓	b			✓	✓	✓	✓		n/a	✓	n/a	352-pin BGA	64-bit PCI, LVD Ultra2 SCSI
ISP1240	✓	✓			✓	✓	✓	✓		n/a	✓	n/a	352-pin TE BGA	64-bit PCI, dual channel Ultra SCSI
SCSI Disk Controllers														
TEC376	✓			✓	✓		✓	✓	✓	✓	✓	✓	100-pin PQFP	Headerless disk, XOR, Ultra SCSI
TEC386	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	120-pin PQFP	Headerless disk, XOR, Ultra SCSI
TEC420	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	128-pin PQFP	Enhanced bandwidth and data rate

Table Notes

[a]Split bus architecture (separate DMA bus and processor bus)

[b]LVD Ultra2

ATA Disk Controller

ATEC378, 128-pin PQFP, Ultra DMA, 33-ATA HDC

Fibre Interface Processors	Single Loop FC-AL	Dual Loop FC-AL	32-bit DMA	Integrated Transceivers	64-bit PCI	10-bit Interface	On-chip 8B/10B	106 MB/sec	On-board Frame Buffers	Package	Additional Information
FTEC440		✓	✓	✓		✓	✓	✓		225-pin BGA	FC-AL disk controller

Fibre Interface Processors	Single Loop FC-AL	Dual Loop FC-AL	32-bit DMA	Integrated Transceivers	64-bit PCI	10-bit Interface	On-chip 8B/10B	106 MB/sec	On-board Frame Buffers	Package	Additional Information
ISP2100	✓			✓	✓	✓	✓	✓	✓	256-pin BGA	PCI–to–FC-AL adapter

Board Family

PCI Bus for PCI	Application	SCSI in MB/sec	Dual Channel Ext SCSI	Narrow (8-bit) Support	Wide (16-bit) Support	Software Drivers Support	Integrated Transceivers	Flash ROM BIOS	Additional Information
QLA1040	Workstation/Server	40		✓	✓	a		✓	
QLA1041	Workstation/Server	40		✓	✓	a		✓	Differential Support
QLA1042	Workstation/Server	40	✓	✓	✓	a		✓	
QLA1042D	Workstation/Server	40	✓	✓	✓	a		✓	Differential Support
PCI Bus for Fibre Channel									
Fibre Channel Development Board	Workstation/Server	100				a	✓	✓	

Table Notes

[a]Software drivers: AIX, BIOS, DOS ASPI, I20 IXWorks, NetWare4.X, OS/2 Warp, SCO 5.0, Solaris, UnixWare Gemini, UnixWare 2.1, VX Works, Windows 95, Windows NT 4.0

Section 3

Parallel SCSI Products

FAS209
Fast SCSI Processor

Features

- Compliance with ANSI SCSI-2 standard X3.131-1994 and SCSI-1
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Synchronous data transfers up to 10 Mbytes/sec fast SCSI and 5 Mbytes/sec normal SCSI
- Asynchronous data transfers up to 7 Mbytes/sec
- Up to 12 Mbytes/sec DMA burst transfer rate
- Clock rates up to 40 MHz
- Supports hot plugging
- Programmable active negation
- Low-input capacitance
- Programmable split-bus architecture
- DMA interface options
- Two bus configurations
- On-chip, 48-mA, single-ended drivers and receivers
- Parity pass-through on FIFO data
- Initiator and target roles
- SCSI sequences implemented without microprocessor intervention
- Part-unique ID code
- Eight-bit, single-ended SCSI operations

Product Description

The FAS209 is a high-performance SCSI interface chip designed to maximize transfer rates over the SCSI bus. It is the enhanced SCSI follow-on to QLogic's FAS216 SCSI processor chip, adding active negation and SCAM to the FAS216 design. The FAS209 supports bidirectional, single-ended SCSI operations. The FAS209 block diagram is illustrated in figure 1.

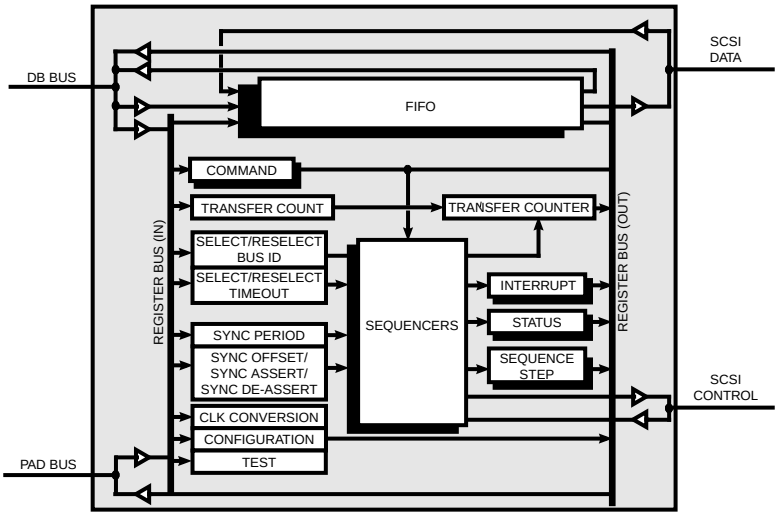


Figure 1. FAS209 Block Diagram

The FAS209 maximizes transfer rates by sustaining asynchronous data rates of up to 7 Mbytes/sec and fast, synchronous data transfer rates of up to 10 Mbytes/sec. The normal 5 Mbytes/sec synchronous transfer rate is also supported. With its on-chip, 48-mA, single-ended drivers and receivers, the FAS209 connects directly to the SCSI bus, minimizing board space requirements. The FAS209's highly integrated structure provides users with numerous benefits.

Initiator and target roles are supported; therefore, the FAS209 can be used in both host adapter and peripheral applications. The FAS209 performs such functions as bus arbitration, selection of a target, or reselection of an initiator. It handles message, command, status, and data transfer between the SCSI bus and the chip's 16-byte internal FIFO or a buffer memory. The above functions are internal processes performed by the FAS209 chip without microprocessor intervention.

SCAM Implementation

The FAS209 supports levels 1 and 2 of the SCAM protocol. (Refer to the latest revision of X3T10/855D, Annex B.) SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

Bus Configuration

The FAS209 split-bus architecture separates the two high-traffic information buses of the system, providing maximum efficiency and throughput. The versatile bus architecture supports various microprocessor and DMA bus configurations, including those listed below:

- Microprocessor interface via the PAD bus or the DB bus
- Concurrent microprocessor and DMA accesses
- PAD bus selectable as a data-only bus

FAS209 bus configuration is selected by pulling the MODE pin up or down, as shown in table 1.

Table 1. Bus Modes

Mode No.	MODE Pin	Register Data	DMA Data	Configuration
0	0	DB bus	DB bus	Single bus, 8-bit DMA
1	1	PAD bus	DB bus	Split bus, 8-bit DMA

Interfaces

The FAS209 interfaces include the microprocessor interface and DMA interface. Pins that support these interfaces and other chip operations are shown in figure 2.

Microprocessor Interface

Microprocessor interface to the FAS209 occurs over the PAD bus or the DB bus. Both interfaces allow the microprocessor to read and write to all the internal chip registers, including the FIFO.

In single-bus mode (bus configuration mode 0), the PAD bus is not used and the microprocessor must arbitrate with other controllers for use of the DB bus. In split-bus mode (bus configuration mode 1), the PAD bus is dedicated to the microprocessor interface.

DMA Interface

All FAS209 DMA activity occurs over the DB bus. The path is eight bits wide. The DB bus consists of the data parity pin DBP0 and data pins DB7-0. Data is transferred on DB7-0 on writes to and reads from the SCSI bus.

$\overline{\text{DACK}}$ must be active during DMA accesses. The transfer direction is determined by the type of command executed by the chip. $\overline{\text{DBWR}}$ strobes data into the chip. DMA read data is driven by the chip when $\overline{\text{DACK}}$ is true.

Packaging

The FAS209 is available in a 64-pin plastic quad flat pack (PQFP) and a thin quad flat pack (TQPF).

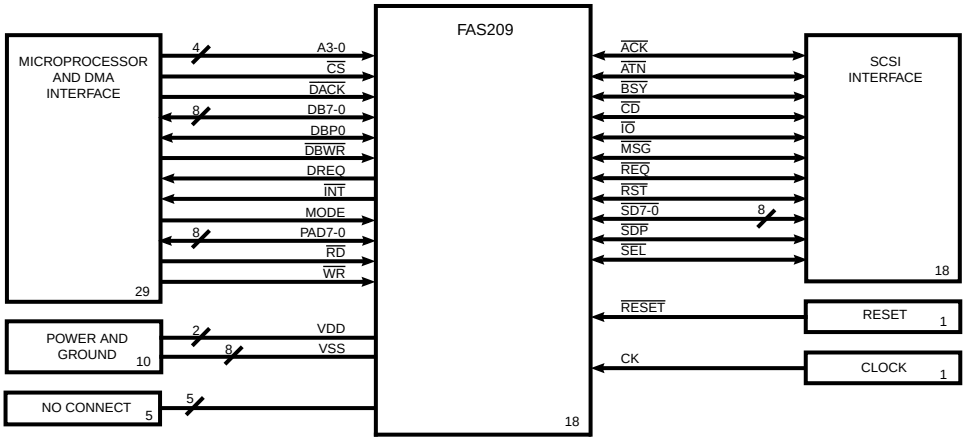


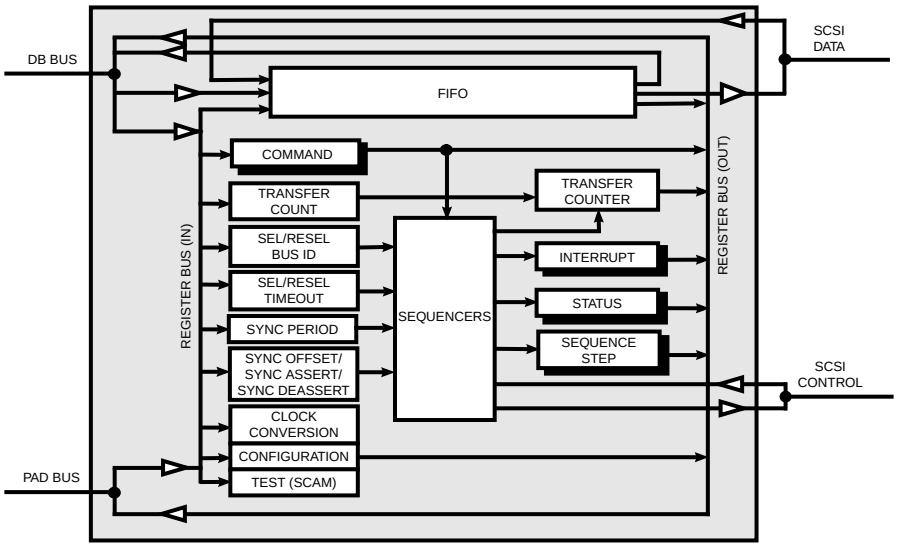
Figure 2. FAS209 Functional Signal Grouping

FAS216/216U/236/236U
Fast Architecture SCSI Processor

Features

- Host application and 16-bit peripheral application support
- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI X3T10/1071D Fast-20 standard
- Asynchronous data transfers up to 7 Mbytes/sec
- Synchronous data transfers up to 5 Mbytes/sec (normal SCSI), 10 Mbytes/sec (fast SCSI), and 20 Mbytes/sec (Ultra SCSI)
- Programmable synchronous transfer period
- Programmable synchronous transfer offsets up to 15 bytes
- 24-bit transfer counter
- Initiator and target modes
- Differential driver protection (DIFFSENS)
- DMA burst transfer rate up to 20 Mbytes/sec
- Pipelined command structure
- 16-byte data FIFO between DMA and SCSI channels
- Parity pass-through on FIFO data
- Part-unique ID code
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Clock rates up to 40 MHz

NOTE: Throughout this catalog, the term *FAS2x6* refers to the FAS216, FAS216U, FAS236, and FAS236U unless otherwise noted.



NOTE: SCAM APPLIES TO THE FAS216U AND FAS236U ONLY.

Figure 1. FAS2x6 Block Diagram

Product Description

The FAS2x6 chips are part of the QLogic SCSI processor family with features designed to facilitate SCSI-2 support (FAS216 and FAS236) and SCSI-3 support (FAS216U and FAS236U). The FAS216 and FAS236 can transfer synchronous data at 10 Mbytes/sec. The FAS216U and FAS236U can transfer data at 20 Mbytes/sec with SCAM support. The normal 5-Mbytes/sec transfer rate and the fast 10-Mbytes/sec transfer rate (FAS216U and FAS236U) are supported on-chip by setting the FASTSCSI bit (Configuration 3 register bit 4). Asynchronous transfers up to 7 Mbytes/sec are also supported. The FAS216U and FAS236U chips are firmware and pin compatible with the FAS216 and FAS236 chips, respectively. Figure 1 shows the FAS2x6 block diagram.

The FAS2x6 replaces existing SCSI interface circuitry, which typically consists of discrete devices, an external driver, and a low-performance SCSI interface chip. The FAS2x6 contains a fast DMA interface; a 16-byte FIFO; and fast asynchronous and synchronous data interfaces to the SCSI bus, including drivers in single-ended mode. Differential mode requires external drivers.

The FAS216 and FAS216U support single-ended mode; the FAS236 and FAS236U support single-ended and differential modes. Since the FAS2x6 operates in both initiator and target modes, it can be used in both host and peripheral applications. The chip performs such functions as bus arbitration, selection of a target, and reselection of an initiator. The FAS2x6 also handles message, command, status, and data transfers between the SCSI bus and its internal FIFO or between the SCSI bus and buffer memory. The chip maximizes protocol efficiency by utilizing a FIFO command pipeline and combination commands to minimize host intervention.

Differential Driver Protection (FAS236/236U Only)

The FAS236/236U pins 5 (DIFFSENS) and 7 (EDIFFS) support the SCSI DIFFSENS differential driver protection function.

The DIFFSENS function is enabled in differential mode when pins 5 and 7 are pulled up by an external device. The FAS236/236U is configured for differential mode operations when pin 87 (DIFFM) is low. If a single-ended device or terminator is connected while the chip is configured for differential operations, DIFFSENS becomes grounded, disabling the differential drivers. The Gross Error bit (Status register bit 6) is set and a disconnect interrupt is generated. The Gross Error bit and the disconnect interrupt are asserted as long as the DIFFSENS condition exists. The DIFFSENS function has no effect in single-ended mode.

SCAM Implementation

The FAS216U and FAS236U support levels 1 and 2 of the SCAM protocol. SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the chip hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

System Organization

The FAS2x6 controller systems support three main buses: the 8- or 16-bit data bus (DB), the 8-bit microprocessor address and data bus (PAD), and the 8-bit SCSI bus. The DB provides a path for DMA transfers through the FIFO. The PAD bus provides access to all internal registers. The FAS2x6 supports parity pass-through from the SCSI bus through the FIFO to the DB. This versatile split-bus architecture separates the two high-traffic information flows, the SCSI bus and DB bus, to provide maximum efficiency and throughput. Single- or split-bus configurations with 8- or 16-bit DMA are pin selectable.

Interfaces

The FAS2x6 acts as an interface between the microprocessor and the SCSI bus in target or initiator mode. The other interfaces are described in the following sections.

Pins that support the FAS216/216U and FAS236/236U operations are shown in figures 2 and 3.

Microprocessor Interface

The DB or PAD bus is the microprocessor interface to the FAS2x6. Both buses allow the microprocessor eight-bit read and write access to all chip registers, including the FIFO. The PAD bus allows microprocessor interface to the chip registers independent of DMA activity on the DB.

DMA Interface

The FAS2x6 logic transfers data to and from a buffer over the DB configured as 8 or 16 bits. (Each byte on the bus has its own parity.) If byte control mode (Configuration 2 register bit 5) is set, an external DMA controller dictates how the bytes are placed on the bus.

Packaging

The FAS216/216U is available as an 84-pin plastic leaderless chip carrier (PLCC); the FAS236/236U is available as a 100-pin plastic quad flat pack (PQFP).

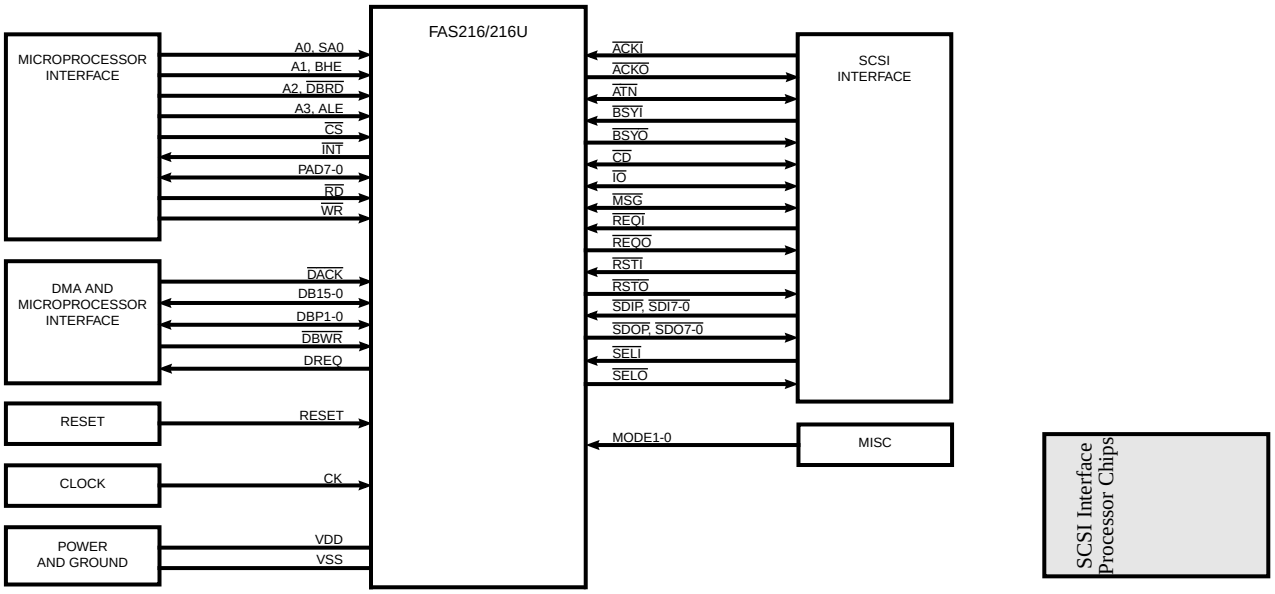


Figure 2. FAS216/216U Functional Signal Grouping

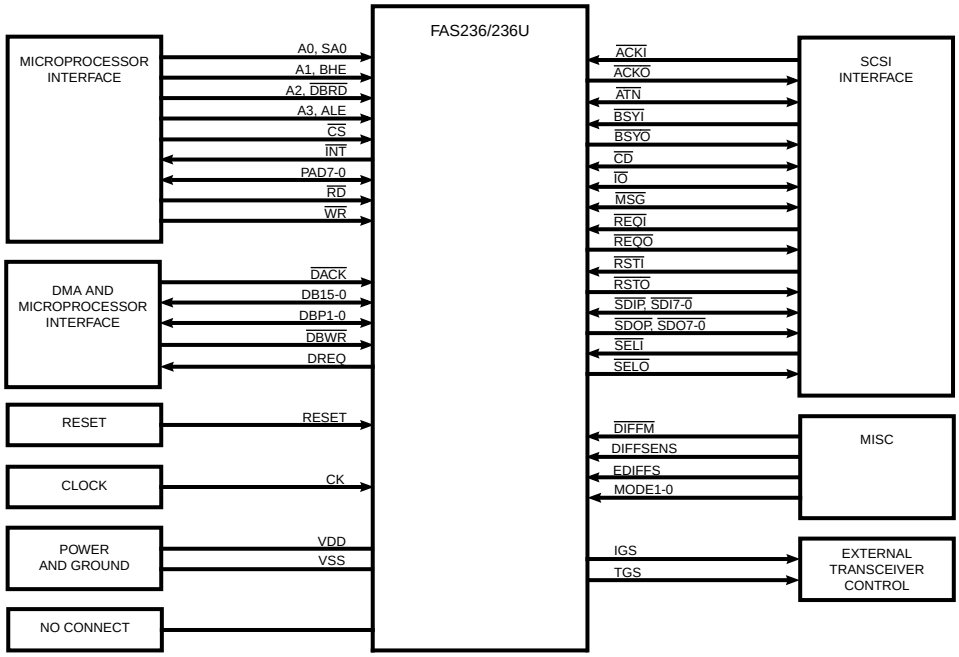


Figure 3. FAS236/236U Functional Signal Grouping

FAS366U
Fast Architecture SCSI Processor

Features

- Compliance with ANSI X3T10/1071D Fast-20 standard
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Sustained SCSI data transfer rates of up to:
  - ❒ 40 Mbytes/sec synchronous (Ultra and wide SCSI)
  - ❒ 14 Mbytes/sec asynchronous (wide SCSI)
- Synchronous DMA timing; DMA speed of 50 Mbytes/sec
- $\overline{REQ}$ and $\overline{ACK}$ programmable assertion and deassertion control
- Support for hot plugging
- Target and initiator block transfer sequences
- Bus idle timer
- Split-bus architecture
- Pipelined command structure
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Initiator and target roles
- Active negation
- 16-bit recommand counter
- Differential mode
- SCSI bus reset watchdog timer

Product Description

The FAS366U is a new addition to the QLogic fast architecture SCSI processor (FAS) chip family. The FAS366U supports advanced SCSI-3 options including Ultra SCSI synchronous transfers. Also included is the advanced SCAM level 2 SCSI controller core.

The FAS366U is a single-chip controller for use in host and peripheral applications. It is firmware and pin-out compatible with the QLogic FAS366 chip. The FAS366U block diagram is shown in figure 1.

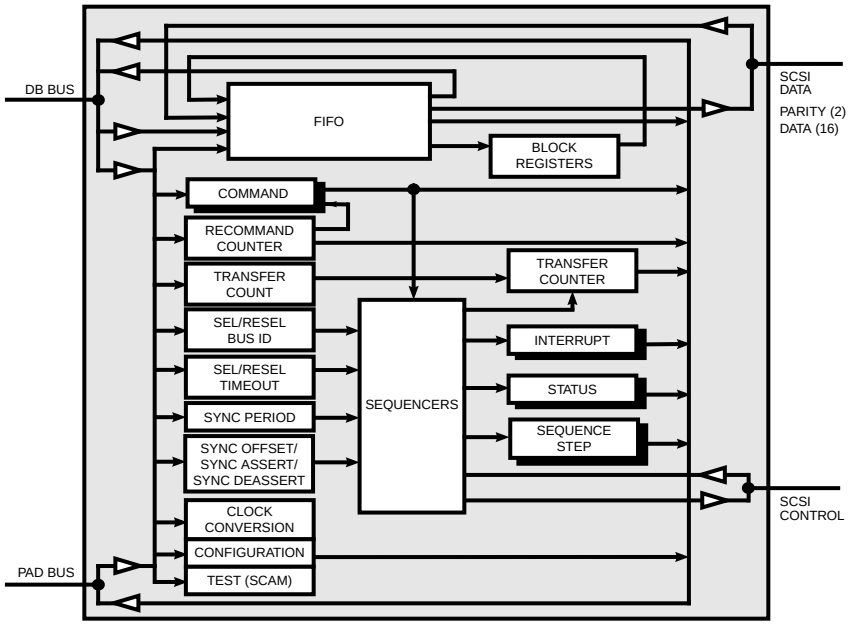


Figure 1. FAS366U Block Diagram

The FAS366U implements QLogic's new SCSI target and initiator block transfer sequences. The block sequences reduce firmware overhead and are composed of the following new commands: Target Block Sequence (including the bus idle timer), Initiator Block Sequence, Load/Unload Block Registers Sequences, Abort Block Sequence, and Disconnect Abort Block Sequence.

The FAS366U supports both single-ended and differential mode SCSI operations and operates in initiator and target roles. The FAS366U has been optimized for interaction with a DMA controller and the controlling microprocessor.

The versatile split-bus architecture supports various microprocessor and DMA bus configurations. A separate 8-bit microprocessor bus (PAD) provides access to all internal registers, and a 16-bit DMA bus (DB) provides a path for DMA transfers through the FIFO. Each bus is protected by a parity bit (byte-wide parity) to improve data integrity. During data transfers, the microprocessor has instant access to status and has the ability to execute commands.

SCAM Implementation

The FAS366U supports levels 1 and 2 of the SCAM protocol. (Refer to the latest revision of X3T10/855D, Annex B.) SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

Fast DMA Protocol

The fast DMA protocol is required for supporting the full bandwidth of Ultra, wide SCSI.

The DREQ signal initiates DMA transfers and runs asynchronous to the user's clock. For read operations, $\overline{\text{DACK}}$ acts as a chip select to enable the FAS366U drivers onto the DMA bus. The chip select role of $\overline{\text{DACK}}$ helps support the burst timing of fast DMA mode. $\overline{\text{DACK}}$ selects the FAS366U after DREQ is asserted and is removed either after DREQ is deasserted or when the DMA transfer is paused.

$\overline{\text{DBRD}}$ requests data from the FAS366U and $\overline{\text{DBWR}}$ validates data sent to the FAS366U. Data is valid around the rising (trailing) edge of $\overline{\text{DBRD}}$ or $\overline{\text{DBWR}}$.

DMA transfers are terminated by deasserting DREQ. Deassertion of DREQ is triggered by the leading edge of $\overline{\text{DBRD}}$ or $\overline{\text{DBWR}}$ under any of the following conditions:

- To prevent FIFO overrun conditions
- To prevent FIFO underrun conditions
- When the required amount of data has been transferred

When DREQ is deasserted, the FAS366U ignores $\overline{\text{DBRD}}$ and $\overline{\text{DBWR}}$. Data transfers do not take place unless DREQ is asserted.

The FAS366U does not generate parity on the incoming DMA bus. Correct parity must always be supplied with the data.

The DMA interface signals are described in table 1.

Table 1. DMA Interface Signals

Pin	Type	Active Level	Description
DREQ	O	High	The FAS366U DMA request line begins and ends DMA cycles.
$\overline{\text{DACK}}$	I	Low	The acknowledge is used as a chip select to activate FAS366U drivers and to acknowledge acceptance of DREQ.
$\overline{\text{DBRD}}$	I	Rising edge	The trailing edge accepts data from the FAS366U for DMA read operations.
$\overline{\text{DBWR}}$	I	Rising edge	The trailing edge strobes data into the FAS366U FIFO on DMA write operations.
DB15-0	I/O	N/A	This is the DMA data bus.

Interfaces

The FAS366U interfaces include the microprocessor bus and the SCSI bus. Pins that support these interfaces and other chip operations are shown in figure 2.

Packaging

The FAS366U is available in a 128-pin plastic quad flat pack (PQFP).

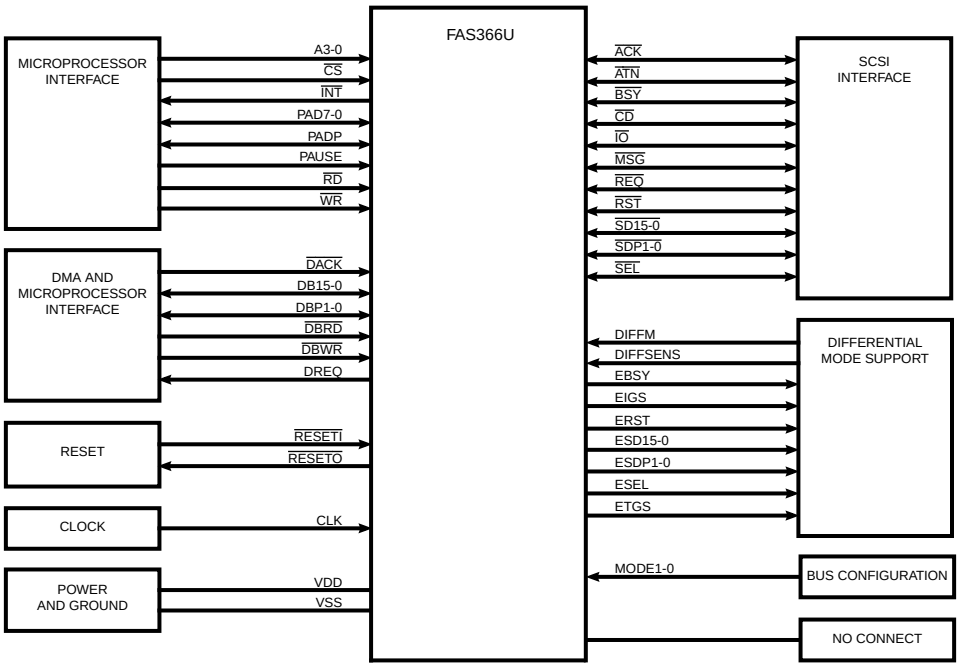


Figure 2. FAS366U Functional Signal Grouping

TEC376/386
Triple Embedded Controller

Features

- Compliance with ANSI SCSI configured automatically (SCAM) protocol
- Compliance with ANSI X3T10/1071D Fast-20 standard
- Wide, 16-bit Ultra SCSI synchronous data transfer rates up to 40 Mbytes/sec and asynchronous up to 14 Mbytes/sec (TEC386)
- Narrow, eight-bit Ultra SCSI synchronous data transfer rates up to 20 Mbytes/sec and asynchronous up to 7 Mbytes/sec (TEC376)
- Multithread automation
- Initiator and target support for automated disconnection and reconnection
- Differential support (TEC386)
- Disk data rate of 16 Mbytes/sec
- Enhanced, programmable Reed Solomon 144- or 192-bit ECC data field protection with on-the-fly, quadruple-burst error correction
- ID-less disk formatter providing magnetoresistive (MR) head support
- 16-bit DMA bandwidth of 40 Mbytes/sec peak, 36 Mbytes/sec sustained
- Table search tool to support sophisticated disk caching operations
- Data protection with buffer CRC (BCRC)
- Enhanced data streaming support
- Hardware XOR (exclusive OR) function at DMA speeds (TEC386)
- Logical block address (LBA) seeder and checker
- Dual TEC mode to support dual ported applications

Product Description

The TEC376/386 triple embedded controller is part of the QLogic family of high-performance, low-cost, single-chip, disk data controllers for use in host and peripheral applications. The TEC376/386 provides a state-of-the-art disk formatter, a high-speed buffer controller, and Ultra SCSI synchronous transfer rates (see figure 1). The TEC376/386 SCSI controller core provides advanced SCAM level 1 and level 2 support.

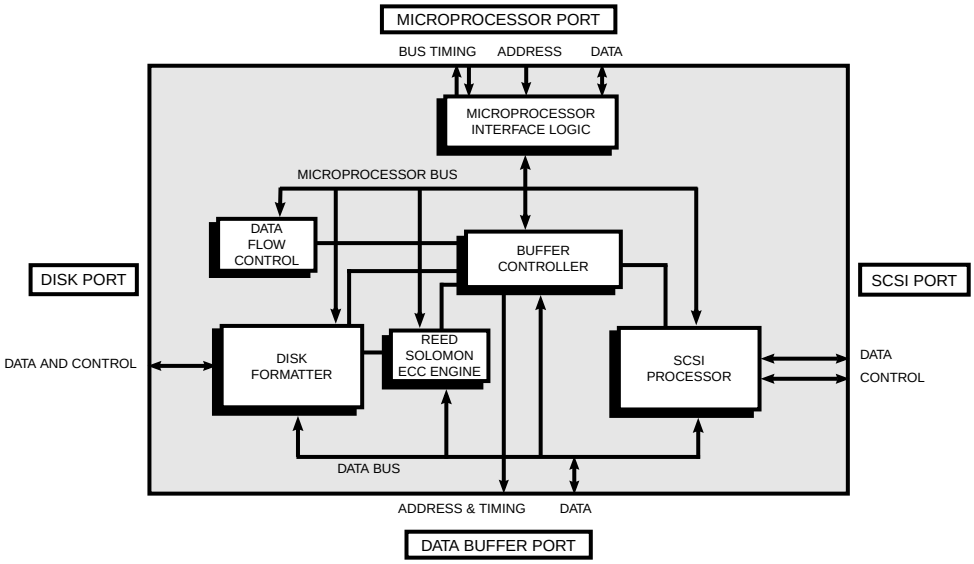


Figure 1. TEC376/386 Block Diagram

The TEC376/386 supports QLogic's SCSI Target Block Sequence and Initiator Block Sequence that reduce interrupt overhead in single-thread and multithread operations by implementing SCSI firmware sequences in the hardware. The block sequences are composed of the following new commands: Target Block Sequence (including the bus idle timer), Initiator Block Sequence, Load and Unload Block Registers Sequences, Abort Block Sequence, and Disconnect Abort Block Sequence.

The TEC386 supports both single-ended SCSI and differential SCSI mode operations (the TEC376 supports single-ended SCSI operations only), operates in initiator and target roles, and supports XOR operations. The TEC376/386 microprocessor interface is optimized to support DMA access of buffer memory. In addition, the TEC376/386 maximizes protocol efficiency with a FIFO command pipeline and stacked commands to minimize host intervention.

The TEC376/386 is designed for use in high-performance 3.5-inch and 2.5-inch embedded SCSI disk drive designs.

Product Architecture

SCSI Processor

The TEC376/386 SCSI processor supports the following:

- Ultra SCSI data rates of 20 Mtransfers at 40 Mbytes/sec for TEC386 and 20 Mbytes/sec for TEC376
- Compliance with the ANSI X3.131-1994 SCSI-2 standard
- Compliance with the ANSI X3T10-855D SCSI-3 parallel interface (SPI) standard
- SCSI-3 message support
- Programmed active negation
- Differential support (TEC386)

The TEC376/386 SCSI bus interface provides direct, single-ended SCSI bus control. The TEC386 also provides differential SCSI bus control. The TEC376/386 SCSI processor consists of programmable registers and state machine sequencers that interface to the SCSI bus on one side and to a fast, buffered DMA channel on the other. A high-level state machine performs the selection and reselection sequences, and several low-level state machines perform the actual SCSI bus cycle operations.

Disk Formatter

The TEC376/386 disk formatter supports the following:

- On-the-fly correction up to 12 bytes
- Embedded servo field skipping support
- Variable length sectors up to 5966 bytes

The disk formatter is a full-function, disk interface controller. The disk formatter structure contains a data FIFO, ECC engine, and a writable control store (WCS) state machine. Buffer controller DMA channel 0 is dedicated to the disk formatter.

The disk interface control operation occurs when the local microprocessor loads all required control information and parameter values into the WCS RAM, then issues a command. The disk formatter automatically executes the command with no further microprocessor intervention required.

The disk formatter performs all operations while fully supporting sector splits for embedded servo disk drives. Embedded servo support consists of a servo split count value from the DRAM-based table, counters, and a timer. The TEC376/386 has the ability to split a data field or ECC field around a servo cell.

A powerful 144- or 192-bit Reed Solomon code provides ECC protection for the data field. This code supports quadruple-burst, on-the-fly correction up to 96 bits. With error logging, the TEC376/386 supports up to 5966 byte sectors.

MR-head support is accomplished with ID-less architecture that enhances capacity and throughput. IDs and sector pulses generated from a DRAM-based table are fetched for each servo cell on the track.

Buffer Controller

The TEC376/386 buffer controller supports the following:

- Maximum buffer size of 8 Mbytes (TEC386) and 512 Kbytes (TEC376)
- Page mode or static column mode DRAMs for fast burst DMA

The TEC376/386 buffer management is provided by a four-channel, high-speed, bursting DMA controller. The buffer controller connects the buffer DRAM to the disk channel, ECC channel, SCSI channel, and the microprocessor bus. The buffer controller regulates all data movement into and out of DRAM buffer memory. Each DMA channel supports DMA bursting, which maintains the optimal bandwidth. The disk and SCSI channels each have a 16-word deep FIFO. Each DMA channel has associated control, configuration, and buffer memory address registers.

The buffer controller also provides microprocessor address decoding, priority arbitration for the buffer resource, BCRC, and automatic DRAM refresh control.

The buffer controller table search tool compares 16 or 32 bits to a table of numbers, such as an LBA, to provide high-speed lookups for cache, zone, defect, and other searches required by the system.

An XOR engine running at DMA speeds generates an XOR of two data buffers to support the SCSI-3 redundant array of inexpensive disks (RAID) commands in the TEC376/386. RAID commands include XDRead, XDWrite, and XDParity.

To facilitate firmware debugging and to guarantee data integrity, LBA seeding is provided for all data blocks written to the disk.

Data Flow Control

Data Flow reduces data transfer time by automatically monitoring and controlling the flow of data between the disk and the SCSI channels. This is accomplished by reducing the number of interrupts that occur in a typical disk-to-SCSI data transfer. When the disk and SCSI data transfer rates are the same, both channels transfer data at the maximum rate, which prevents slipped sectors in the disk port and periods of inactivity during the data phases of a SCSI bus transfer.

Data Flow automatically prevents buffer overflow and underflow conditions by temporarily suspending (pausing) the disk formatter or SCSI processor DMA channel before the buffer becomes full or empty. To stop the disk formatter on sector boundaries and not in the middle of a data field, the disk formatter is paused by suspending the start of any disk sequence after a sector's data field is processed. The SCSI processor is paused on SCSI block boundaries only.

Microprocessor Interface

The TEC376/386 samples the BA signals during power-up reset to configure the microprocessor operating mode. Power-down (low-power) mode is controlled by the microprocessor.

The TEC376/386 connects to the Intel and Motorola microprocessors as described below:

- Direct-connect microprocessor support for Intel 80186 and 80188
- External logic for Motorola 68000 and 68300 series

Pins that support microprocessor interfaces and other chip operations are shown in figures 2 and 3.

Packaging

The TEC376 is available in a 100-pin plastic quad flat pack (PQFP), and the TEC386 is available in a 120-pin PQFP.

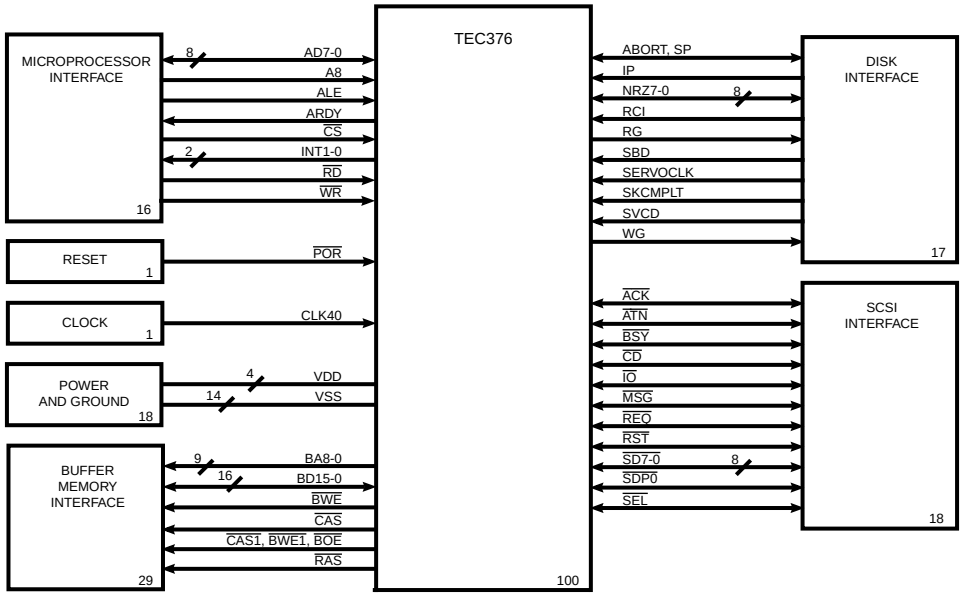


Figure 2. TEC376 Functional Signal Grouping

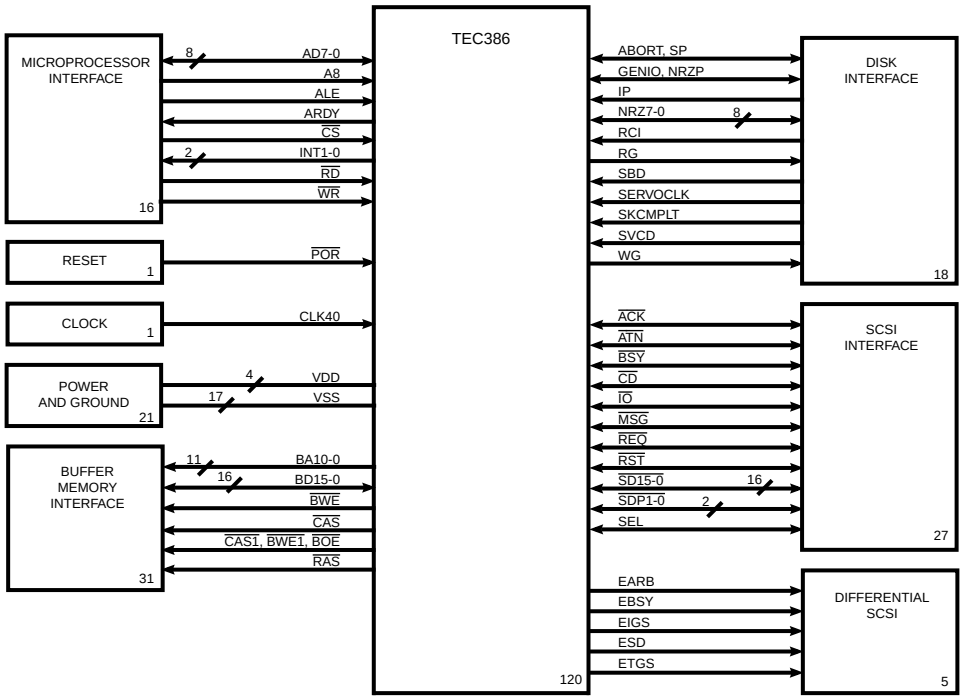


Figure 3. TEC386 Functional Signal Grouping

TEC420
Triple Embedded Controller

Features

- Compliance with ANSI SCSI configured automatically (SCAM) protocol
- Compliance with ANSI X3T10/1071D Fast-20 standard
- Wide, 16-bit Ultra SCSI synchronous data transfer rates up to 40 Mbytes/sec
- Narrow, eight-bit Ultra SCSI synchronous data transfer rates up to 20 Mbytes/sec
- Multithread automation
- Initiator and target support for automated disconnection and reconnection
- Differential support
- Disk data rate of 30 Mbytes/sec
- Enhanced, programmable Reed Solomon 144- or 192-bit ECC data field protection with on-the-fly, quadruple-burst error correction
- ID-less disk formatter providing magnetoresistive (MR) head support
- 16-bit DMA bandwidth of 70 Mbytes/sec sustained
- Table search tool to support sophisticated disk caching operations
- Data protection with buffer CRC (BCRC)
- Enhanced data streaming support
- Hardware XOR (exclusive OR) function at DMA speeds
- Logical block address (LBA) seeder and checker
- Dual TEC mode to support dual ported applications
- Programmable sequencer to automate SCSI protocol handling

Product Description

The TEC420 triple embedded controller is part of the QLogic family of high-performance, low-cost, single-chip, disk data controllers for use in host and peripheral applications. The chip is designed for use in high-performance 3.5-inch and 2.5-inch embedded SCSI disk drive designs, and provides a state-of-the-art disk formatter, a high-speed buffer controller, and Ultra SCSI synchronous transfer rates (see figure 1).

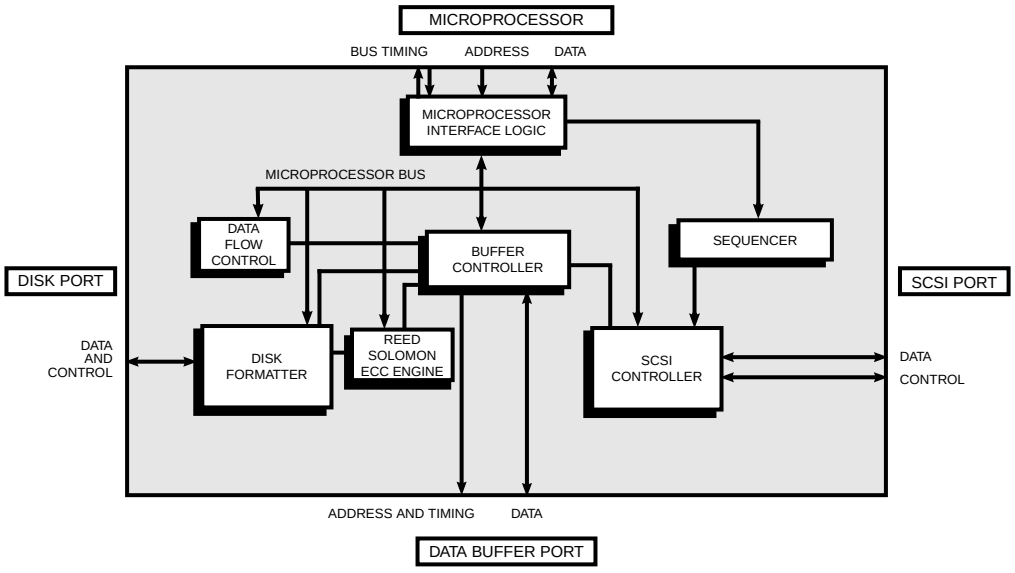


Figure 1. TEC420 Block Diagram

The TEC420 SCSI controller core provides advanced SCAM level 1 and level 2 support.

The TEC420 includes a sequencer to provide the user with a flexible, programmable means to coordinate SCSI sequences.

The TEC420 supports both single-ended SCSI and differential SCSI mode operations, operates in initiator and target roles, and supports XOR operations. The TEC420 microprocessor interface is optimized to support DMA access of buffer memory.

Product Architecture

SCSI Processor

The TEC420 SCSI processor supports the following:

- Ultra SCSI data rates of 40 Mbytes/sec
- Compliance with the ANSI X3.131-1994 SCSI-2 standard
- Compliance with the ANSI X3T10-855D SCSI-3 parallel interface (SPI) standard
- SCSI-3 message support
- Programmable active negation
- Differential support

The TEC420 SCSI bus interface provides direct, single-ended SCSI bus control. The TEC420 also provides differential SCSI bus control. The TEC420 SCSI processor consists of programmable registers and state machine sequencers that interface to the SCSI bus on one side and to a fast, buffered DMA channel on the other. A programmable sequencer provides command automation.

Sequencer

The TEC420 sequencer supports the following:

- Maximum of 20 MIPS (50-ns instruction cycle except for branch)
- 64 single-word instructions only
- 14-bit wide instructions
- Eight-bit wide data path
- 256 instruction locations
- 32 general purpose registers
- Five-level deep hardware stack
- Direct, indirect, absolute, and immediate addressing modes
- Two firmware interrupt sources: I0 and I1
- Two hardware interrupts, one with four-bit autointerrupt vector and status
- Full chip access through the microprocessor bus

The sequencer allows the user to customize SCSI sequences. A simple program sequence implements the QLogic Target Block Sequence commands. A 256-location instruction memory allows the user to customize autocommand features.

The Harvard architecture of the sequencer improves performance and flexibility by separating instruction and data memory. Its pipelined architecture overlaps instruction fetch and results storage with instruction decode and execution cycles to provide two-clock instruction execution and four-clock branch execution. The sequencer supports direct, indirect, absolute, and immediate addressing modes.

The sequencer has a 32-byte register file, a five-level deep stack, an integer ALU, and other special purpose registers. The sequencer has access to its internal registers, the SCSI FIFO, the DRAM buffer, and all registers within the TEC420. This access provides flexibility in automating the TEC420 to respond to SCSI commands.

The sequencer supports two types of interrupt schemes: firmware and hardware. The firmware interrupt allows the external microprocessor to initiate an operation within the sequencer without stopping its current operation. The firmware interrupt vector can be modified by the microprocessor while a sequencer program is running.

The hardware interrupts come directly from the SCSI module. The sequencer can be configured to deliver these interrupts to the microprocessor or to intercept these interrupts and act on them as part of command automation. Hardware interrupts handled through the sequencer are based on the values of the SCSI module interrupt and status vector inputs.

Disk Formatter

The TEC420 disk formatter supports the following:

- On-the-fly correction up to 12 bytes
- Embedded servo field skipping support
- Variable length sectors up to 5968 bytes

The disk formatter is a full-function, disk interface controller. The disk formatter structure contains a data FIFO, ECC engine, and a writable control store (WCS) state machine. Buffer controller DMA channel 0 is dedicated to the disk formatter.

The disk interface control operation occurs when the local microprocessor loads all required control information and parameter values into the WCS RAM, then issues a command. The disk formatter automatically executes the command with no further microprocessor intervention required.

The disk formatter performs all operations while fully supporting sector splits for embedded servo disk drives. Embedded servo support consists of a servo split count value from the DRAM-based table, counters, and a timer. The TEC420 can split a data field or ECC field around a servo cell.

A powerful 144- or 192-bit Reed Solomon code provides ECC protection for the data field. This code supports quadruple-burst, on-the-fly correction up to 96 bits. The TEC420 supports sectors up to 5968 bytes in length.

MR-head support is accomplished with an ID-less architecture that enhances capacity and throughput. Servo split and sector count information generated from a DRAM-based table are fetched for each servo cell on the track.

Buffer Controller

The TEC420 buffer controller supports the following:

- Maximum buffer size of 2 Mbytes
- Extended data out (EDO) DRAMs for fast burst DMA

The TEC420 buffer management is provided by a high-speed, bursting DMA controller. The buffer controller connects the buffer DRAM to the disk channel, ECC channel, and SCSI channel. The buffer controller regulates all data movement into and out of DRAM buffer memory. Each DMA channel supports DMA bursting, which maintains the optimal bandwidth. The disk and SCSI channels each have a 32-word deep FIFO. Each DMA channel has associated control, configuration, and buffer memory address registers.

The buffer controller also provides microprocessor address decoding, priority arbitration for the buffer resource, BCRC, and automatic DRAM refresh control.

The buffer controller table search tool compares 16 or 32 bits to a table of numbers, such as an LBA, to provide high-speed lookups for cache, zone, defect, and other searches required by the system.

An XOR engine running at DMA speeds generates an XOR of two data buffers to support the SCSI-3 redundant array of inexpensive disks (RAID) commands in the TEC420. RAID commands include XDRead, XDWrite, and XDParity.

To facilitate firmware debugging and to guarantee data integrity, LBA seeding is provided for all data blocks written to the disk.

Data Flow Control

Data Flow is designed to reduce data transfer time by automatically monitoring and controlling the flow of data between the disk and the SCSI channels. This is accomplished by reducing the number of interrupts that occur in a typical disk-to-SCSI data transfer. When the disk and SCSI data transfer rates are the same, both channels transfer data at the maximum rate, which prevents slipped sectors in the disk port and periods of inactivity during the data phases of a SCSI bus transfer.

Data Flow automatically prevents buffer overflow and underflow conditions by temporarily suspending (pausing) the disk formatter or SCSI processor DMA channel before the buffer becomes full or empty. The disk formatter is paused on sector boundaries. The SCSI processor is paused on SCSI block boundaries only.

Microprocessor Interface

The TEC420 samples the BA signals during power-up reset to configure the microprocessor operating mode. Power-down (low-power) mode is controlled by the microprocessor.

The TEC420 connects to the Intel and Motorola microprocessors as follows:

- Direct-connect microprocessor support for Intel 80186 and 80188
- External logic for Motorola 68000 and 68300 series

Pins that support microprocessor interfaces and other chip operations are shown in figure 2.

Packaging

The TEC420 is available in a 128-pin plastic quad flat pack (PQFP).

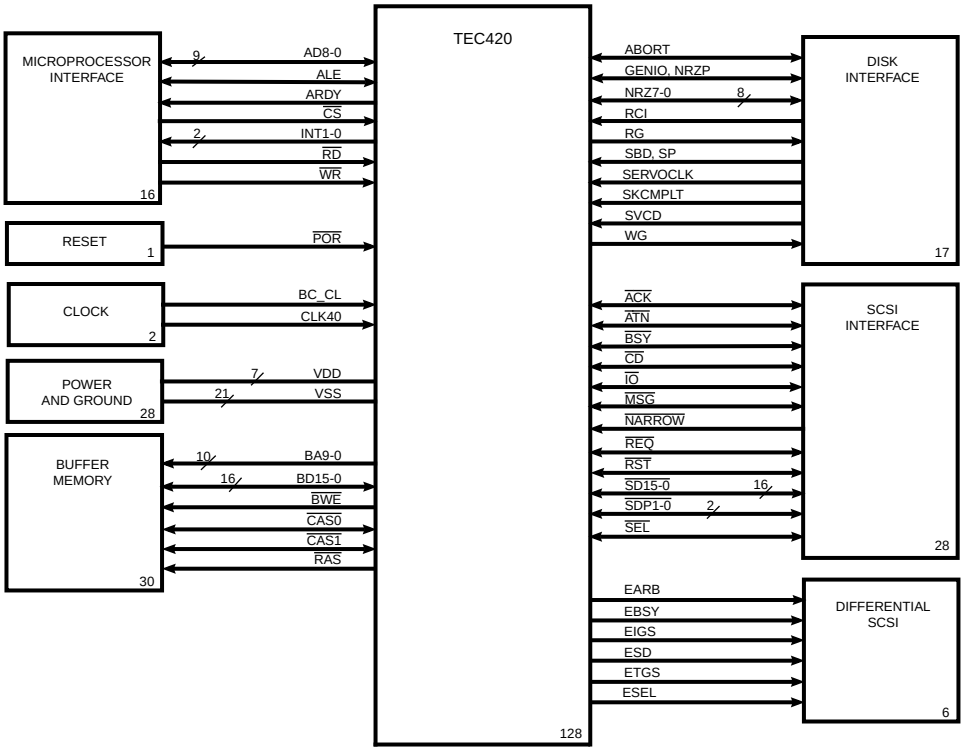


Figure 2. TEC420 Functional Signal Grouping

ATEC378
ATA Triple Embedded Controller

Features

- Register architecture similar to QLogic TEC products for fast firmware adaptation
- Power-down management, low-power operation: idle, standby, and sleep modes

Product Description

The ATEC378 is a small, low-cost, disk and host bus interface controller solution intended for next-generation, small ATA drives (see figure 1).

This single-chip, integrated circuit is essential for high-performance, data path control in ATA-compatible disk drives, which are required in PC computer systems. The ATEC378 directly connects to the host bus through a cable and adapter arrangement defined in the ATA specification (see figure 2). This bus is directly driven by the ATEC378 with high-current I/O buffers that have Schmitt trigger inputs. The chip provides a combined state-of-the-art disk formatter, buffer controller, and host ATA bus processor controller.

The ATEC378 offers high data transfer performance for both host and disk interfaces. The chip exceeds all ATA-2 and ATA-3 bus specifications for advanced PIO timing modes 3 and 4 and meets specifications for multiword DMA timing modes 1, 2, and 3, and ultra DMA transfer modes 0, 1, and 2. The ATEC378 provides an eight-bit parallel NRZ disk interface that supports disk data rates of up to 25 Mbytes/sec.

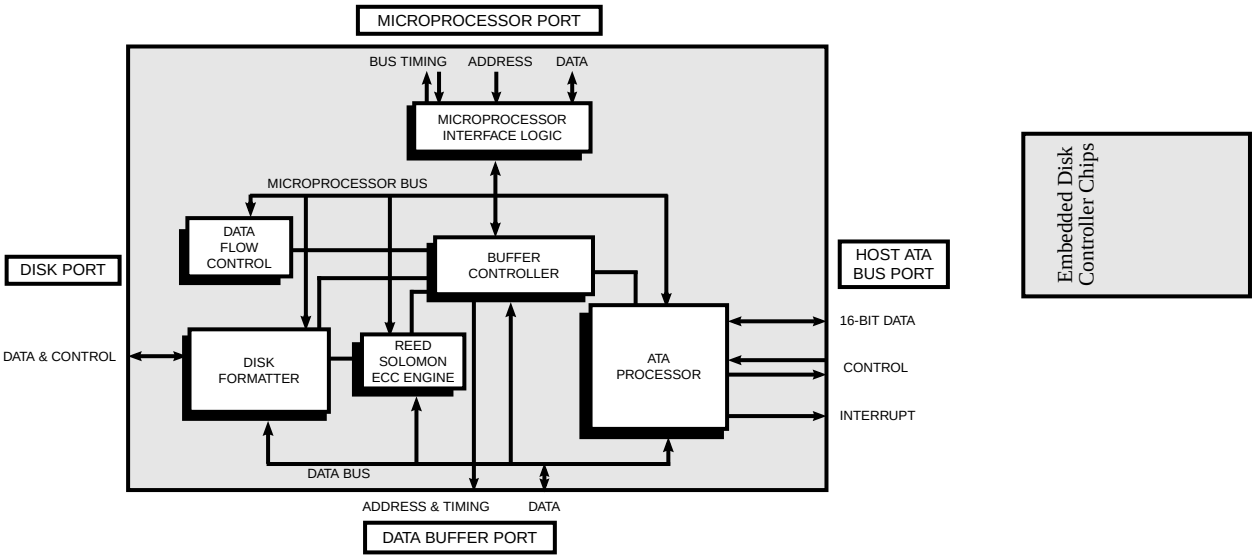


Figure 1. ATEC378 Block Diagram

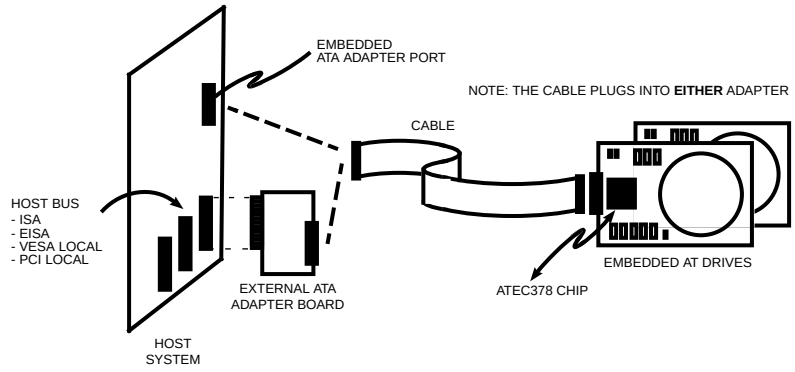


Figure 2. ATEC378 Chip Within a Host System

Interfaces

The ATEC378 interfaces consist of the microprocessor interface, the buffer controller interface, the DMA interface, the disk formatter interface, and the host ATA bus interface.

The ATEC378 pins that support these and other chip interfaces are shown in figure 3 and described in the following sections.

Microprocessor

The ATEC378 microprocessor supports the following:

- Intel 80188 and 80186 multiplexed bus architecture direct connection; minimal external logic requirement for Motorola 68000
- Zero wait state microprocessor I/O timing for all register read operations

Buffer Controller

The ATEC378 buffer controller supports the following:

- 50 Mbytes/sec peak bandwidth
- 16-bit data protection with buffer cyclical redundancy check (BCRC) for block-oriented data and protection against miscorrecting data
- Enhanced Data Flow and greater system efficiency using hysteresis (ensures that a programmable amount of data is available in the buffer before initiating a data transfer).
- Logical block address (LBA) seeding and checking for firmware debugging, data integrity, and mispositioning protection
- 16-bit DRAM data buffer
- Enhanced microprocessor data buffer access
- Support for fast page mode DRAMs for fast burst DMA
- Autoreload address pointers for circular buffers
- Multiple DMA ports and automatic DRAM refresh

Disk Formatter

The ATEC378 disk formatter supports the following:

- Enhanced, programmable Reed Solomon 144- or 192-bit ECC data field protection with on-the-fly, quadruple-burst error correction with error logging
- DRAM-based, ID-less disk formatter that provides magnetoresistive (MR)-head support
- Disk data rate of 25 Mbytes/sec, eight-bit parallel
- Embedded servo field skipping support
- Single-sector and multisector operations
- Writable control store, 31 words by 32 bits wide, for flexible operation

Host ATA Bus

The ATEC378 host ATA bus supports the following:

- Conformity with ANSI ATA-2 and ATA-3 standards
- Conformity with ATA/ATAPI-4 revision 8 draft
- ATA command and control block (WD1003 task file registers emulation) with local (snapshot) register set for advanced performance extensions
- Automated host command processing on all write and certain read commands
- Host ATA bus data transfer timing rates:
  - ❒ Up to 16.6 Mbytes/sec PIO
  - ❒ 16.67 Mbytes/sec DMA
  - ❒ 33 Mbytes/sec ultra DMA
- ATAPI support
- Hardware that handles full data streaming on read/write multiple commands

Packaging

The ATEC378 is available in a 128-pin plastic quad flat pack (PQFP).

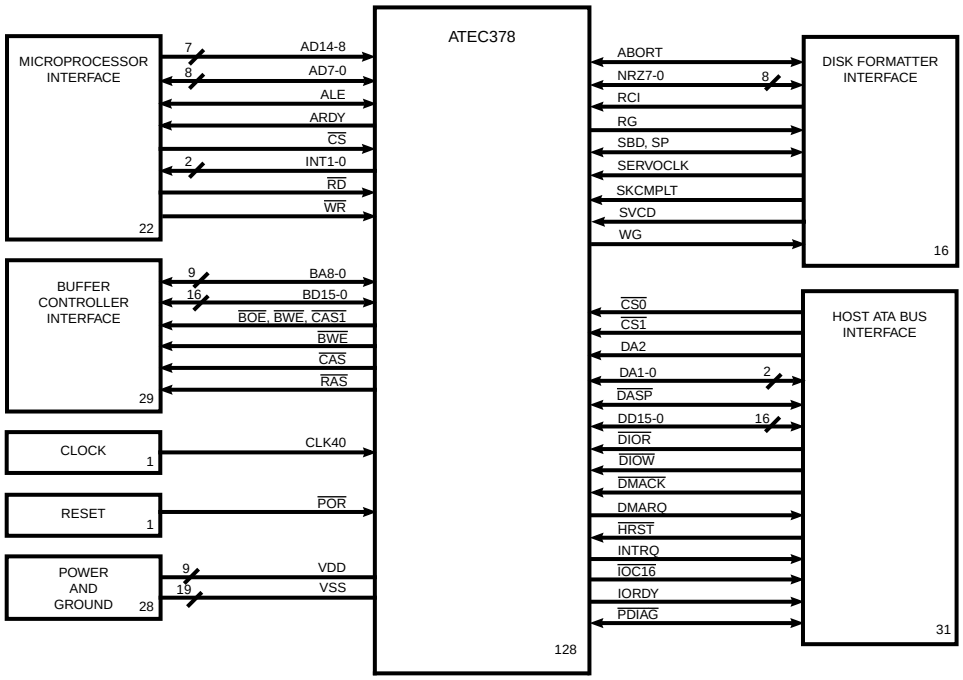


Figure 3. ATEC378 Functional Signal Grouping

FTEC440
Triple Embedded Controller for Fibre Channel

Features

- Dual Port Fibre Channel Arbitrated Loop (FC-AL) Interface Manager
- 100 Mbytes/sec data transfer rate
- On-chip 8B/10B encode and decode
- 10-bit interface to external transceivers
- Disk data rate of 33 Mbytes/sec
- Enhanced, programmable Reed Solomon 192-bit or 320-bit ECC data field protection with on-the-fly, five-burst error correction
- ID-less disk formatter providing magnetoresistive (MR)-head support
- On-the-fly correction up to 20 bytes
- Embedded servo field skipping support
- Variable length sectors up to 7840 bytes
- 125 Mbytes/sec total, sustained 32-bit DMA bandwidth
- Table search tool to support sophisticated disk caching operations
- Data protection with buffer CRC (BCRC)
- Enhanced data streaming support
- Intelligent sequencer to automate Fibre Channel operations

Product Description

The FTEC440 triple embedded controller is part of the QLogic family of high-performance, low-cost, single-chip, disk data controllers. It provides a state-of-the-art disk formatter and a high-speed buffer controller. The FTEC440 is designed for use in high-performance, 3.5- and 2.5-inch embedded Fibre Channel disk drive designs. Figure 1 shows the block diagram for the FTEC440.

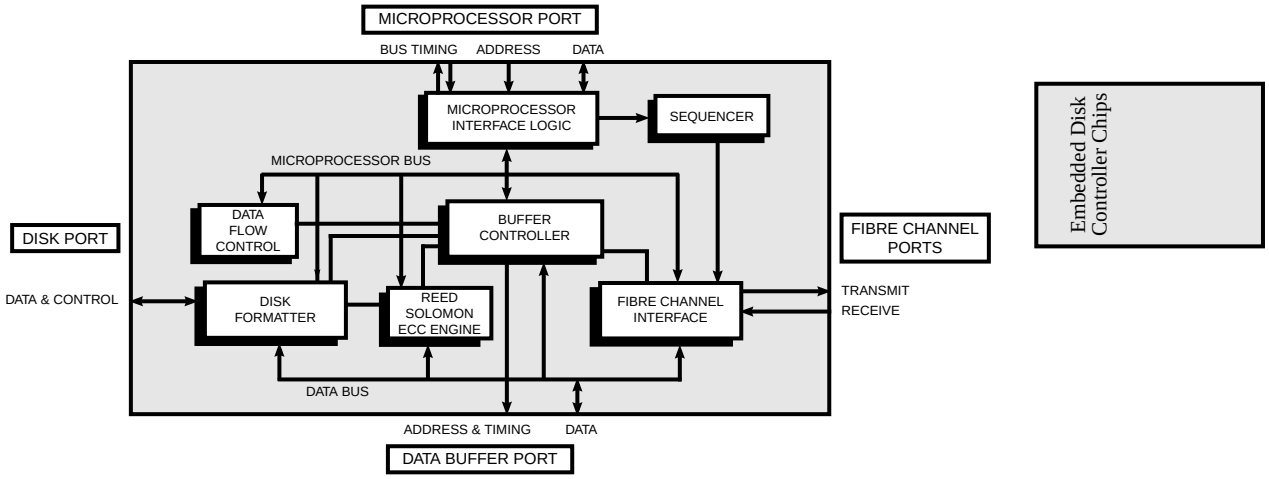


Figure 1. FTEC440 Block Diagram

Product Architecture

Fibre Channel Interface Manager

The Fibre Channel Interface Manager (FCIM) implements the FC-AL protocol, including the FC-1 and FC-2 layers of the signaling interface. The FC-0 layer is implemented for each port by external serial link transmitter and receiver modules that connect to the FCIM through two 10-bit interfaces. The FCIM includes an 8B/10B encoder and decoder, an elasticity buffer for clock skew management, and an FC-AL state machine. The FCIM transmits and receives at the full Fibre Channel rate of 106.25 Mbytes/sec. As specified in the FC-AL protocol, the FCIM uses the alternate

buffer-to-buffer credit model to pace frames. The FCIM receive path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer. The transmit path transmits frames from the frame buffer to the Fibre Channel. The FCIM automatically handles frame delimiters and frame control.

Sequencer

The FTEC440 sequencer supports the following:

- Maximum of 20 MIPS (50-ns instruction cycle except for branch)
- 64 single-word instructions only
- 16-bit wide instructions
- Eight-bit wide data path
- 1024 instruction locations
- 32 general purpose registers (16 are dual port to act as mailboxes)
- Five-level deep hardware stack
- Direct, indirect, absolute, and immediate addressing modes
- Two firmware interrupt sources: I0 and I1
- Two hardware interrupts, one with four-bit autointerrupt vector and status
- Full chip access through the microprocessor bus

The sequencer allows the user to automate the FC-AL and SCSI protocol.

The Harvard architecture of the sequencer improves performance and flexibility by separating instruction and data memory. Its pipelined architecture overlaps instruction fetch and results storage with instruction decode and execution cycles to provide two-clock instruction execution and four-clock branch execution. The sequencer supports direct, indirect, absolute, and immediate addressing modes.

The sequencer has a 32-byte register file, a five-level deep stack, an integer ALU, and other special purpose registers. The sequencer has access to its internal registers, the FC-AL command FIFO, the DRAM buffer, and all registers within the FTEC440. This access provides flexibility in automating the FTEC440 to respond to SCSI commands.

The sequencer supports two types of interrupt schemes: firmware and hardware. The firmware interrupt allows the external microprocessor to initiate an operation within the sequencer without stopping its current operation. The firmware interrupt vector can be modified by the microprocessor while a sequencer program is running.

The hardware interrupts come directly from the Fibre Channel module. The sequencer can be configured to deliver these interrupts to the microprocessor or to intercept these interrupts and act on them as part of command automation. Hardware interrupts handled through the sequencer are based on the values of the SCSI module interrupt and status vector inputs.

Disk Formatter

The disk formatter is a full-function, disk interface controller. The disk formatter structure contains a data FIFO, ECC engine, and a writable control store (WCS) state machine.

The disk interface control operation occurs when the local microprocessor loads all required control information and parameter values into the WCS RAM, then issues a command. The disk formatter automatically executes the command with no further microprocessor intervention required.

The disk formatter performs all operations while fully supporting sector splits for embedded servo disk drives. Embedded servo support consists of a servo split count value from the DRAM-based table, counters, and a timer. The FTEC440 has the capability to split a data field or ECC field around a servo cell.

A powerful 192- or 320-bit Reed Solomon code provides ECC protection for the data field. This code supports five-burst, on-the-fly correction up to 160 bits. With error logging, the FTEC440 supports up to 7840 byte sectors.

MR-head support is accomplished with ID-less architecture that enhances capacity and throughput. IDs and sector pulses generated from a DRAM-based table are fetched for each servo cell on the track.

Buffer Controller

The FTEC440 buffer controller supports the following:

- Maximum buffer size of 4 Mbytes
- High-speed buffer memory initialization and verification to reduce power on initializations
- Synchronous DRAM (SDRAM)

FTEC440 buffer management is provided by a four-channel, high-speed, bursting DMA controller. The buffer controller provides the connection between the buffer DRAM and the disk channel, ECC channel, Fibre Channel, and the microprocessor bus. The buffer controller regulates all data movement into and out of DRAM buffer memory. Each DMA channel supports DMA bursting, which allows the optimal bandwidth to be maintained. Each DMA channel has associated control, configuration, and buffer memory address registers.

The buffer controller also provides microprocessor address decoding, priority arbitration for the buffer resource, BCRC, and automatic DRAM refresh control.

The buffer controller table search tool compares 16 or 32 bits to a table of numbers, such as an LBA, to provide high-speed cache lookup, zone lookup, defect lookup, and other searches the system requires.

To facilitate firmware debugging and to guarantee data integrity, LBA seeding is provided for all data blocks written to the disk.

Data Flow Control

Data Flow is designed to reduce data transfer time by automatically monitoring and controlling the flow of data between the disk and the Fibre Channel ports. Automatic control of data flow between these channels reduces the number of interrupts that occur in a typical disk-to-Fibre Channel data transfer.

Data Flow automatically prevents buffer overflow and underflow conditions by temporarily suspending (pausing) the disk formatter or Fibre Channel DMA channel before the buffer becomes full or empty. To stop the disk formatter on sector boundaries and not in the middle of a data field, the disk formatter is paused by suspending the start of any disk sequence after a sector's data field has been processed. The Fibre Channel processor is paused on Fibre Channel frame boundaries only.

Microprocessor Interface

The FTEC440 samples the DRAM buffer address signals during power-up reset to configure the microprocessor operating mode. Power-down (low-power) mode is controlled by the microprocessor.

The FTEC440 connects to the microprocessors as described below:

- Direct-connect microprocessor support for Intel 80188 and 80186
- Microprocessor support with external logic for Motorola 68000 and 68300 series

The 68300 and 68000 microprocessor series provide separate, nonmultiplexed address and data buses.

FTEC440 pins that support microprocessor interfaces and other chip operations are shown in figure 2.

Packaging

The FTEC440 is available in a 225-pin ball grid array (BGA) package.

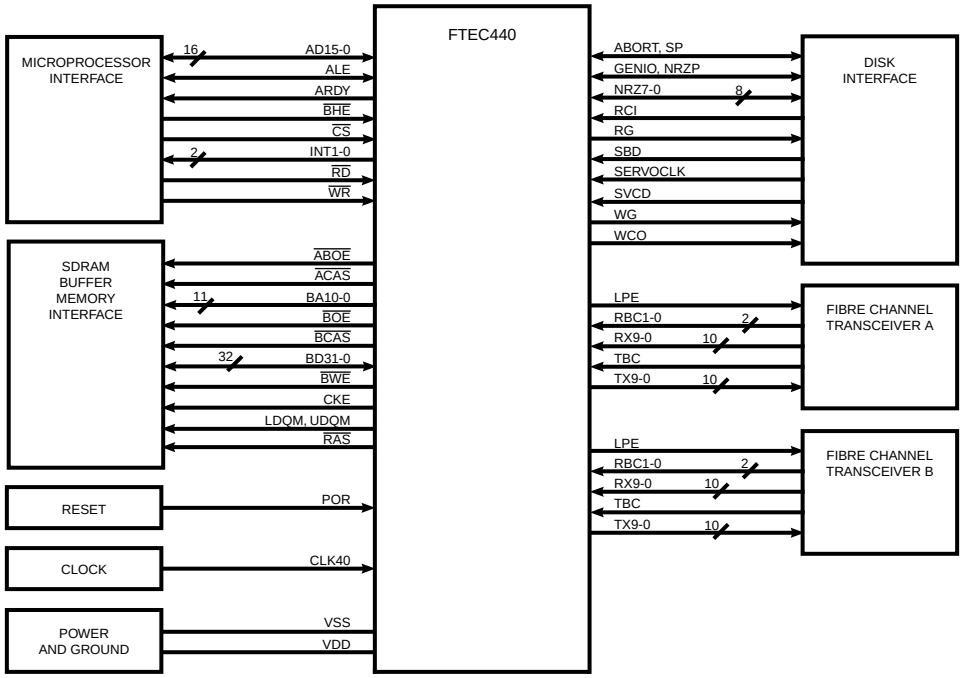


Figure 2. FTEC440 Functional Signal Grouping

ISP1000/1000U
Intelligent SCSI Processor

Features

- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI X3T10/1071D Fast-20 standard (ISP1000U)
- Supports fast and wide SCSI transfers (ISP1000)
- Supports fast, wide, and Ultra SCSI (Fast-20) transfers (ISP1000U)
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control block level from the host memory
- No host intervention to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads

Product Description

The ISP1000/1000U is a single-chip, highly integrated, bus master, SCSI I/O processor for use in SCSI applications. It interfaces the Sun Microsystems SBus to an ANSI fast and wide SCSI bus and contains an onboard RISC processor. The ISP1000/1000U is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP1000/1000U block diagram is illustrated in figure 1.

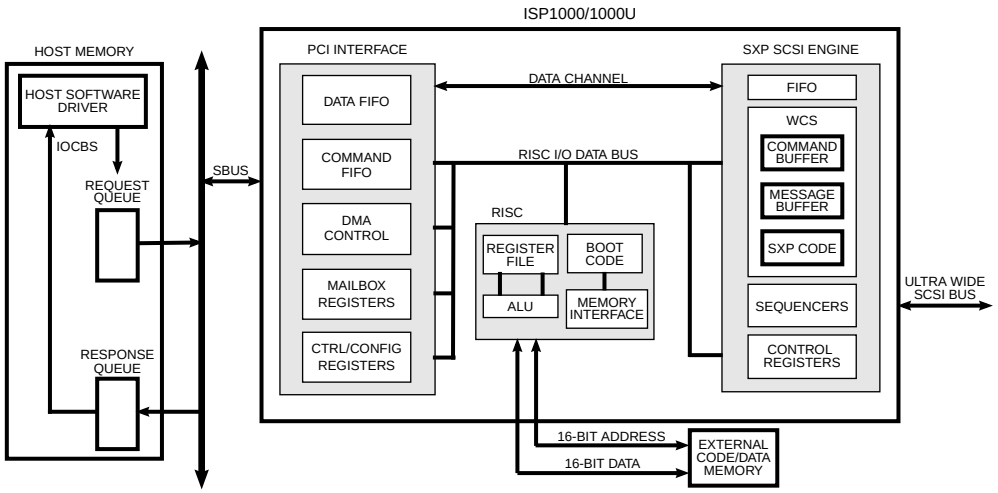


Figure 1. ISP1000/1000U Block Diagram

ISP Initiator Firmware

The ISP firmware implements a cooperative multitasking host adapter that provides the host with complete SCSI command and data transport capabilities, thus freeing the host from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host: the command interface and the SCSI transport interface. The single-threaded command interface is intended for debugging, configuration, and error recovery. The multithreaded SCSI transport interface maximizes use of the SCSI and host buses, and ISP1000/1000U processing.

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1000/1000U incorporates a high-speed, proprietary RISC processor; an intelligent

SCSI bus controller (SCSI executive processor [SXP]); and a host bus dual-channel, first-party DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP1000/1000U RISC interface requires external program data memory.

The complete I/O subsystem solution using the ISP1000/1000U and associated supporting memory devices is shown in figure 2.

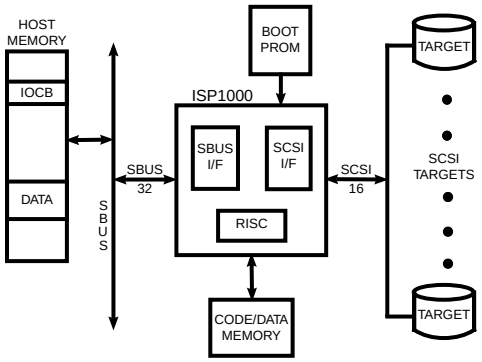


Figure 2. I/O Subsystem Design Using the ISP1000/1000U

Interfaces

The ISP1000/1000U interfaces consist of the RISC processor, SBus interface, SCSI executive processor, and FCODE boot PROM. Pins that support these interfaces and other chip operations are shown in figure 3 and described in the following sections.

RISC Processor

The ISP1000/1000U RISC processor supports the following:

- High-speed instruction execution
- Flexible external memory support
- Programmable cycle time for external memory access
- Internal 16-bit wide data paths

One of the major features of the ISP1000/1000U is its ability to handle complete I/O transactions with no intervention from the host. This is accomplished with an onboard RISC processor. The ISP1000/1000U RISC processor controls the chip interfaces; executes simultaneous, multiple I/O control blocks (IOCB); and maintains the required thread information for each transfer.

The RISC memory interface is a 16-bit data path that provides access to RISC instructions, data, and I/O transactions. The RISC processor can access internal ROM as well as RAM and ROM external to the ISP1000/1000U. The first 4K words of address space are allocated for internal memory. The remaining 60K words of address space are allocated for external memory.

SBus Interface

The ISP1000/1000U SBus interface supports the following:

- Address and control signals to operate as a 32-bit bus master DMA device
- Control signals to operate in 16-bit slave mode
- DMA FIFO management and data alignment, data assembly, and data disassembly
- Registers for bus ID, configuration, and DMA functions

The ISP1000/1000U interfaces directly with the Sun Microsystems SBus and operates as a 32-bit, direct virtual memory access (DVMA) master. This operation (32-bit DVMA) is accomplished through an SBus interface unit (SBIU) containing an onboard DMA controller. The SBIU generates and samples SBus control signals, generates host memory addresses, and facilitates data transfers between host memory and the onboard DMA FIFO. It also allows the host to access the ISP1000/1000U internal registers and communicate with the onboard RISC processor through the SBus slave mode operation.

The ISP1000/1000U onboard DMA controller consists of two independent DMA channels that initiate transactions on the SBus and transfer data between the host memory and the DMA FIFO. The two DMA channels are the command DMA channel and the data DMA channel. The command DMA channel has limited capability and is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory. The data DMA channel transfers data between the host memory and the SCSI bus.

The SBIU internally arbitrates between the two channels and alternately services them. Each DMA channel has a set of registers that are programmed for transfers by the RISC processor.

SCSI Executive Processor

The ISP1000/1000U SXP supports the following:

- SCSI A and P cable ready
- Asynchronous SCSI transfers up to 12 Mbytes/sec

- SCSI synchronous transfer rates:
  - ❒ 20 Mbytes/sec
  - ❒ 40 Mbytes/sec (Ultra SCSI; ISP1000U)
- Programmable SCSI processor
- On-chip data storage
- 32-bit, configurable transfer counter
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Diagnostic support

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

Packaging

The ISP1000/1000U is available in a 208-pin plastic quad flat pack (PQFP).

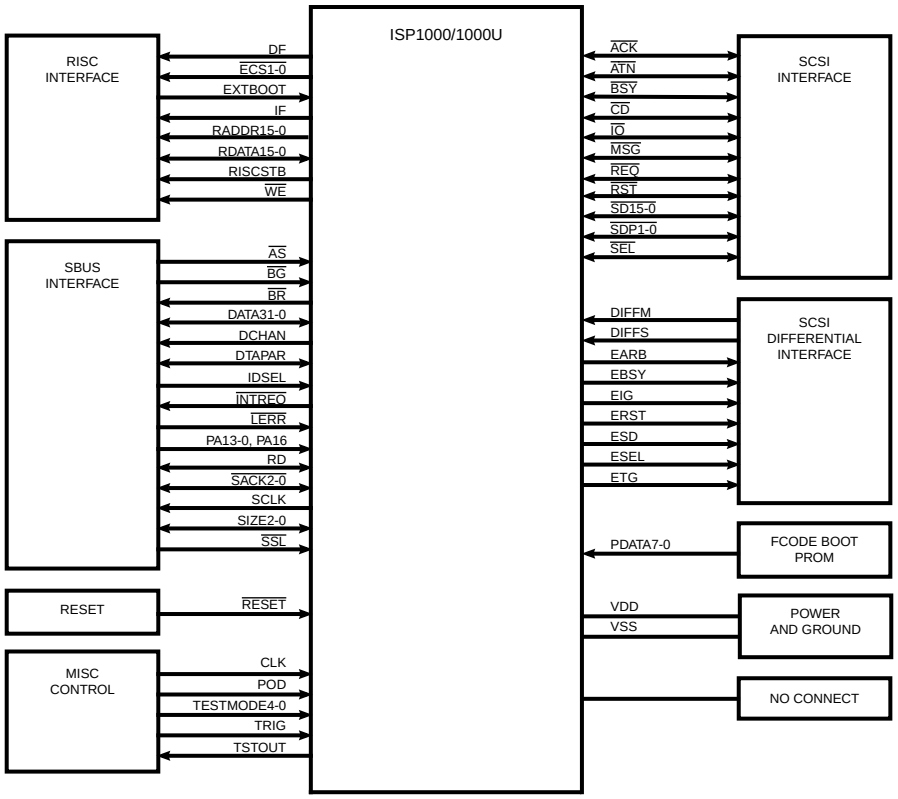


Figure 3. ISP1000/1000U Functional Signal Grouping

ISP1040B
Intelligent SCSI Processor

Features

- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI X3T10/1071D Fast-20 standard
- Onboard RISC processor to execute operations at the I/O control block level from the host memory
- Supports fast, wide, and Ultra (Fast-20) SCSI data transfer rates
- SCSI initiator and target modes of operation
- 32-bit, intelligent bus master, DMA PCI bus interface
- SCSI operations executed from start to finish without host intervention
- Simultaneous, multiple logical threads
- JTAG boundary scan support

Product Description

The ISP1040B is a single-chip, highly integrated, bus master, SCSI I/O processor for use in SCSI initiator-type applications. The device interfaces the PCI bus to a wide, Ultra SCSI bus and contains an onboard RISC processor. The ISP1040B is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from initiation to completion without host CPU intervention. The ISP1040B block diagram is illustrated in figure 1.

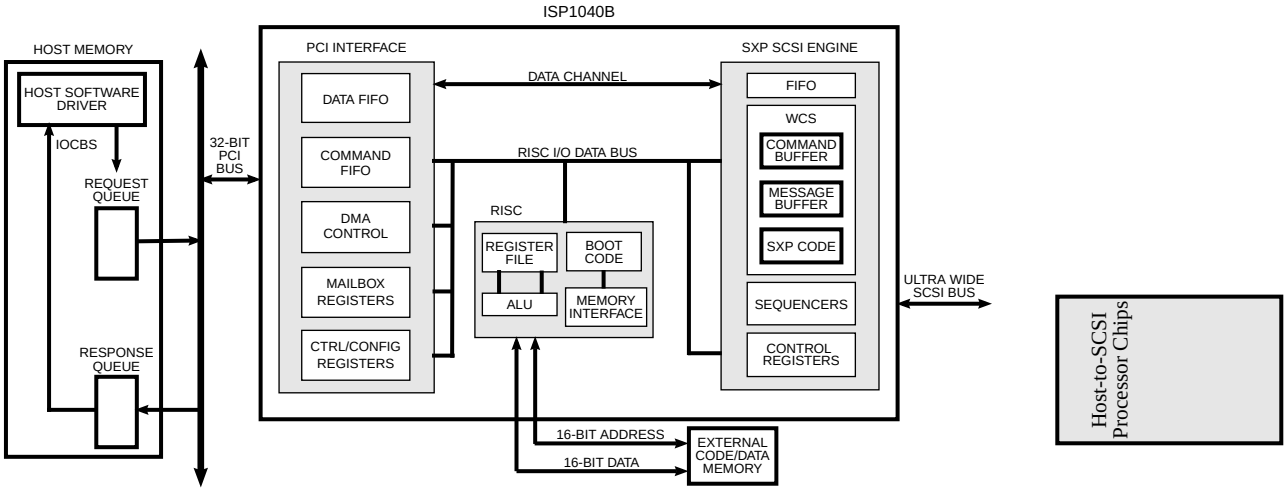


Figure 1. ISP1040B Block Diagram

ISP Initiator and Target Firmware

The ISP1040B firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The ISP1040B firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery. The multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP1040B can switch between initiator and target modes.

I/O Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1040B incorporates a high-speed, proprietary RISC processor; an intelligent SCSI bus controller (SCSI executive processor [SXP]); and a host bus, dual-channel DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under control of the onboard RISC processor for maximum system performance. The ISP1040B RISC interface requires external program data memory.

The complete I/O subsystem solution using the ISP1040B and associated supporting memory devices is shown in figure 2.

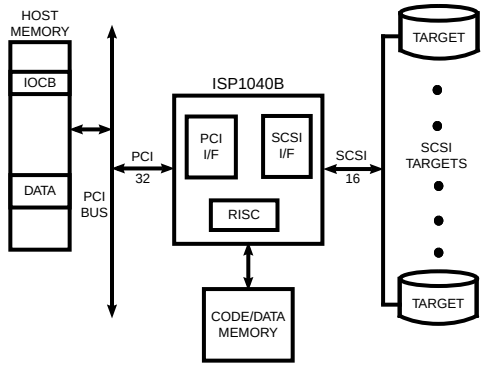


Figure 2. I/O Subsystem Design Using the ISP1040B

Interfaces

The ISP1040B supports the following interfaces:

- PCI bus
- RISC processor
- SCSI executive processor

Pins that support these interfaces and other chip operations are shown in figure 3.

PCI Bus Interface

The ISP1040B PCI bus interface supports the following:

- 128-byte data DMA FIFO and 64-byte command DMA FIFO with threshold control
- 16-bit target mode
- DMA FIFO management, data alignment, data assembly, and data disassembly
- *PCI Local Bus Specification* revision 2.1 compliant
- Support for subsystem ID and subsystem vendor ID
- Dual voltage (3.3V and 5.0V) PCI I/O buffers
- Flash ROM support

The ISP1040B interfaces directly to the PCI local bus and operates as a 32-bit DMA master. This function is accomplished through the PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI bus control signals, generates host memory addresses, and facilitates data transfers between host memory and the onboard DMA FIFO. The PBIU also allows the host to access the ISP1040B internal registers and communicate with the onboard RISC processor through the PCI bus target mode operation.

The ISP1040B onboard DMA controller consists of two independent DMA channels that initiate transactions on the PCI bus and transfer data between the memory and DMA FIFO. The two DMA channels are the command DMA channel and the data DMA channel. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channel transfers data between the SCSI bus and the PCI bus.

The PBIU internally arbitrates between the data DMA channel and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

RISC Processor Interface

The ISP1040B RISC processor interface supports the following:

- Programmable cycle time for external memory access
- Internal 16-bit wide data paths
- Execution of multiple I/O control blocks from the host memory
- Management of onboard host bus DMA controller and SCSI bus controller
- Reduced host intervention and interrupt overhead
- Capacity to generate one interrupt per I/O operation

The onboard RISC processor enables the ISP1040B to handle complete I/O transactions with no intervention from the host. The ISP1040B RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCBs); and maintains the required thread information for each transfer.

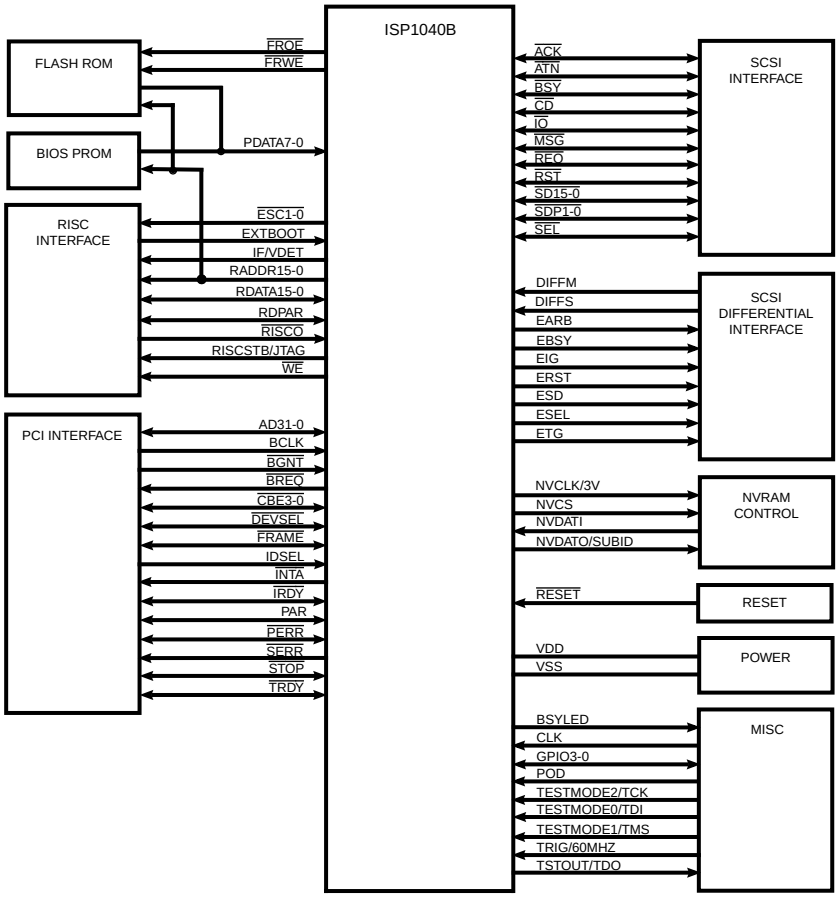


Figure 3. ISP1040B Functional Signal Grouping

SCSI Executive Processor Interface

The ISP1040B SXP interface supports the following:

- SCAM level 1 and level 2 support
  - 32-byte FIFO with parity pass-through option
  - Command, status, message in, and message out buffers
  - Device information storage area
- SCSI synchronous transfer rates of 40 Mbytes/sec (requires 60-MHz clock)
- SCSI asynchronous transfer rate of 12 Mbytes/sec
- Programmable SCSI processor
  - Specialized instruction set with 16-bit microword
  - 384-bit by 16-bit internal control store RAM
- Diagnostic support

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

Packaging

The ISP1040B is available in a 208-pin plastic quad flat pack (PQFP).

ISP1080
Intelligent SCSI Processor

Features

- Compliance with ANSI draft Ultra-2 (Fast-40) Low Voltage Differential Signaling (LVDS)
- 64-bit PCI host bus interface, compliant with *PCI Local Bus Specification* revision 2.1. Supports 3.3 volt or 5.0 volt PCI host bus.
- Up to 80 Mbytes/sec parallel SCSI transfer rates
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control-block level from the host memory
- No host intervention required to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads

Product Description

The ISP1080 adds Ultra-2 (Fast-40) SCSI support to the expanding functionality of the ISP. The product is a single-chip, highly integrated bus master, SCSI I/O processor for SCSI initiator and target applications. This device interfaces the PCI bus to an ANSI Ultra-2 (Fast-40) SCSI bus and contains an onboard RISC processor. The product is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP1080 is host-software compatible with the QLogic ISP1040B. The ISP1080 block diagram is illustrated in figure 1.

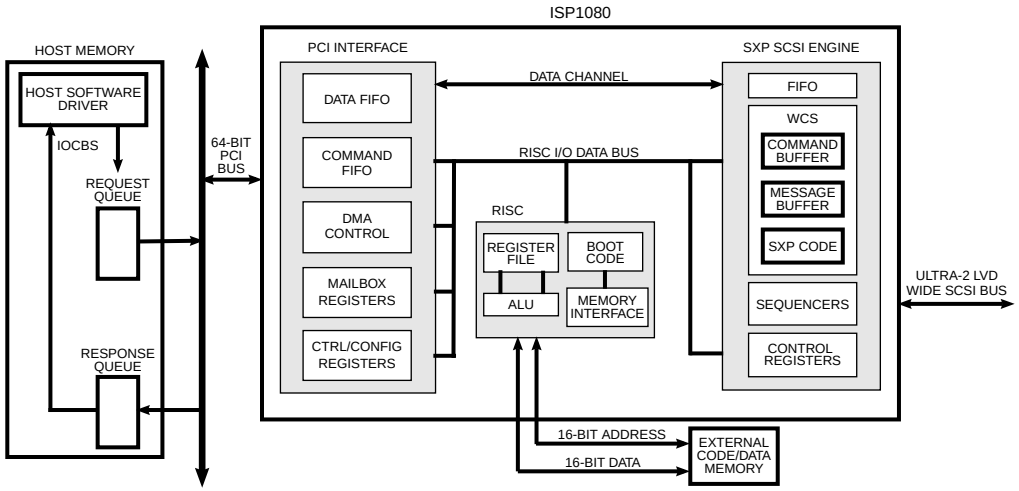


Figure 1. ISP1080 Block Diagram

ISP Initiator and Target Firmware

The ISP1080 firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery, while the multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP1080 can switch between initiator and target modes.

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1080 incorporates a high-speed proprietary RISC processor; an intelligent

SCSI bus controller (SCSI executive processor [SXP]); and a host bus, dual-channel, first-party DMA controller. The SCSI bus controller and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP1080 RISC interface requires external program data memory.

The complete I/O subsystem solution including the ISP1080 and associated supporting memory devices is shown in figure 2.

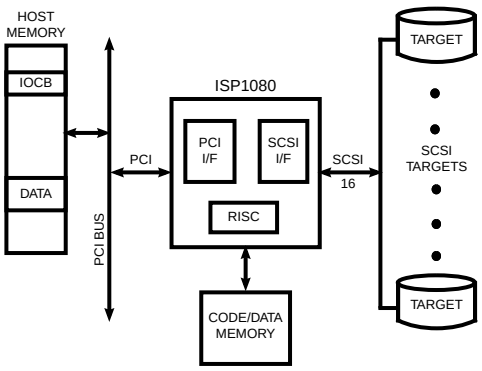


Figure 2. I/O Subsystem Design Using the ISP1080

Interfaces

The ISP1080 interfaces consist of the PCI bus interface, SCSI interface, RISC interface, BIOS PROM interface, and NVRAM interface. Pins that support these interfaces and other chip operations are shown in figure 3.

PCI Interface

The ISP1080 PCI interface supports the following:

- 64-bit (address and data), intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers
- Dual-channel DMA controller
- Data DMA FIFO and command DMA FIFO with threshold control
- 16-bit slave mode for communication with host
- Boundary alignment and aligned transfers
- Pipelined DMA registers for efficient scatter and gather operations
- 24-bit transfer counter for I/O transfer lengths up to 16 Mbytes (DMA)
- Bus ID and configuration registers
- Support for BIOS PROM
- Support for cache commands

The ISP1080 interfaces directly to the PCI bus and operates as a 64-bit DMA bus master. This operation is accomplished through a PCI bus interface unit (PBIU) that contains an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard DMA FIFO. It also allows the host to access the ISP1080 internal registers and communicate with the onboard RISC processor through the PCI target mode operation.

The ISP1080 onboard DMA controller consists of two independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and DMA FIFO. The two DMA channels are the command DMA channel and the data DMA channel. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channel transfers data between the SCSI bus and the PCI bus.

The PBIU internally arbitrates between the data DMA channel and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

SCSI Executive Processor

The ISP1080 SXP supports the following:

- SCSI A and P cable ready
- Ultra-2 (Fast-40) SCSI synchronous data transfer rates of up to 80 Mbytes/sec
- Asynchronous SCSI data transfer rates up to 12 Mbytes/sec
- Programmable SCSI processor
- 32-bit, configurable SCSI transfer counter
- On-chip, LVDS SCSI transceivers
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

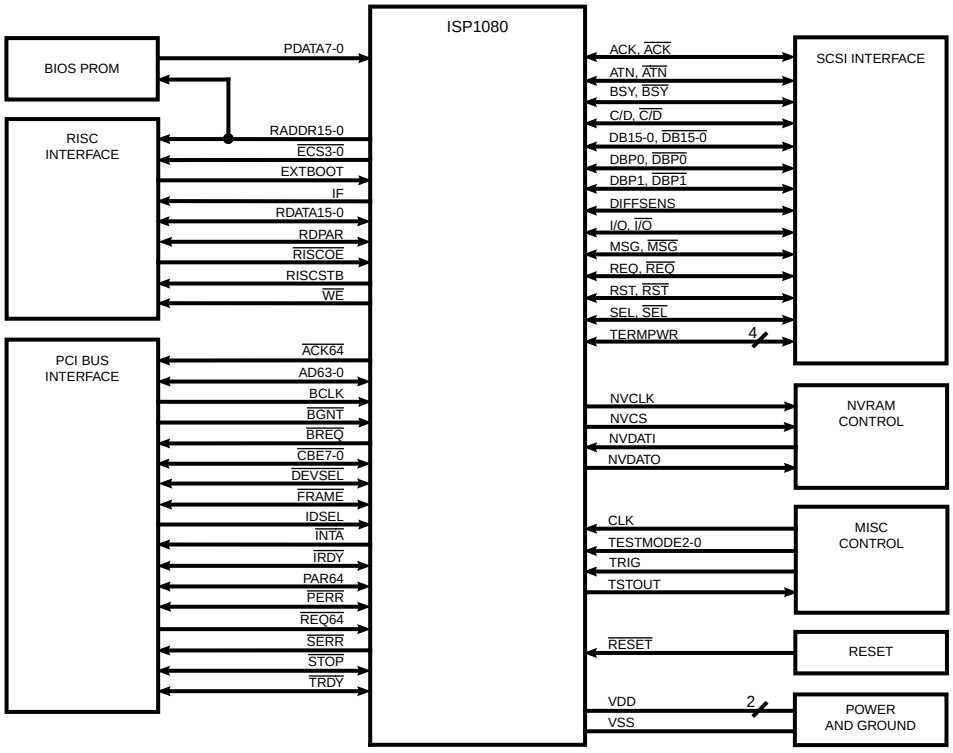


Figure 3. ISP1080 Functional Signal Grouping

RISC Processor

The ISP1080 RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

The onboard RISC processor enables the ISP1080 to handle complete I/O transactions with no intervention from the host. The ISP1080 RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCB); and maintains the required thread information for each transfer.

Packaging

The ISP1080 is available in a 352-pin ball grid array (BGA) package.

ISP1240
Intelligent, Dual SCSI Processor

Features

- 64-bit PCI host bus interface, compliant with *PCI Local Bus Specification* revision 2.1
- Compliance with ANSI Fast-20 standard X3T10/1071D
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Supports fast, wide, and Ultra (Fast-20) SCSI data transfer rates
- Two concurrently operating wide, Ultra SCSI channels
- Supports single-ended and differential SCSI
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control-block level from the host memory
- SCSI operations executed from start to finish without host intervention
- Simultaneous, multiple logical threads

Product Description

The ISP1240 is the latest addition to the QLogic ISP family. The chip adds dual channel, Ultra SCSI support to the expanding functionality of the ISP. The ISP1240 is a single-chip, highly integrated, bus master, dual-channel SCSI I/O processor for SCSI initiator and target applications. This device interfaces the 64-bit PCI bus to two Ultra SCSI buses and contains an onboard RISC processor. The ISP1240 is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers simultaneously on two SCSI channels from start to finish without host intervention. The ISP1240 is host-software compatible with the QLogic single channel ISP1040, requiring only a minor input/output control block (IOCB) change to select the additional channel. The ISP1240 block diagram is illustrated in figure 1.

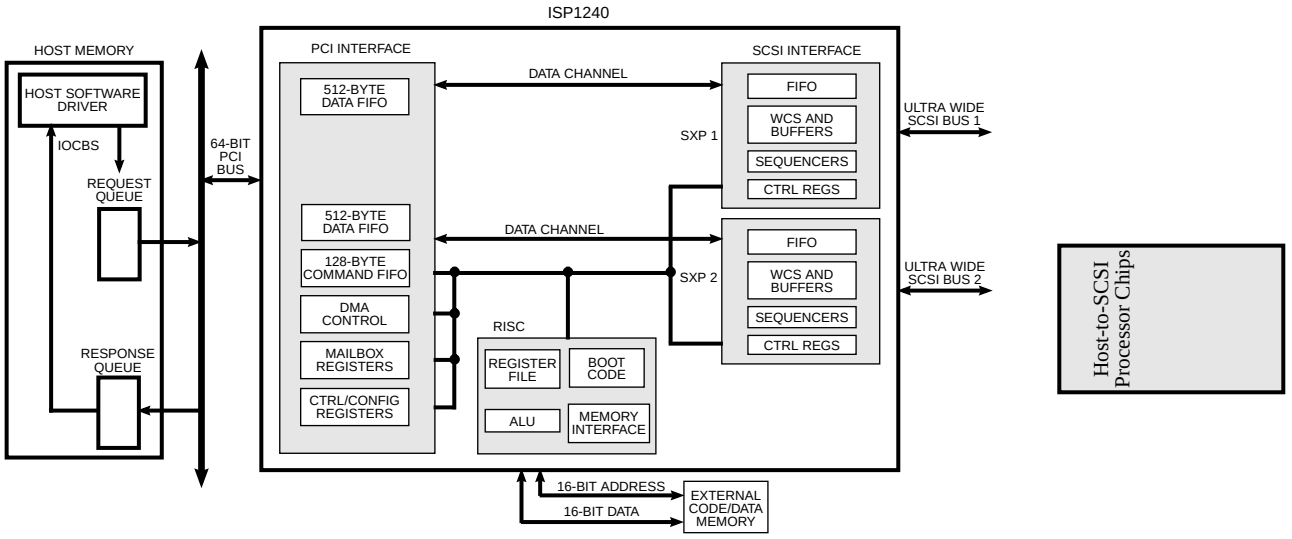


Figure 1. ISP1240 Block Diagram

ISP Initiator and Target Firmware

The ISP1240 firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery. The multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP1240 can switch between initiator and target modes.

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1240 incorporates a high-speed, proprietary RISC processor; two intelligent SCSI bus controllers (SCSI executive processor [SXP]); and a host bus, three-channel, first-party DMA controller. The SCSI bus controllers and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP1240 RISC interface requires external program data memory.

The complete I/O subsystem solution using the ISP1240 and associated supporting memory devices is shown in figure 2.

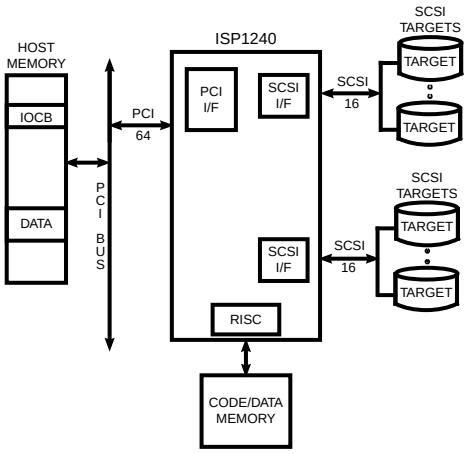


Figure 2. I/O Subsystem Design Using the ISP1240

Interfaces

The ISP1240 interfaces consist of the 64-bit PCI bus interface, two SCSI interfaces, and the RISC interface. Pins that support these interfaces and other chip operations are shown in figure 3.

PCI Interface

The ISP1240 PCI interface supports the following:

- 64-bit, intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers
- 64-bit host memory addressing (dual address cycle)
- Backward compatible to 32-bit PCI
- Three-channel DMA controller
- 512-byte data DMA FIFO per channel and 128-byte command DMA FIFO with threshold control
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter/gather operations
- 24-bit transfer counter for I/O transfer length of up to 16 Mbytes (DMA)
- Bus ID and configuration registers
- Support for BIOS PROM
- Support for cache commands
- 3.3V and 5.0V tolerant PCI pads

The ISP1240 is designed to interface directly to the PCI bus and operate as a 64-bit, DMA bus master. This operation is accomplished through a PCI bus interface unit (PBIU) that contains an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard DMA FIFO. It also allows the host to access the ISP1240 internal registers and communicate with the onboard RISC processor through the PCI target mode operation.

The ISP1240 onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and DMA FIFO. The three DMA channels consist of the command DMA channel and two data DMA channels. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channels transfer data between two SCSI buses and the PCI bus.

The PBIU internally arbitrates between the data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

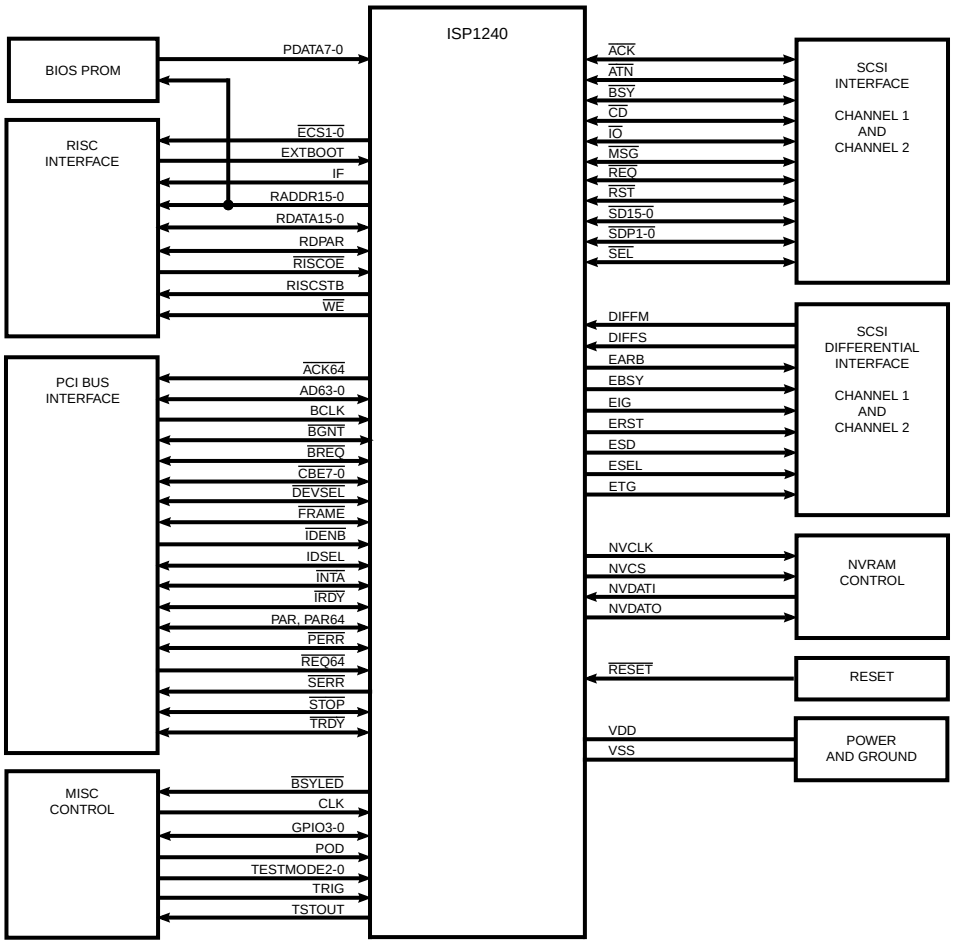


Figure 3. ISP1240 Functional Signal Grouping

SCSI Executive Processors

Each ISP1240 SXP supports the following:

- SCSI A and P cable ready
- Ultra SCSI (Fast-20) synchronous data transfer rates up to 40 Mbytes/sec
- Asynchronous SCSI data transfer rates up to 12 Mbytes/sec
- Programmable SCSI processor
- 32-bit, configurable SCSI transfer counter
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

RISC Processor

The ISP1240 RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

The onboard RISC processor enables the ISP1240 to handle complete I/O transactions with no intervention from the host. The ISP1240 RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs for both SCSI channels; and maintains the required thread information for each transfer.

Packaging

The ISP1240 is available in a 352-pin thermally enhanced (TE) ball grid array (BGA).

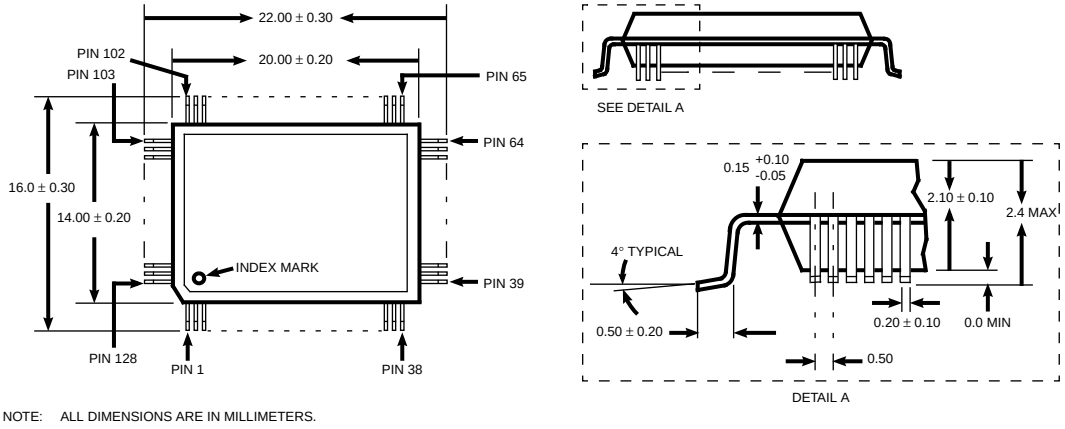


Figure 1. ATEC378 128-Pin PQFP Mechanical Drawings

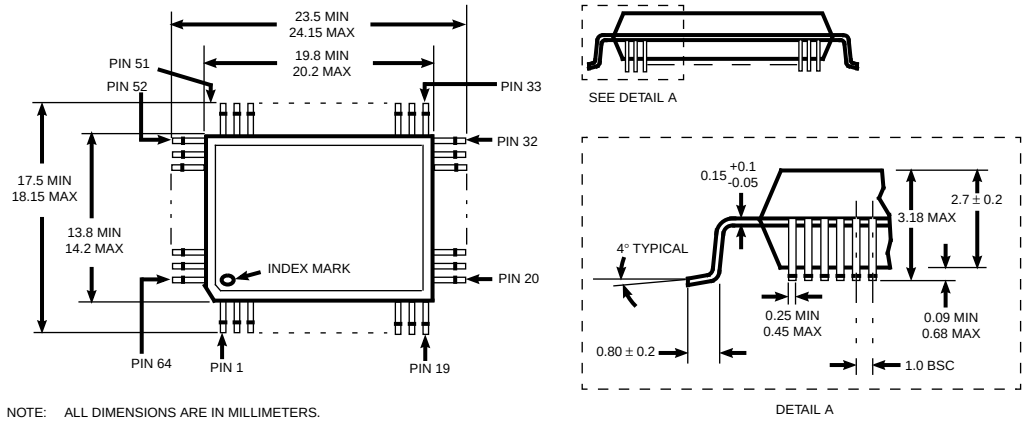
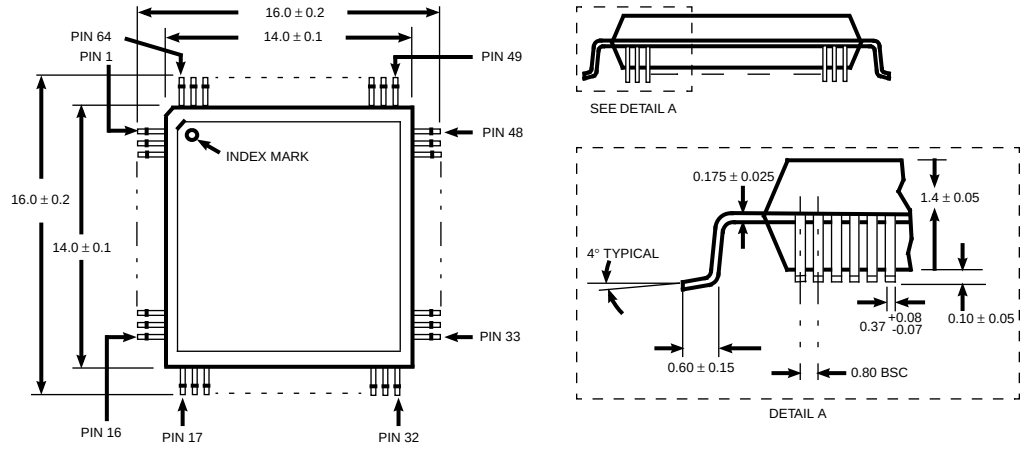
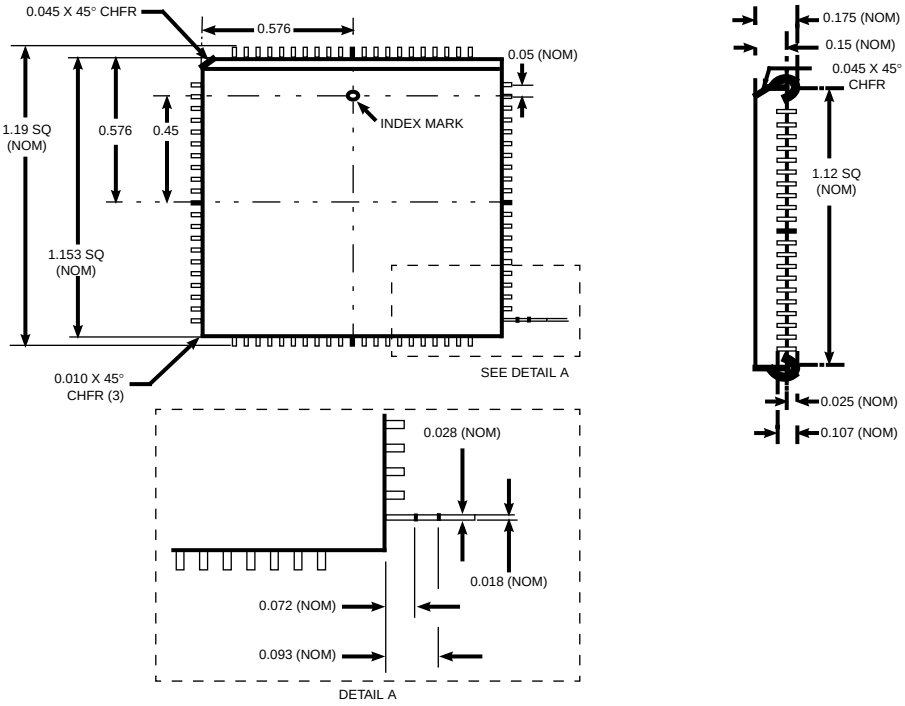


Figure 2. FAS209 64-Pin PQFP Mechanical Drawings



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 3. FAS209 64-Pin TQFP Mechanical Drawings



NOTE: ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ARE NOMINAL UNLESS SPECIFIED OTHERWISE.

Figure 4. FAS216/216U 84-Pin PLCC Mechanical Drawings

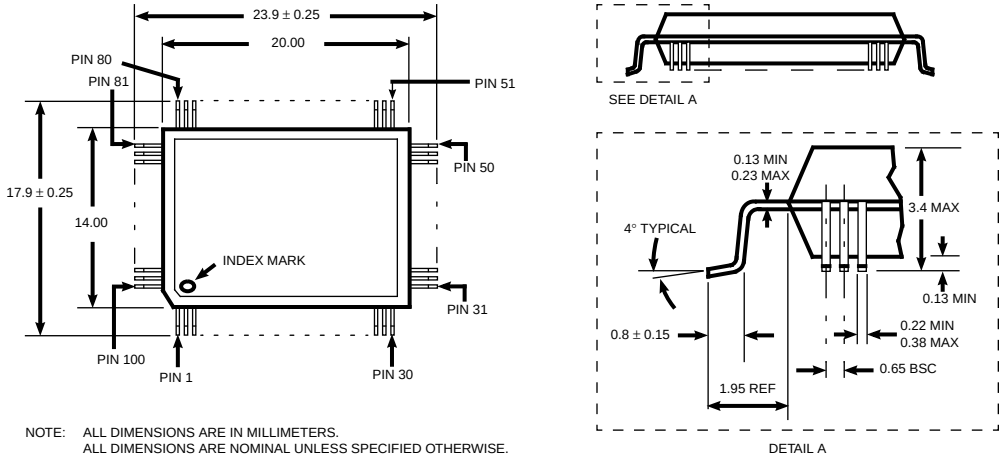


Figure 5. FAS236/236U 100-Pin PQFP Mechanical Drawings

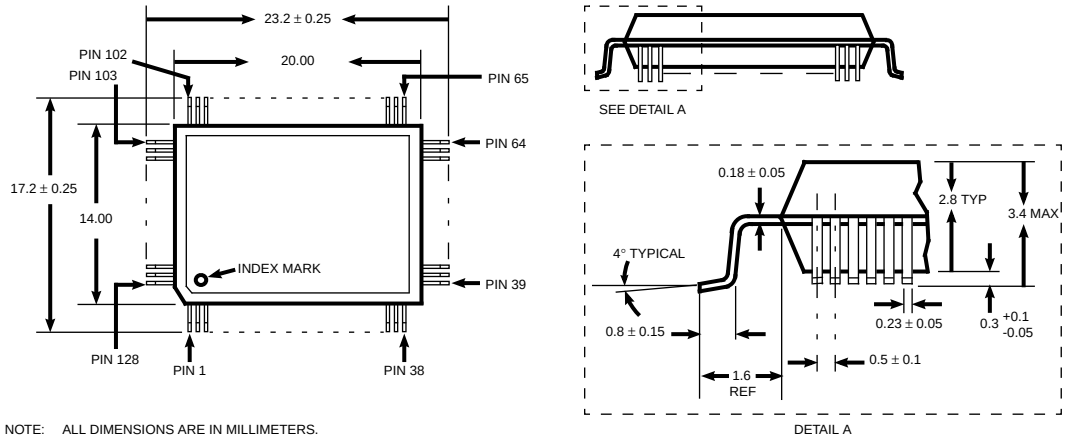
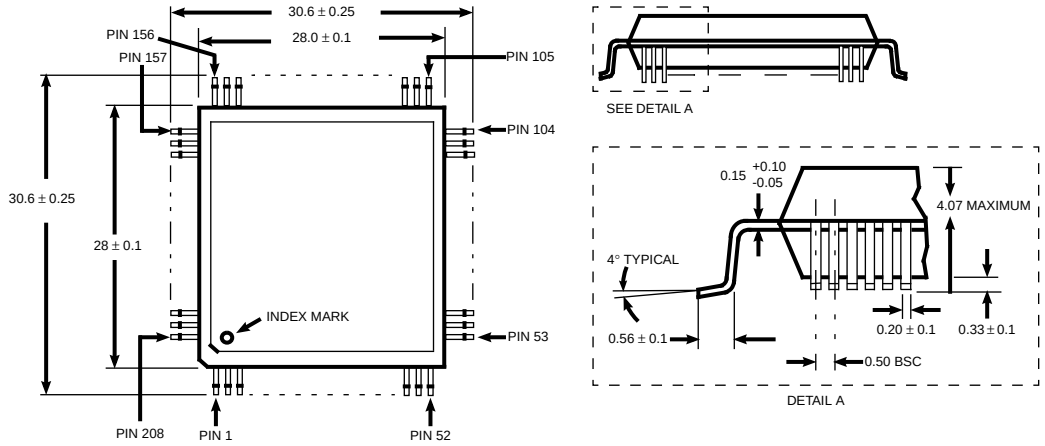
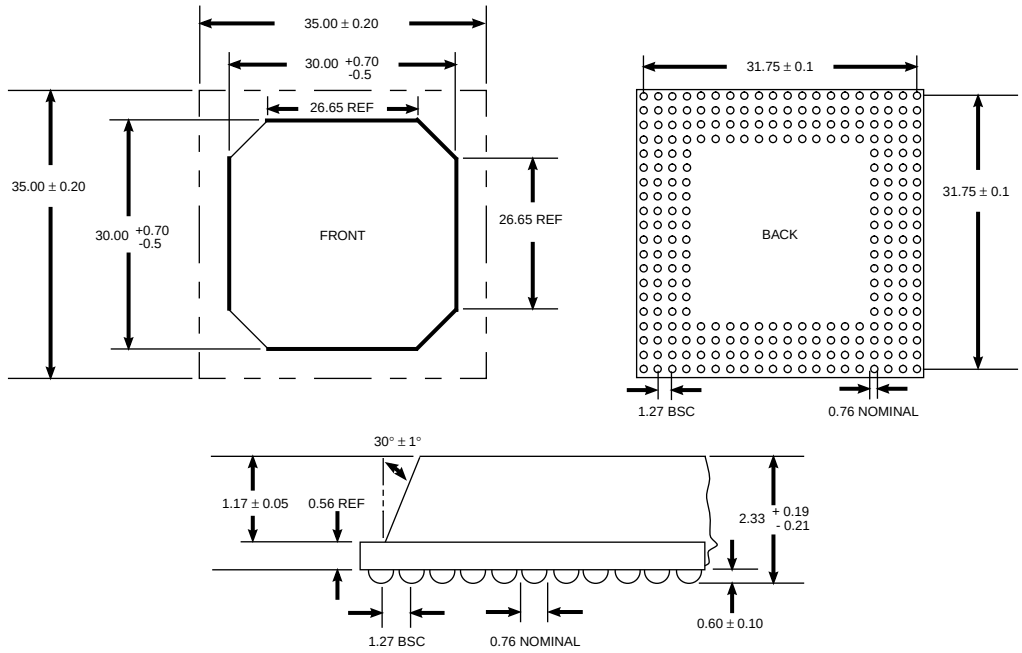


Figure 6. FAS366/366U 128-Pin PQFP Mechanical Drawings



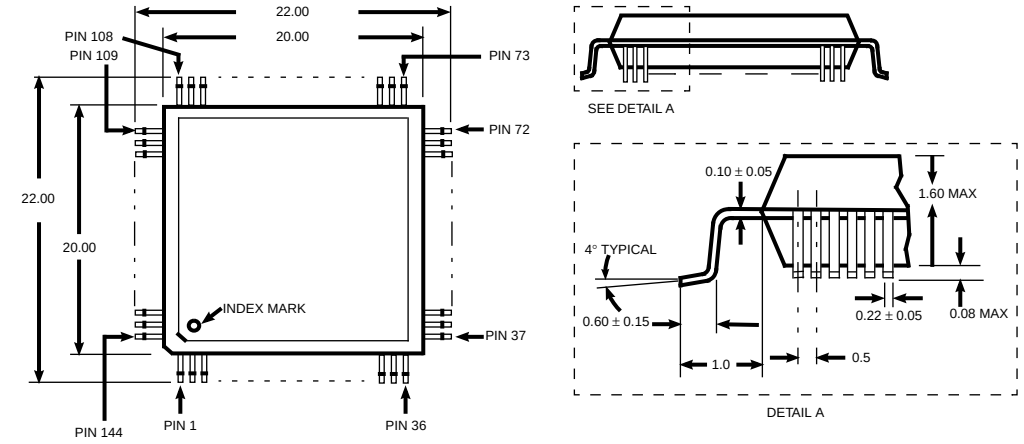
NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 7. ISP1000/1000U/1040B 208-Pin PQFP Mechanical Drawings



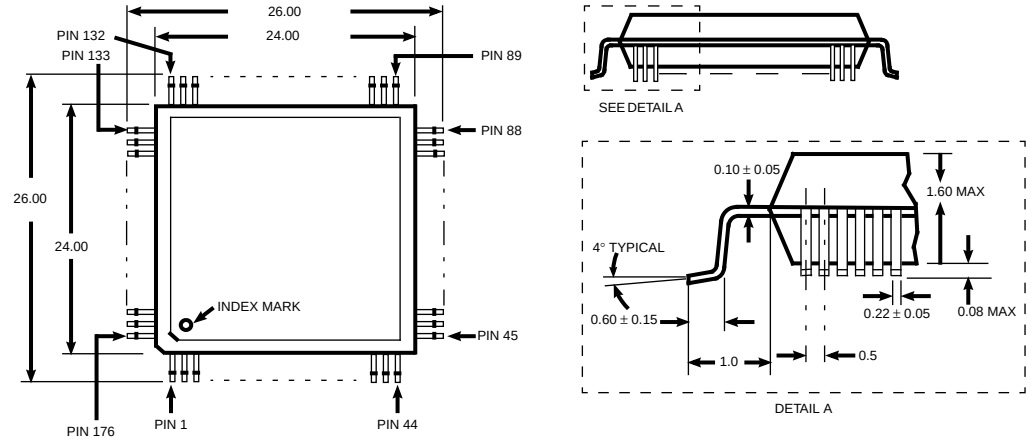
NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 8. ISP1080/1240 352-Pin BGA Mechanical Drawings



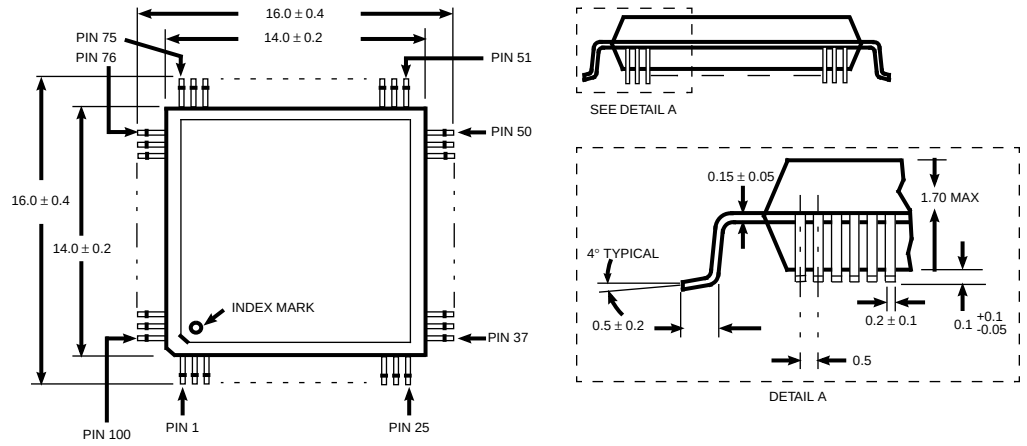
NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 9. TEC336 144-Pin PQFP Mechanical Drawings



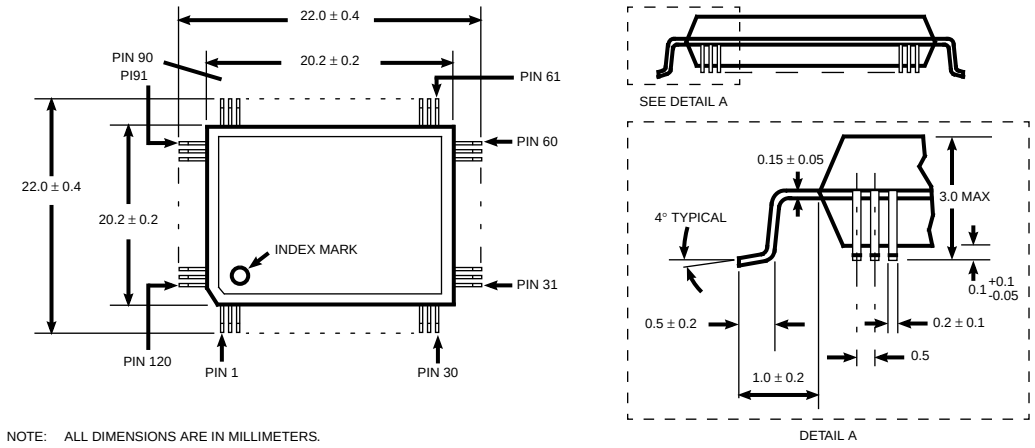
NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 10. TEC356 176-Pin PQFP Mechanical Drawings



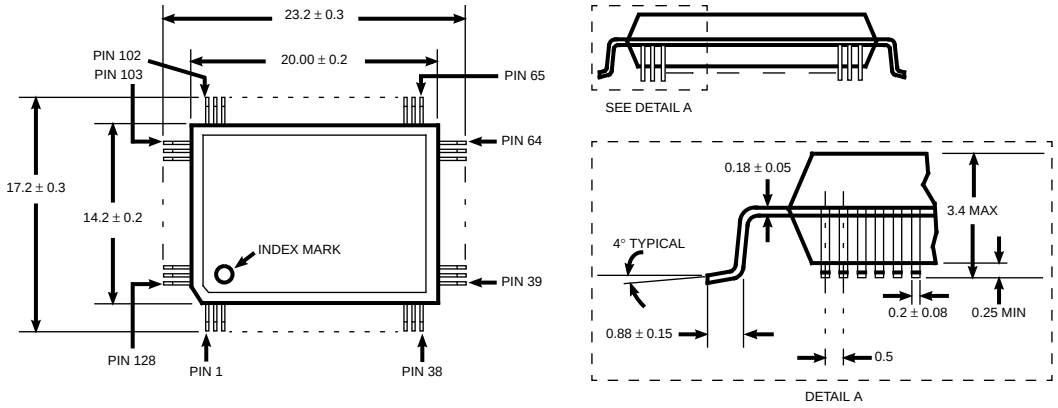
NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 11. TEC376 100-Pin PQFP Mechanical Drawings



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 12. TEC386 120-Pin PQFP Mechanical Drawings



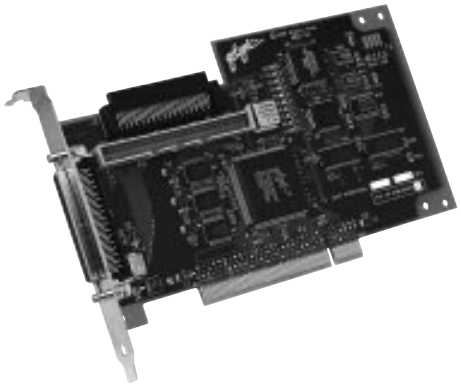
NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 13. TEC420 128-Pin PQFP Mechanical Drawings

QLA1040/1041
PCI-to-Ultra SCSI Boards (Single-Ended/Differential)

Features

- SCSI bus transfer rates up to:
  - ❒ 40 Mbytes/sec wide
  - ❒ 20 Mbytes/sec narrow
- 32-bit bus master data transfers up to 132 Mbytes/sec
- Sustained data transfer rates up to 10,000 I/Os per second (actual performance varies with system configuration and I/O transfer size)
- Only one PCI bus interrupt per SCSI I/O operation
- Compatible with SCSI-2; SCSI-3; Ultra SCSI; and wide, Ultra SCSI peripherals
- Supports up to 15 concurrent SCSI peripherals
  - ❒ Single-ended support (QLA1040)
  - ❒ Differential support (QLA1041)
- SCSI disconnect/reconnect queued in on-chip memory
- SCSI transfer rate arbitration and error recovery managed onboard
- Flash ROM BIOS included for easy field upgrades
- Active termination (QLA1040)
- Plug and play – no switches or jumpers necessary
- Internal 68-pin and 50-pin SCSI connectors
- External 68-pin, high-density SCSI connector
- Meets or exceeds U.S. and international safety/emissions standards



QLA1040

QLA1041

Product Description

The QLA1040/1041 is an extremely high performance, third-generation Ultra SCSI board representing the best in SCSI processor integration.

Based on QLogic's industry-leading, dual processor ISP1040B PCI-to-wide Ultra SCSI chip, the high-speed QLA1040/1041 can handle up to 10,000 I/Os per second, depending on system configuration and I/O transfer size. The chip also minimizes host CPU loading (no more than one host interrupt generated per SCSI I/O). The ISP1040B's two on-chip processors manage the SCSI bus protocol and host system interface, respectively. This management permits the QLA1040/1041 to complete entire SCSI I/O instructions, as well as manage many types of exception or error conditions, without host CPU intervention. This combination of performance and host CPU independence makes the QLA1040/1041 ideal for performance-sensitive workstation and server environments.

Peripheral Support

The QLA1040/1041 concurrently supports synchronous and asynchronous SCSI-2; SCSI-3; fast, wide SCSI; Ultra SCSI; and wide, Ultra SCSI devices. Fixed and removable disks, optical disks, tape drives, scanners, CD-ROMs, and CD-recorders are supported.

Software Driver Features

- QLogic software drivers for AIX, BIOS, DOS ASPI, I20 IXWorks, NetWare4.X, OS/2 Warp, SCO 5.0, Solaris, UnixWare Gemini, UnixWare 2.1, VX Works, Windows 95, Windows NT 4.0.
- Installation utility for quick integration of driver software
- Easy host software migration from Ultra SCSI to Fibre Channel SCSI-FCP
- Software compatible with QLogic's other ISP1040-based host adapters

The QLA1040/1041's advanced, message-style host software interface permits nearly complete host software compatibility between the QLA1040/1041 and QLogic's QLA2100 board, enabling QLA1040/1041 software to migrate from parallel SCSI to Fibre Channel with minimal changes. This feature allows developers to retain their current host software investment while migrating to future SCSI interface technologies.

Technical Specifications

The QLA1040/1041 technical specifications are listed in table 1.

Table 1. QLA1040 Technical Specifications

Type	Specification
Host bus	Conforms to *PCI Local Bus Specification* revision 2.1
SCSI standard	ANSI X3.131-1994 SCSI-2/SCSI-3 SPI; X3T10/855D SCSI-3 Fast-20 X3T10/1071D
SCSI data transfer rates	Up to 40 Mbytes/sec
Data transfer	Asynchronous and synchronous transfers to 40 Mbytes/sec
SCSI data handling	8-bit narrow and 16-bit wide Single-ended (QLA1040) Differential (QLA1041)
Onboard processors	Single chip, dual processor design: RISC engine and SCSI executive processor

Table 1. QLA1040 Technical Specifications (Continued)

Type	Specification
Host data transfer	32-bit bus master DMA data transfers to 132 Mbytes/sec
RAM	64 Kbytes static RAM
DMA channels	128-byte data DMA FIFO with threshold control and 64-byte command DMA FIFO
Electrical drivers	On-chip, 48-mA, single-ended (QLA1040) Differential (QLA1041)
Connectors	68-pin, high-density external SCSI connector 68-pin and 50-pin internal ribbon connectors
Termination	Active, software controlled (QLA1040) Passive (socketed resistors) (QLA1041)
Form factor	17.78 cm x 10.67 cm (7.0" x 4.2")
Operating temperature	0°C/32°F to 55°C/131°F
Storage temperature	-20°C/-4°F to 70°C/158°F
Relative humidity	10% to 90% (noncondensing)
Storage humidity	5% to 95% (noncondensing)

QLA1042/1042D
PCI-to-Ultra SCSI Dual Channel Boards (Single-Ended/Differential)

Features

- SCSI bus transfer rates (on two independent channels) of up to
  - ❒ 40 Mbytes/sec (wide)
  - ❒ 20 Mbytes/sec (narrow)
- 32-bit bus master data transfers up to 132 Mbytes/sec per channel
- Sustained data transfer rates up to 10,000 I/Os per second per channel (actual performance varies with system configuration and I/O transfer size)
- Only one PCI bus interrupt per SCSI I/O operation
- Compatible with SCSI-2; SCSI-3; Ultra SCSI; and wide, Ultra SCSI peripherals
- Supports up to 15 concurrent SCSI peripherals per channel
  - ❒ Single-ended support (QLA1042)
  - ❒ Differential support (QLA1042D)
- SCSI disconnect/reconnect queued in on-chip memory
- SCSI transfer rate arbitration and error recovery managed onboard
- Flash ROM BIOS included for easy field upgrades
- Active termination (QLA1042)
- Plug and play – no switches or jumpers necessary
- Two external 68-pin VHDC connectors
- One internal 68-pin, high density connector (QLA1042)
- Meets or exceeds U.S. and international safety/emissions standards

Product Description

The QLA1042/1042D is an extremely high-performance, dual channel Ultra SCSI board targeted at high-connectivity SCSI applications.

Based on two QLogic wide, Ultra SCSI processor ISP1040B chips (one chip per channel), the high speed QLA1042/1042D supports two wide, Ultra SCSI channels, each capable of handling up to 10,000 I/Os per second, depending on system configuration and I/O transfer size. Each ISP1040B chip contains two on-chip processors that manage the SCSI bus protocol and host system interface, respectively. This management allows the QLA1042/1042D to complete entire SCSI I/O instructions, as well as manage many types of exception or error corrections, without host CPU intervention (no more than one host interrupt is generated per SCSI I/O). This powerful combination of performance and host CPU independence make the QLA1042/1042D ideal for performance-sensitive workstation and server environments.

Peripheral Support

The QLA1042/1042D concurrently supports synchronous and asynchronous SCSI-2; SCSI-3; fast, wide SCSI; Ultra SCSI; and wide, Ultra SCSI devices. Fixed and removable disks, optical disks, tape drives, scanners, CD-ROMs, and CD-recorders are supported.

Software Driver Features

- QLogic software drivers for AIX, BIOS, DOS ASPI, I20 IXWorks, NetWare4.X, OS/2 Warp, SCO 5.0, Solaris, UnixWare Gemini, UnixWare 2.1, VX Works, Windows 95, Windows NT 4.0.
- Easy host software migration from ultra SCSI to Fibre Channel SCSI-FCP
- Software compatible with QLogic's other ISP1040B-based host adapters

The QLA1042/1042D's advanced, message-style host software interface permits nearly complete host software compatibility between the QLA1042/1042D and QLogic's QLA2100 board, enabling QLA1042/1042D software to migrate from parallel SCSI to Fibre Channel with minimal changes. This feature allows developers to retain their current host software investment while migrating to future SCSI interface technologies.

Technical Specifications

The QLA1042/1042D technical specifications are listed in table 1.

Table 1. QLA1042/1042D Technical Specifications

Type	Specification
Host bus	Conforms to *PCI Local Bus Specification* revision 2.1
SCSI standard	ANSI X3.131-1994 SCSI-2/SCSI-3 SPI; X3T10/855D SCSI-3 Fast-20 X3T10/1071D
SCSI data transfer rates	Up to 40 Mbytes/sec on each independent SCSI channel
Data transfer	Asynchronous and synchronous transfers to 40 Mbytes/sec per channel
SCSI data handling	8-bit narrow, 16-bit wide Single-ended (QLA1042) Differential (QLA1042D)
Onboard processors	Single chip per channel, dual processor design with RISC engine and SCSI executive processor
Host data transfer	32-bit bus master DMA data transfers to 132 Mbytes/sec on each channel
RAM	64 Kbytes static RAM per channel

Table 1. QLA1042/1042D Technical Specifications (Continued)

Type	Specification
DMA channels	128-byte data DMA FIFO with threshold control and 64-byte command DMA FIFO on each channel
Electrical drivers	On-chip, 48-mA, single-ended SCSI drivers (QLA1042) Differential (QLA1042D)
Connectors	Two external, 68-pin VHDC connectors One internal, 68-pin high-density connector (QLA1042)
Termination	Active, software controlled (QLA1042) Passive (socketed resistors) (QLA1042D)
Form factor	32.20 cm x 110.67 cm (12.283" x 4.2")
Operating temperature	0°C/32°F to 55°C/131°F
Storage temperature	-20°C/-4°F to 70°C/158°F
Relative humidity	10% to 90% (noncondensing)
Storage humidity	5% to 95% (noncondensing)

Section 4

Fibre Channel Computer Products

ISP2100
Intelligent Fibre Channel Processor

Features

- Direct connection to 64-bit PCI bus
- Compliance with ANSI SCSI standard X3.131-1994
- Compliance with *Fibre Channel Arbitrated Loop (FC-AL) Direct Disk Attach Profile*, class 3 operation. Supports 100 Mbytes/sec sustained data transfer rate
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control-block (IOCB) level from the host memory
- On-board gigabit serial transceivers
- Supports external transceivers with a 10-bit interface
- No host intervention required to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads

Product Description

The ISP2100 is a single-chip, highly integrated, bus master, Fibre Channel processor that targets SCSI applications. This chip connects the PCI bus to a Fibre Channel interface and contains an onboard RISC processor. The ISP2100 is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention. The ISP2100 block diagram is illustrated in figure 1.

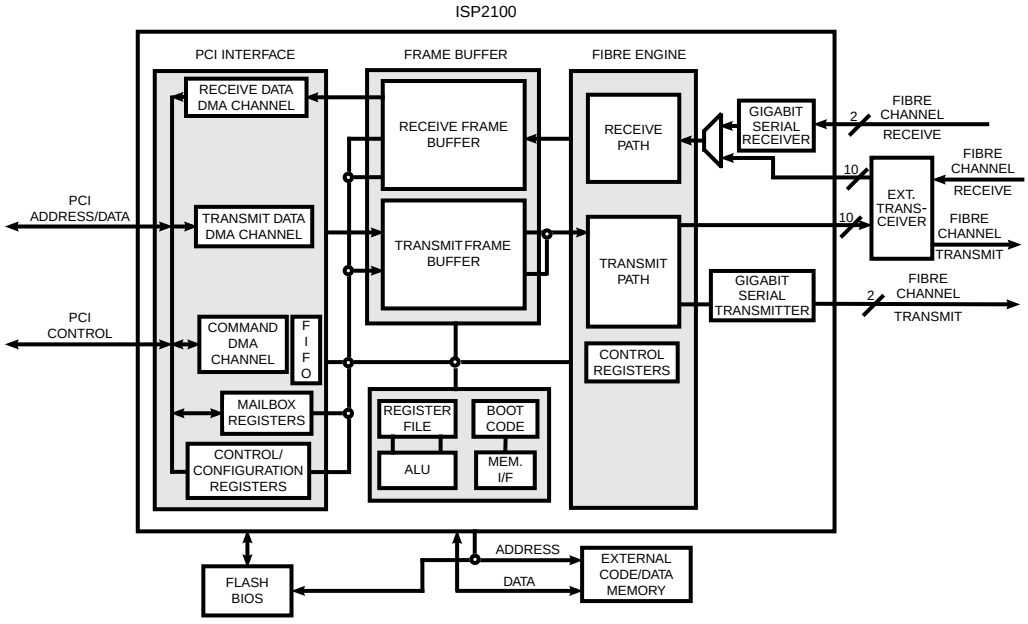


Figure 1. ISP2100 Block Diagram

Fibre Channel Products

ISP Firmware

The ISP2100 firmware implements a multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI Fibre Channel protocol (FCP). The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and recovering errors. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

Software Drivers

The ISP2100 supports a host software interface similar to the parallel SCSI family. Existing ISP1040B software drivers are easily modified to support the ISP2100.

Subsystem Organization

To maximize I/O throughput and improve host and loop utilization, the ISP2100 incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, three-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2100 and associated supporting memory devices is shown in figure 2.

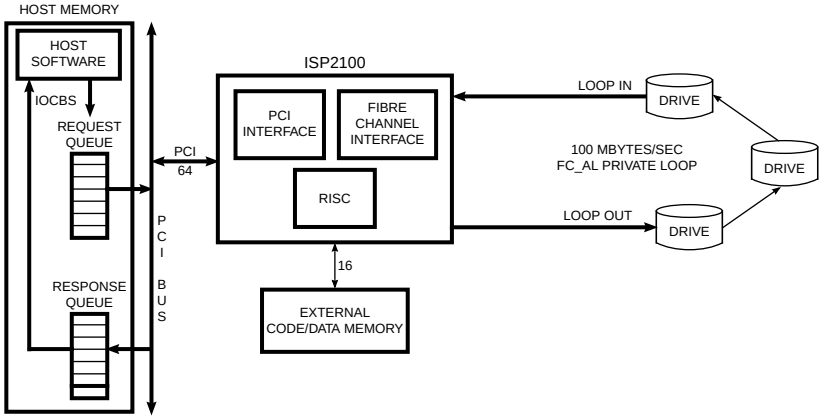


Figure 2. I/O Subsystem Design Using the ISP2100

Interfaces

The ISP2100 interfaces consist of the Fibre Channel interface, PCI bus interface, RISC interface, BIOS PROM interface, and NVRAM control. Pins that support these interfaces and other chip operations are shown in figure 3.

Fibre Channel Interface

The ISP2100 provides on-board gigabit transceivers for direct connection to the Fibre Channel loop on copper media. A standard 10-bit interface is also provided to connect to external transceivers, if desired.

Fibre Channel Protocol Manager

The ISP2100 FPM supports the following:

- Support for one Fibre Channel loop
- 100 Mbytes/sec sustained data transfer rate
- 10-bit interface to external transceivers
- Gigabit serial interface
- Integrated frame buffer

The FPM includes an 8B/10B encoder and decoder, an elasticity buffer for clock skew management, and an FC-AL state machine. The FPM transmits and receives at the full Fibre Channel rate of 106.25 Mbytes/sec. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for

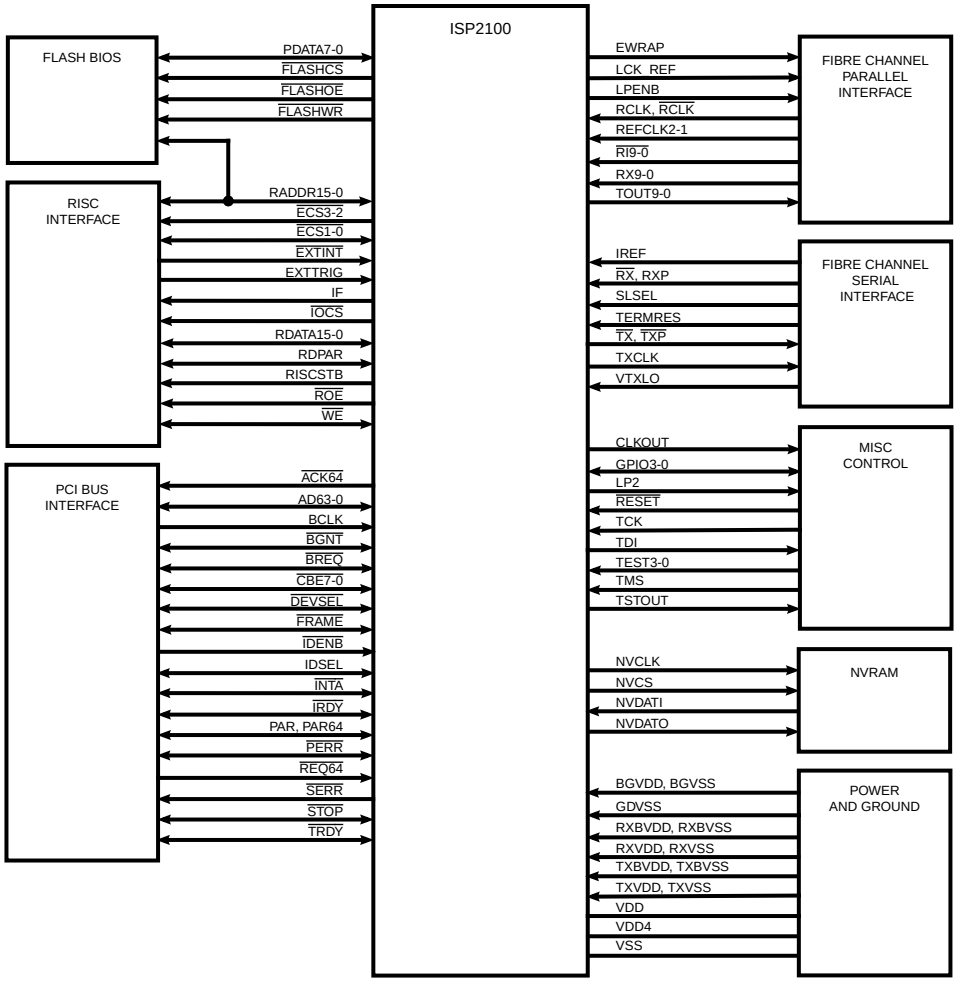


Figure 3. ISP2100 Functional Signal Grouping

managing special frames such as command and response. The FPM receive path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer. The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

PCI Interface

The ISP2100 PCI interface supports the following:

- 64-bit, intelligent bus master interface for fetching IOCBs and data transfers
- Three DMA channels
- 16-bit slave mode for communication with host
- JTAG boundary scan
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit transfer counter for I/O transfer length of up to 4 Gbytes
- Support for flash BIOS

The ISP2100 is designed to interface directly to the PCI bus and operate as a 64-bit, DMA bus master, which is backward compatible to 32-bit operation. This function is accomplished through a PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI control signals,

generates host memory addresses, and facilitates the transfer of data between host memory and the onboard frame buffer. It also allows the host to access the ISP2100 internal registers and communicate with the onboard RISC processor.

The ISP2100 onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and frame buffer. The command DMA channel is used mainly by the RISC processor for small transfers, such as fetching commands from and writing status information to the host memory over the PCI bus. The two data DMA channels, one for transmit and one for receive, transfer data between the Fibre Channel interface and the PCI bus, allowing for fast context switching.

The PBIU internally arbitrates between the two data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

RISC Processor

The ISP2100 RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2100 is its ability to handle complete I/O transactions from start to finish with no intervention from the host. This high level of integration is accomplished with an onboard RISC processor. The ISP2100 RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

Packaging

The ISP2100 is available in a 256-pin ball grid array (BGA). The mechanical drawings are illustrated in figure 4.

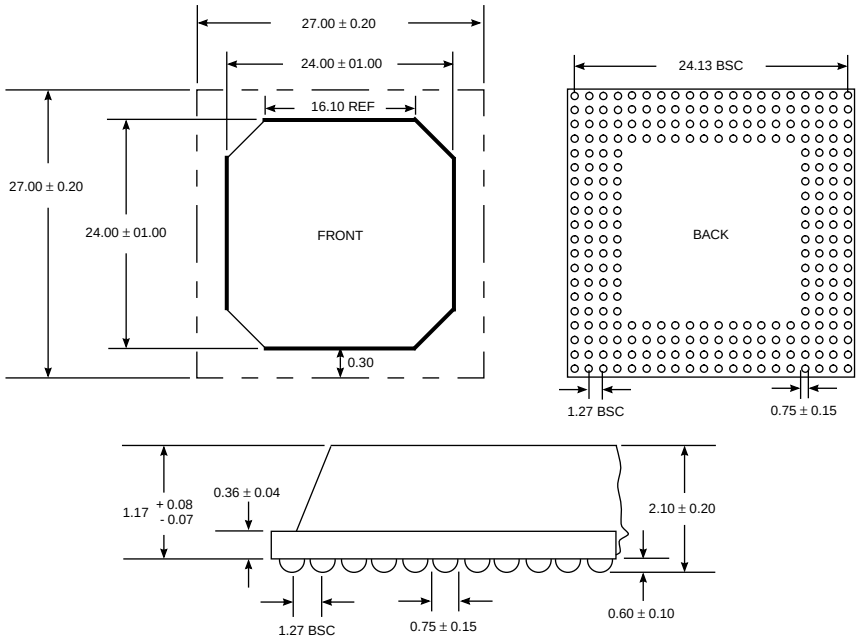
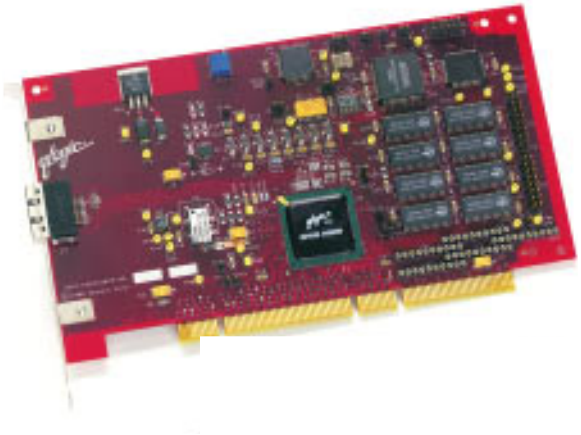


Figure 4. ISP2100 Mechanical Drawings

Fibre Channel Development Board

Features

- On-chip gigabit serial transceivers
- 100 Mbytes/sec fibre channel speed
- 64-bit bus master data transfers of up to 264 Mbytes/sec
- Only one PCI bus interrupt per SCSI I/O operation
- Compatible with Fibre Channel direct disk attach peripherals
- Supports up to 126 concurrent Fibre Channel devices
- QLogic drivers support major operating systems
- Uses copper media
- SCSI initiator and target operation
- Flash ROM BIOS included for easy field upgrades
- External high speed serial data connector (HSSDC) Fibre Channel connector



Product Description

QLogic's PCI-to-fibre channel development board provides an excellent development platform for QLogic's industry-leading ISP2100 PCI-to-fibre channel host processor chip.

Supporting standard PCI board features such as BIOS firmware (field-upgradeable flash ROM) and nonvolatile NVRAM (for Fibre Channel configuration parameters), the fibre channel development board helps users complete their ISP2100 designs quickly and helps minimize debug activity.

Supporting integrated Fibre Channel transceivers, the highly intelligent ISP2100 PCI-to-Fibre Channel host processor chip can support 100 Mbytes/sec transfer rates while minimizing host CPU loading (no more than one host interrupt is generated per completed I/O in SCSI applications). The on-chip RISC processor and Fibre Channel protocol manager permit the ISP2100 to complete entire I/O instructions, as well as manage many types of exception or error conditions without host CPU intervention. This powerful combination of performance and host CPU independence makes the ISP2100 ideal for performance-sensitive workstation and server environments.

Software Drivers

The fibre channel development board's advanced, message-style host software interface permits a high degree of host software compatibility between the ISP2100 and QLogic's ISP1040B PCI-to-Ultra SCSI host processor chip. The compatibility enables ISP1040B SCSI host software to migrate from parallel SCSI to Fibre Channel with minimal changes. The software migration from Ultra SCSI to Fibre Channel SCSI-FCP enables QLogic SCSI customers to retain their host software investment while migrating to future interface technologies.

Technical Specifications

The fibre channel development board technical specifications are listed in table 1.

Table 1. Fibre Channel Development Board Technical Specifications

Type	Specification
Host bus	Conforms to *PCI Local Bus Specification* revision 2.1
Fibre Channel data transfer rate	100 Mbytes/sec
Onboard processors	Single chip, ISP2100 Fibre Channel processor
Host data transfer	64-bit bus master DMA data transfers to 264 Mbytes/sec
RAM	256 Kbytes static RAM
Onboard DMA channels	Two data DMA channels and one command DMA channel. There is one 4-Kbyte frame buffer FIFO for each data DMA channel.
Connectors	One external HSSDC Fibre Channel connector that supports copper cabling
Form factor	17.46 cm x 10.67 cm (6.875” x 4.2”)
Operating temperature	0°C/32°F to 55°C/131°F
Storage temperature	-20°C/-4°F to 70°C/158°F
Relative humidity	10% to 90% (noncondensing)
Storage humidity	5% to 95% (noncondensing)