

# ***Evaluation board Manual***

# **MB39A110**

***Rev 1.0E***  
***October, 2002***

## **MB39A110 Evaluation board**

### **MB39A110 Specifications**

#### **1. Pin Assignments**

#### **2. Package & Dimension**

#### **3. Pin Descriptions**

#### **4. Block Diagram**

#### **5. Setting Method**

##### **1) Output Voltage**

##### **2) Triangular Wave Oscillation Frequency**

##### **3) Soft-Start Time**

##### **4) CTL Functional Matrix**

##### **5) Functional Matrix of Protection enable**

##### **6) Time Constant For Timer-Latch Short-Circuit Protection Circuit**

### **MB39A110 Evaluation board Explanations**

#### **1. Evaluation Board Specifications**

#### **2. Pin Descriptions**

#### **3. Sw Information**

#### **4. Setup & Confirmation Method**

#### **5. Parts Layout Block**

#### **6. Circuit Diagram**

#### **7. Circuit Parts List**

#### **8. Initialization**

#### **9. Reference Data**

#### **10. Parts Select Method**

# **MB39A110**

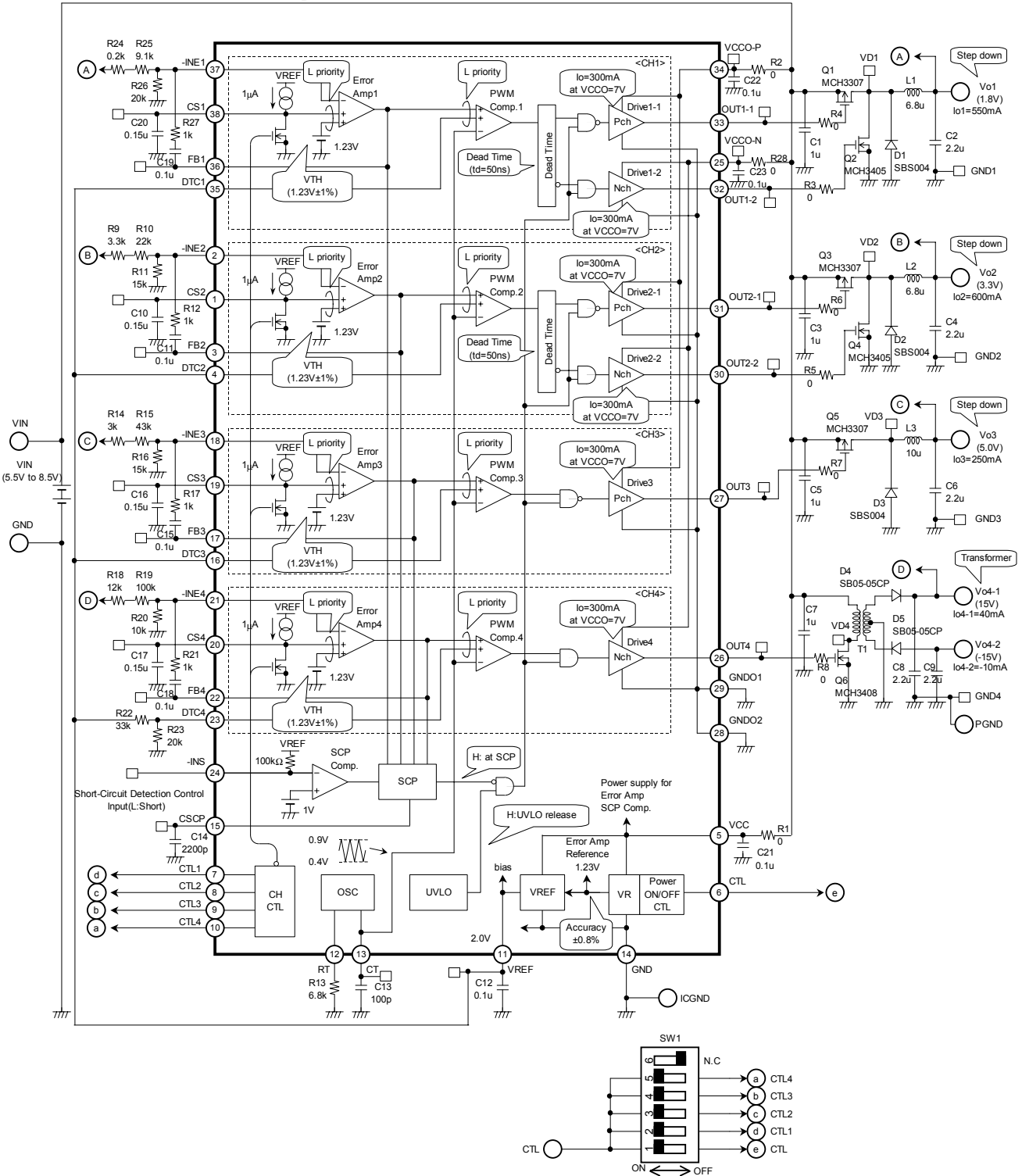
# **Specifications**



## 3. Pin Descriptions

Pin No	Pin Name	I/O	Description
CH1	35	DTC1	I CH1 dead time control terminal.
	36	FB1	O CH1 error amplifier output terminal.
	37	-INE1	I CH1 error amplifier inverted input terminal.
	38	CS1	- CH1 soft-start setting capacitor terminal.
	33	OUT1-1	O CH1 Pch drive output terminal. (External main side FET gate drive)
	32	OUT1-2	O CH1 Nch drive output terminal. (External synchronous rectification side FET gate drive)
CH2	4	DTC2	I CH2 dead time control terminal.
	3	FB2	O CH2 error amplifier output terminal.
	2	-INE2	I CH2 error amplifier inverted input terminal.
	1	CS2	- CH2 soft-start setting capacitor terminal.
	31	OUT2-1	O CH2 Pch drive output terminal. (External main side FET gate drive)
	30	OUT2-2	O CH2 Nch drive output terminal. (External synchronous rectification side FET gate drive)
CH3	16	DTC3	I CH3 dead time control terminal.
	17	FB3	O CH3 error amplifier output terminal.
	18	-INE3	I CH3 error amplifier inverted input terminal.
	19	CS3	- CH3 soft-start setting capacitor terminal.
	27	OUT3	O CH3 Pch drive output terminal.
CH4	23	DTC4	I CH4 dead time control terminal.
	22	FB4	O CH4 error amplifier output terminal.
	21	-INE4	I CH4 error amplifier inverted input terminal.
	20	CS4	- CH4 soft-start setting capacitor terminal.
	26	OUT4	O CH4 Nch drive output terminal.
OSC	13	CT	- Triangular wave oscillation frequency setting capacitor connection terminal.
	12	RT	- Triangular wave oscillation frequency setting resistor connection terminal.
Control	6	CTL	I Power supply control terminal.
	7	CTL1	I CH1 control terminal.
	8	CTL2	I CH2 control terminal.
	9	CTL3	I CH3 control terminal.
	10	CTL4	I CH4 control terminal.
	15	CSCP	- Timer latch short-circuit detection capacitor connection terminal.
	24	-INS	I Short-circuit detection comparator inverted input terminal.
Power	34	VCCO-P	- Pch drive output block power supply terminal.
	25	VCCO-N	- Nch drive output block power supply terminal.
	5	VCC	- Power supply terminal
	11	VREF	O Reference voltage output terminal.
	29	GND01	- Drive output block ground terminal.
	28	GND02	- Drive output block ground terminal.
	14	GND	- Ground terminal.

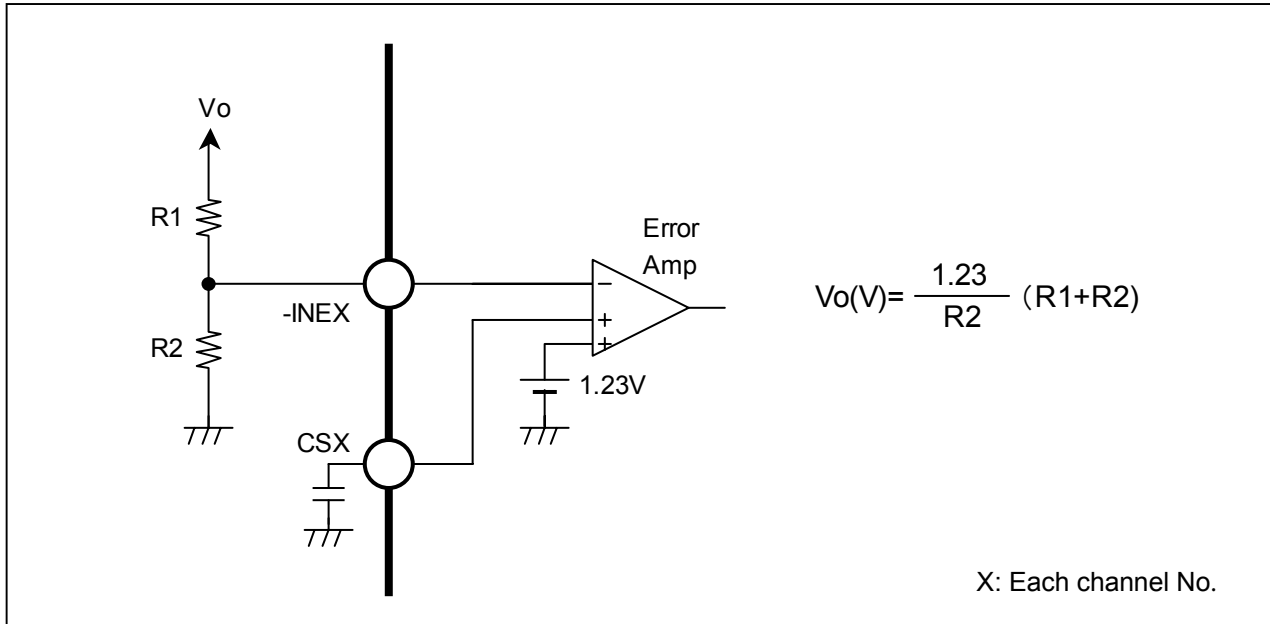
# 4. Block Diagram



It is IC operation, and a state of all channel ON in the above figure.

## 5. Setting Method

### 1) Output Voltage



### 2) Triangular Wave Oscillation Frequency

Oscillation frequency can be set by timing capacitor (CT) connected to CT terminal (pin 13) and timing resistor (RT) connected to RT terminal (pin 12).

Triangular wave oscillation frequency : fosc

$$f_{osc}(\text{kHz}) \cong \frac{693600}{C_T(\text{pF}) \times R_T(\text{k}\Omega)}$$

### 3) Soft-Start Time

To provide a soft-start by preventing current surges at power-on, soft-start capacitor (Cs) can be connected to the CS terminal. The error amplifier makes a soft-start in a proportion to the output voltage to the CS terminal voltage regardless of the load current on the DC/DC converter.

Note that the soft-start time can be calculated by the following formula.

Soft-start time (time to output 100%) : ts

$$t_s(\text{s}) \cong 1.23 \times C_s (\mu\text{F})$$

### 4) CTL Functional Matrix

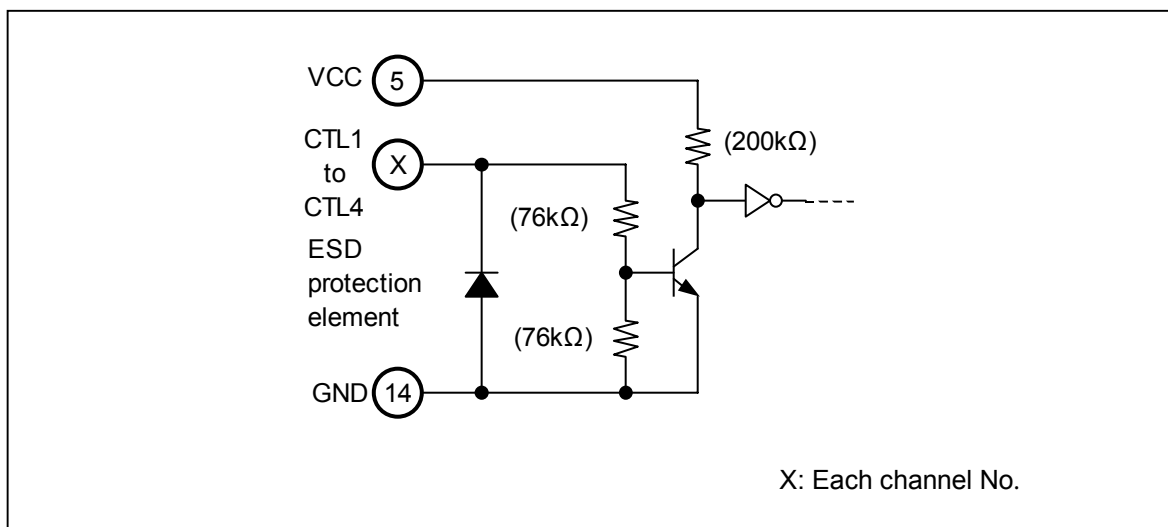
ON/OFF of each channel are set according to a setting condition of the CTL terminal(pin 6), the CTL1 terminal(pin 7), the CTL2 terminal(pin 8), the CTL3 terminal(pin 9), and the CTL4 terminal(pin 10).

CTL	CTL1	CTL2	CTL3	CTL4	Power	CH1	CH2	CH3	CH4
L	-*	-*	-*	-*	OFF	OFF	OFF	OFF	OFF
<b>H</b>	L	L	L	L	<b>ON</b>	OFF	OFF	OFF	OFF
<b>H</b>	<b>H</b>	L	L	L	<b>ON</b>	<b>ON</b>	OFF	OFF	OFF
<b>H</b>	L	<b>H</b>	L	L	<b>ON</b>	OFF	<b>ON</b>	OFF	OFF
<b>H</b>	L	L	<b>H</b>	L	<b>ON</b>	OFF	OFF	<b>ON</b>	OFF
<b>H</b>	L	L	L	<b>H</b>	<b>ON</b>	OFF	OFF	OFF	<b>ON</b>
<b>H</b>	<b>H</b>	<b>H</b>	<b>H</b>	<b>H</b>	<b>ON</b>	<b>ON</b>	<b>ON</b>	<b>ON</b>	<b>ON</b>

\* : Undefined

Note that the current which exceeds the standby current flows to the VCC terminal when either of the CTL1 to CTL 4 terminals is set at H level when the CTL terminal is L level.

(Refer to the CTL1 to CTL4 terminals equivalent circuit.)



<The CTL1 to CTL4 terminals equivalent circuit >



**5) Functional Matrix of Protection enable**

Function	OUT1-1	OUT1-2	OUT2-1	OUT2-2	OUT3	OUT4
Short-Circuit Protection	<u>H</u>	L	<u>H</u>	L	<u>H</u>	L
UVLO	<u>H</u>	L	<u>H</u>	L	<u>H</u>	L

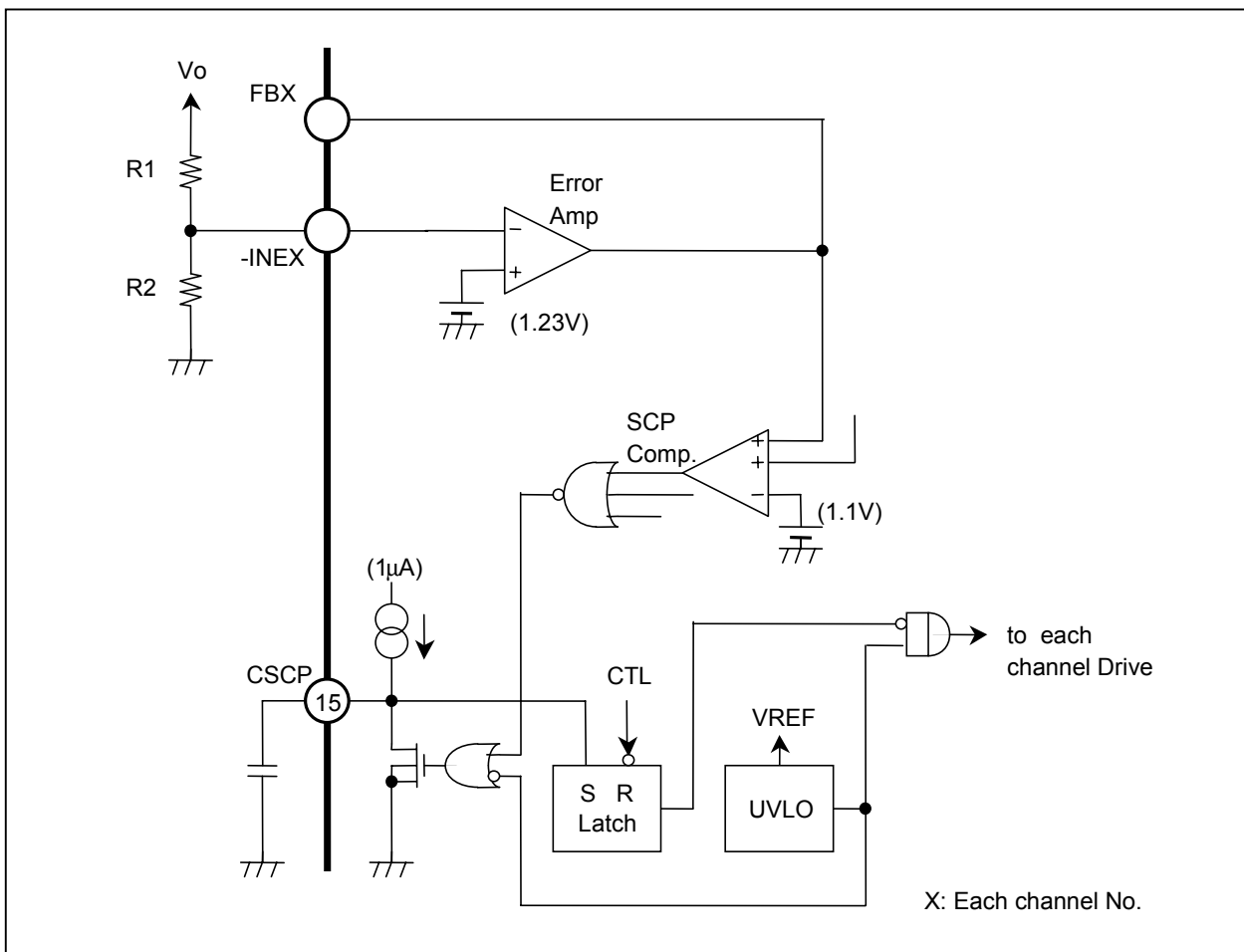
## 6) Constant For Timer-Latch Short-Circuit Protection Circuit

The short-circuit detection comparator (SCP Comp.) in the each channel constantly compares the error amplifier output level. While the DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at “L” level, and the CSCP terminal (pin 15) is held at “L” level. If the load conditions change rapidly due to a short-circuiting of load, causing the output voltage to drop, the output from the short-circuit detection comparator goes to “H” level. The external short-circuit protection capacitor CSCP connected to the CSCP terminal to be charged at 1.0  $\mu\text{A}$ .

Short-circuit detection time :  $t_{cscp}$

$$t_{cscp} \text{ (s)} \cong 0.70 \times C_{SCP} \text{ (\mu F)}$$

When the capacitor CSCP is charged to the threshold voltage  $V_{TH} \cong 0.70\text{V}$  the SR latch is set, and the external FET is turned off (dead time is set to 100%). At this point the SR latch input is closed and the CSCP terminal is held at “L” level. The latch of the timer latch type short-circuit protection circuit can be released by intercepting power supply (VCC) or setting the CTL terminal(pin 6) “L” level.



< Timer latch type short-circuit protection circuit >

# **MB39A110 Evaluation board**

## **Explanations**

## 1. Evaluation Board Specifications

	CH1	CH2	CH3	CH4	
Input voltage	VIN=5.5V to 8.5V(7.2V Typ)				
Oscillation frequency	fosc=1MHz				
Output voltage	1.8V	3.3V	5V	15V	-15V
Output current range	110 to 730mA	150 to 680mA	110 to 730mA	30 to 50mA	-10mA

Note) Output current Min value is decided from the coil discontinuous mode.

## 2. Pin Descriptions

Function table of the Pin terminal

Symbol	Descriptions
VIN	Power supply pin VIN = 5.5V to 8.5V (7.2V Typ)
VoX	DC/DC converter output pin
CTL	Power supply control pin VCTL = 0V to 0.8V : Standby mode VCTL = 2.0V to VIN : Operation mode
PGND	DC/DC converter GND pin
ICGND	MB39A110 GND pin

## 3. Sw Information

DIP Switch Function Table

SW	Name	Function	ON	OFF
1	CTL	Power supply control	Operation mode	Standby mode
2	CTL1	CH1 control	Output ON	Output OFF
3	CTL2	CH2 control	Output ON	Output OFF
4	CTL3	CH3 control	Output ON	Output OFF
5	CTL4	CH4 control	Output ON	Output OFF
6	N.C	Unused	-	-

## 4. Setup & Confirmation Method

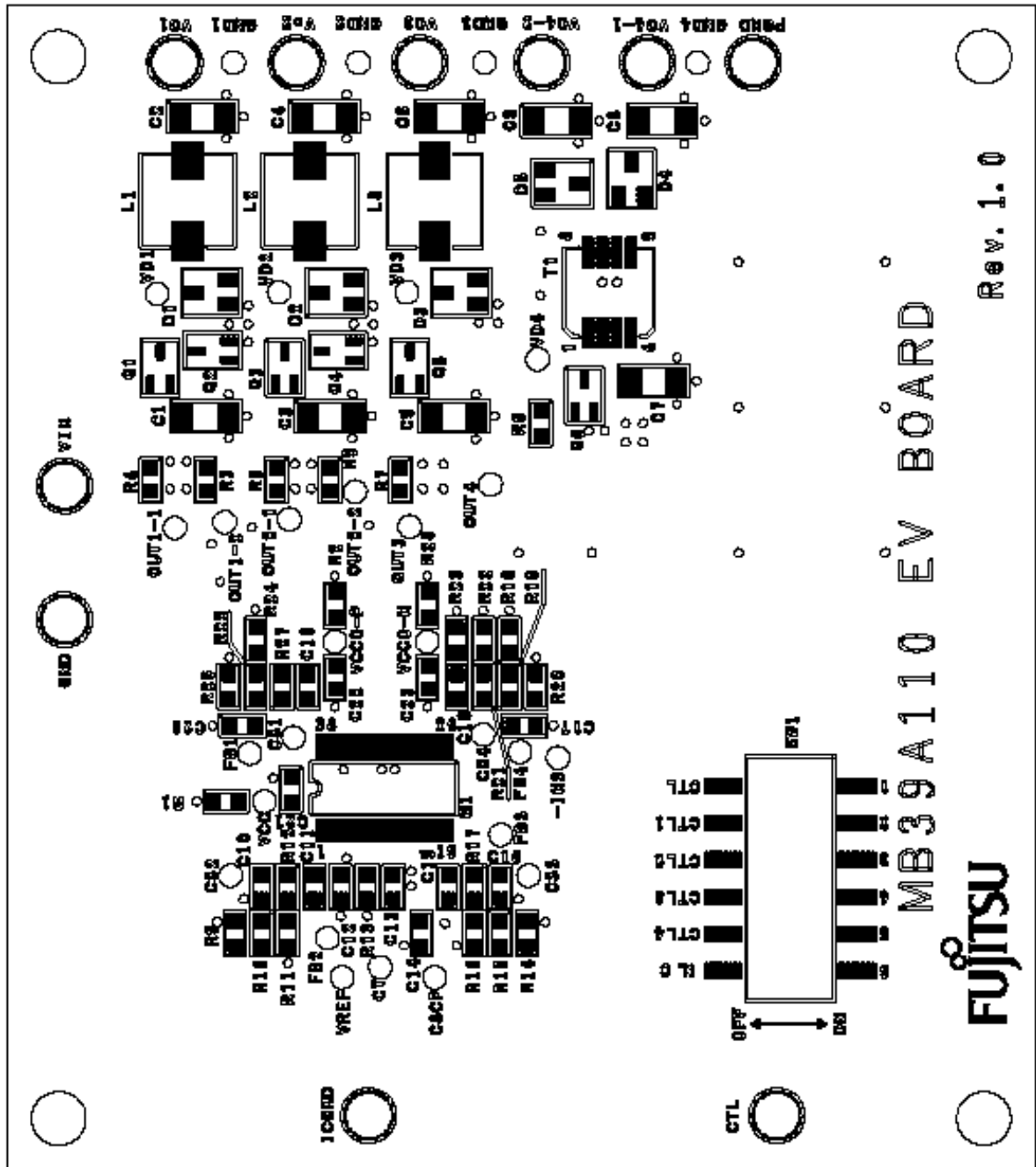
### **(1) Set up**

- \* The power supply side terminal is connected with VIN•GND.  
Please connect the Vo side with a necessary load device or measurement machine.
- \* SW1(CTL) is made OFF(standby mode), and SW2 to SW5(CTL1 to CTL4) is put into the state of turning off (output OFF).

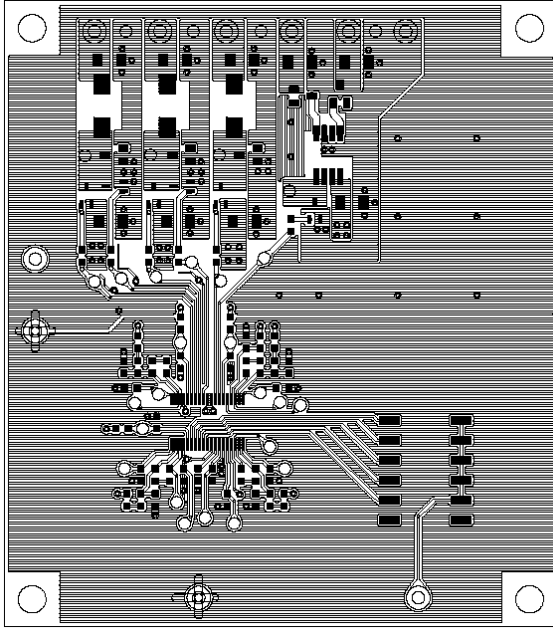
### **(2) Confirmation Method**

- \* Please turn on the power to VIN (power supply), make SW1 ON(Operation mode), and turn on SW2 to SW5 (output ON).  
IC operates normally if  $V_{o1}=1.8V(\text{Typ})$ ,  $V_{o2}=3.3V(\text{Typ})$ ,  $V_{o3}=5V(\text{Typ})$ ,  $V_{o4-1}=15V(\text{Typ})$ , and  $V_{o4-2}=-15V(\text{Typ})$  are output.
- \* Please confirm each output referring to various setting etc. of the attached paper.

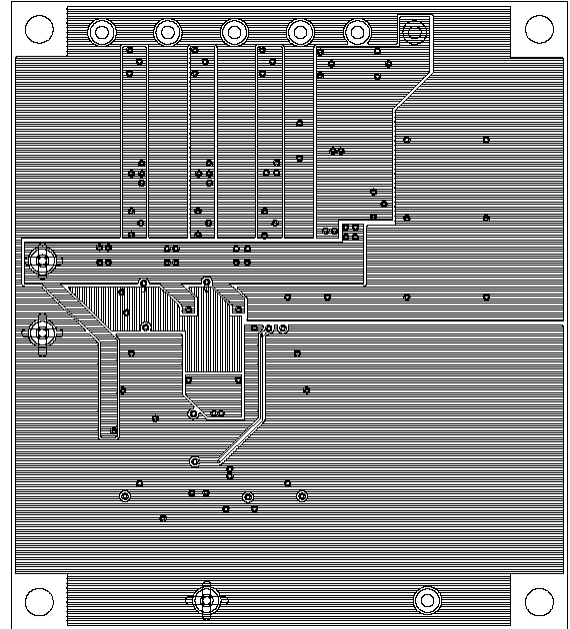
## 5. Parts Layout Block



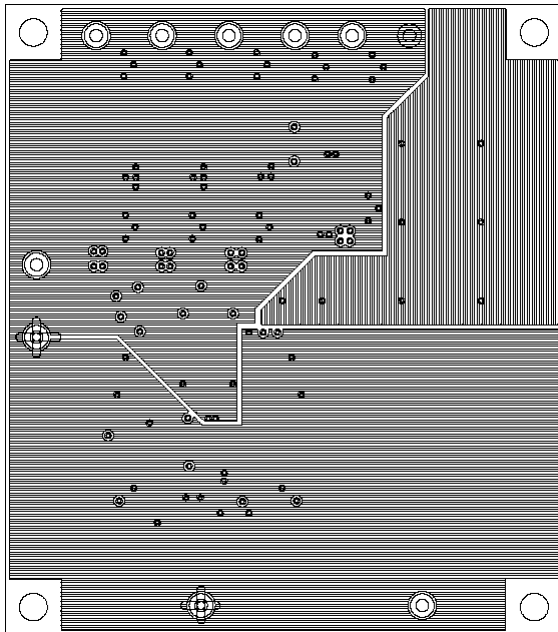
### Board Layout



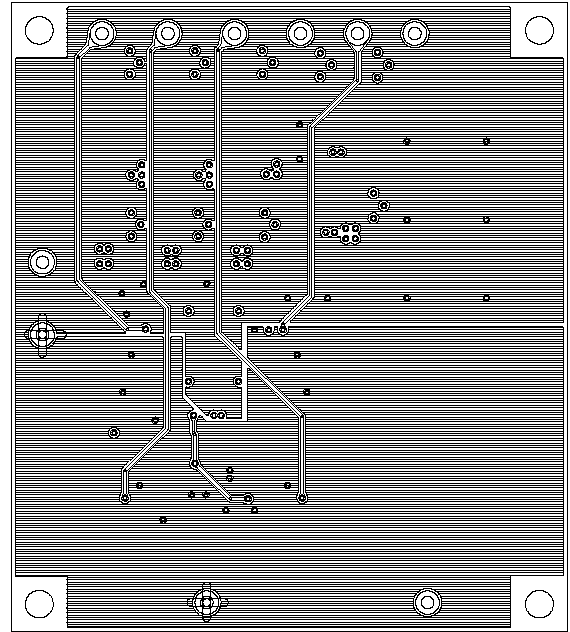
Top Side



Inside VIN & GND(Layer 2)

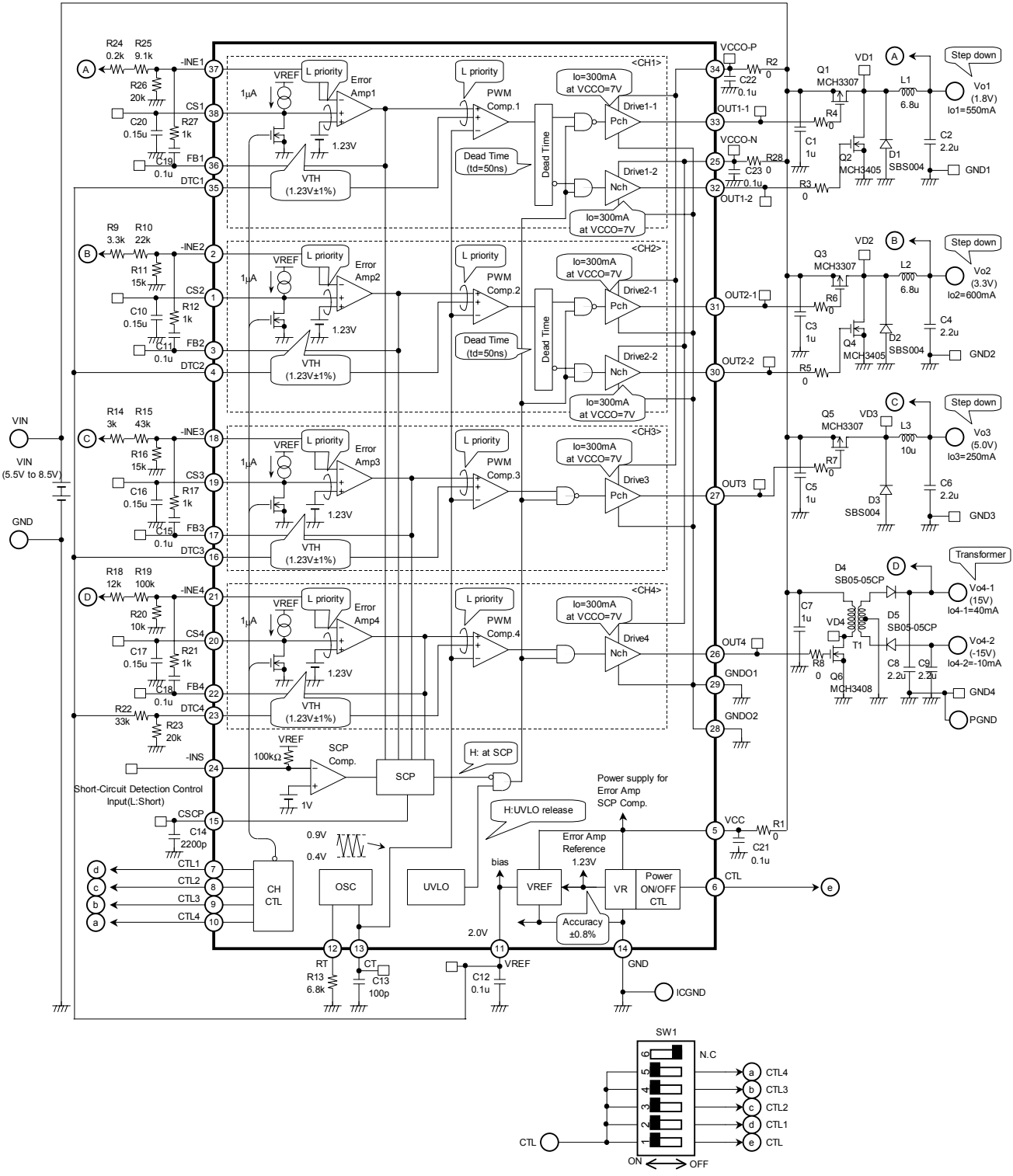


Inside GND(Layer 3)



Bottom Side

# 6. Circuit Diagram



It is IC operation, and a state of all channel ON in the above figure.



## 7. Circuit Parts List

No.	Component (Circuit diagram mark)	Item	Parts No.	Specification						Package	Vendor	Remark
				Rated1	Rated2	Rated3	Value	Deviation	Characteristic			
1	M1	IC	MB39A110PFT	-	-	-	-	-	-	FPT-38P-M03	FUJITSU	
2	Q1	Pch FET	MCH3307	PD=0.8W	VGSS=10V	ID=1.0A	-	-	-	MCPH3	SANYO	
3	Q2	Nch FET	MCH3405	PD=0.8W	VGSS=10V	ID=1.8A	-	-	-	MCPH3	SANYO	
4	Q3	Pch FET	MCH3307	PD=0.8W	VGSS=10V	ID=1.0A	-	-	-	MCPH3	SANYO	
5	Q4	Nch FET	MCH3405	PD=0.8W	VGSS=10V	ID=1.8A	-	-	-	MCPH3	SANYO	
6	Q5	Pch FET	MCH3307	PD=0.8W	VGSS=10V	ID=1.0A	-	-	-	MCPH3	SANYO	
7	Q6	Nch FET	MCH3408	PD=0.8W	VGSS=20V	ID=1.4A	-	-	-	MCPH3	SANYO	
8	D1	SBD	SBS004	IF(AV)=1A	VRRM=15V	-	-	-	-	SOT-23	SANYO	
9	D2	SBD	SBS004	IF(AV)=1A	VRRM=15V	-	-	-	-	SOT-23	SANYO	
10	D3	SBD	SBS004	IF(AV)=1A	VRRM=15V	-	-	-	-	SOT-23	SANYO	
11	D4	SBD	SB05-05CP	IF(AV)=0.5A	VRRM=50V	-	-	-	-	SOT-23	SANYO	
12	D5	SBD	SB05-05CP	IF(AV)=0.5A	VRRM=50V	-	-	-	-	SOT-23	SANYO	
13	L1	Inductor	RLF5018T-6R8M1R1	IDC1=1.1A	IDC2=1.4A	-	6.8u	±20%	RDC=47mΩ	-	TDK	
14	L2	Inductor	RLF5018T-6R8M1R1	IDC1=1.1A	IDC2=1.4A	-	6.8u	±20%	RDC=47mΩ	-	TDK	
15	L3	Inductor	RLF5018T-100MR94	IDC1=0.94A	IDC2=1.3A	-	10u	±20%	RDC=56mΩ	-	TDK	
16	T1	Transformer	CLQ52 5388-T139	-	-	-	-	-	-	-	SUMIDA	
17	C1	Ceramic Capacitor	C3216JB1E105K	25V	-	-	1u	±10%	B Characteristic	3216	TDK	
18	C2	Ceramic Capacitor	C3216JB1E225K	25V	-	-	2.2u	±10%	B Characteristic	3216	TDK	
19	C3	Ceramic Capacitor	C3216JB1E105K	25V	-	-	1u	±10%	B Characteristic	3216	TDK	
20	C4	Ceramic Capacitor	C3216JB1E225K	25V	-	-	2.2u	±10%	B Characteristic	3216	TDK	
21	C5	Ceramic Capacitor	C3216JB1E105K	25V	-	-	1u	±10%	B Characteristic	3216	TDK	
22	C6	Ceramic Capacitor	C3216JB1E225K	25V	-	-	2.2u	±10%	B Characteristic	3216	TDK	
23	C7	Ceramic Capacitor	C3216JB1E105K	25V	-	-	1u	±10%	B Characteristic	3216	TDK	
24	C8	Ceramic Capacitor	C3216JB1E225K	25V	-	-	2.2u	±10%	B Characteristic	3216	TDK	
25	C9	Ceramic Capacitor	C3216JB1E225K	25V	-	-	2.2u	±10%	B Characteristic	3216	TDK	
26	C10	Ceramic Capacitor	C1608JB1C154K	25V	-	-	0.15u	±10%	B Characteristic	1608	TDK	
27	C11	Ceramic Capacitor	C3216JB1E225K	25V	-	-	2.2u	±10%	B Characteristic	3216	TDK	
28	C11	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
29	C12	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
30	C13	Ceramic Capacitor	C1608CH1H101J	50V	-	-	100p	±5%	CH Characteristic	1608	TDK	
31	C14	Ceramic Capacitor	C1608JB1H222K	50V	-	-	2200p	±10%	B Characteristic	1608	TDK	
32	C15	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
33	C16	Ceramic Capacitor	C1608JB1C154K	25V	-	-	0.15u	±10%	B Characteristic	1608	TDK	
34	C17	Ceramic Capacitor	C1608JB1C154K	25V	-	-	0.15u	±10%	B Characteristic	1608	TDK	
35	C18	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
36	C19	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
37	C20	Ceramic Capacitor	C1608JB1C154K	25V	-	-	0.15u	±10%	B Characteristic	1608	TDK	
38	C21	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
39	C22	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	
40	C23	Ceramic Capacitor	C1608JB1H104K	50V	-	-	0.1u	±10%	B Characteristic	1608	TDK	

< Continued >

< Continued >

No.	Component (Circuit diagram mark)	Item	Parts No.	Specification						Package	Vendor	Remark
				Rated1	Rated2	Rated3	Value	Deviation	Characteristic			
41	R1	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
42	R2	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
43	R3	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
44	R4	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
45	R5	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
46	R6	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
47	R7	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
48	R8	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
49	R9	Resistor	RR0816P-332-D	1/16W	-	-	3.3kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
50	R10	Resistor	RR0816P-223-D	1/16W	-	-	22kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
51	R11	Resistor	RR0816P-153-D	1/16W	-	-	15kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
52	R12	Resistor	RR0816P-102-D	1/16W	-	-	1kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
53	R13	Resistor	RR0816P-682-D	1/16W	-	-	6.8kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
54	R14	Resistor	RR0816P-302-D	1/16W	-	-	3kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
55	R15	Resistor	RR0816P-433-D	1/16W	-	-	43kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
56	R16	Resistor	RR0816P-153-D	1/16W	-	-	15kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
57	R17	Resistor	RR0816P-102-D	1/16W	-	-	1kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
58	R18	Resistor	RR0816P-123-D	1/16W	-	-	12kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
59	R19	Resistor	RR0816P-104-D	1/16W	-	-	100kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
60	R20	Resistor	RR0816P-103-D	1/16W	-	-	10kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
61	R21	Resistor	RR0816P-102-D	1/16W	-	-	1kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
62	R22	Resistor	RR0816P-333-D	1/16W	-	-	33kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
63	R23	Resistor	RR0816P-203-D	1/16W	-	-	20kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
64	R24	Resistor	RR0816P-201-D	1/16W	-	-	200Ω	±0.5%	±25ppm/°C	1608	SUSUMU	
65	R25	Resistor	RR0816P-912-D	1/16W	-	-	9.1kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
66	R26	Resistor	RR0816P-203-D	1/16W	-	-	20kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
67	R27	Resistor	RR0816P-102-D	1/16W	-	-	1kΩ	±0.5%	±25ppm/°C	1608	SUSUMU	
68	R28	Jumper	RK73Z1J	1A	-	-	0 Ω	max 50mΩ	-	1608	KOA	
69	SW1	DIP SW	DMS-6H	-	-	-	-	-	-	-	MATSUKYU	
70	PIN	Wiring terminals	WT-2-1	-	-	-	-	-	-	-	Mac-Eight	

## **8. Initialization**

### **(1) Output voltage setting**

CH1

$$V_{o1} \text{ (V)} = 1.23 / R26 \times (R24 + R25 + R26) \cong 1.8 \text{ (V)}$$

CH2

$$V_{o2-2} \text{ (V)} = 1.23 / R11 \times (R9 + R10 + R11) \cong 3.3 \text{ (V)}$$

CH3

$$V_{o3-2} \text{ (V)} = 1.23 / R16 \times (R14 + R15 + R16) \cong 5.0 \text{ (V)}$$

CH4

$$V_{o4} \text{ (V)} = 1.23 / R20 \times (R18 + R19 + R20) \cong 15 \text{ (V)}$$

### **(2) Oscillation frequency**

$$f_{osc} \text{ (kHz)} = 693600 / (C13(\text{pF}) \times R13(\text{k}\Omega)) \cong 1.02 \text{ (MHz)}$$

### **(3) Soft-start time**

CH1

$$t_s \text{ (s)} = 1.23 \times C20 \text{ (\mu F)} \cong 185 \text{ (ms)}$$

CH2

$$t_s \text{ (s)} = 1.23 \times C10 \text{ (\mu F)} \cong 185 \text{ (ms)}$$

CH3

$$t_s \text{ (s)} = 1.23 \times C16 \text{ (\mu F)} \cong 185 \text{ (ms)}$$

CH4

$$t_s \text{ (s)} = 1.23 \times C17 \text{ (\mu F)} \cong 185 \text{ (ms)}$$

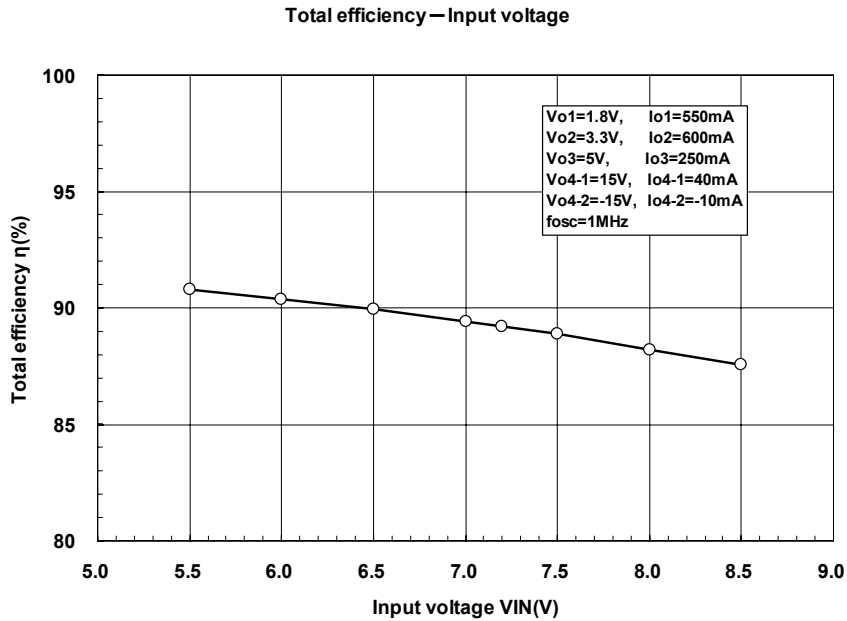
### **(4) Short-circuit detection time**

$$t_{scp} \text{ (s)} = 0.70 \times C14 \text{ (\mu F)} \cong 1.54 \text{ (ms)}$$

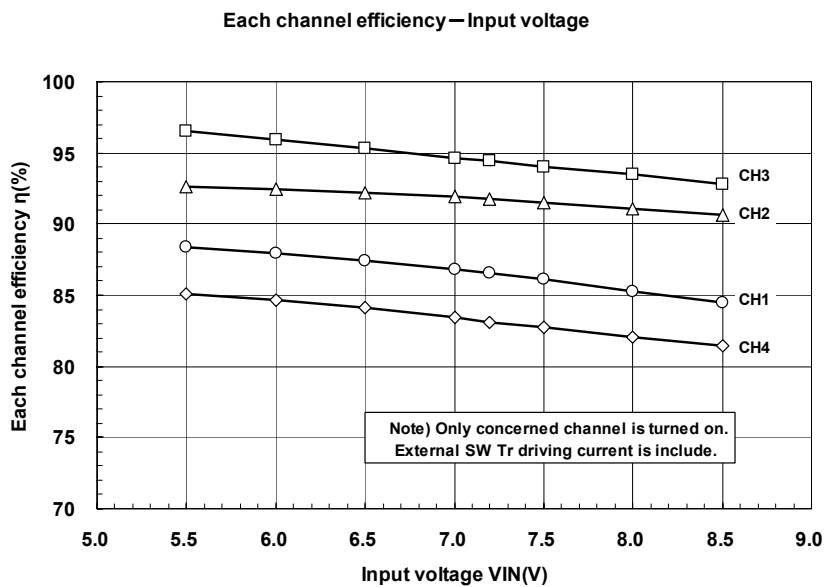
## 9. Reference Data

### (1) Conversion efficiency – Input voltage

#### Total efficiency

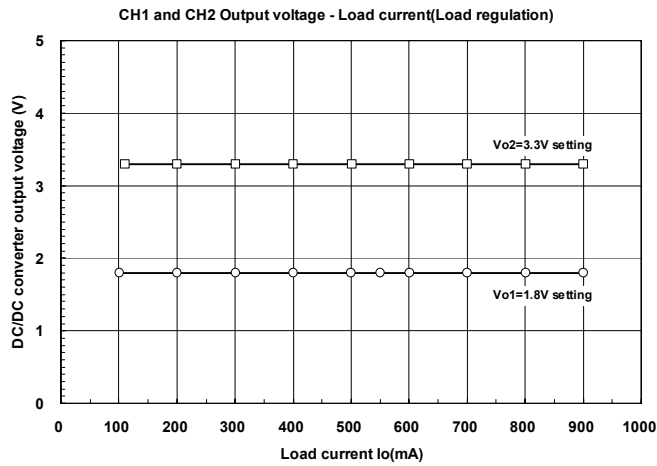


#### Each channel efficiency

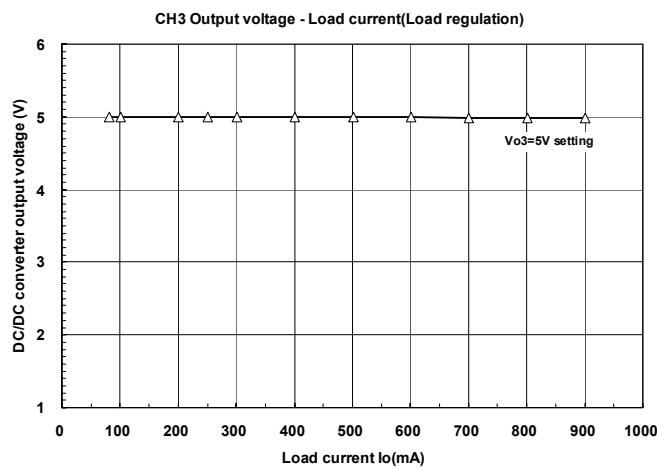


**(2) Load regulation ( $V_{IN}=3.6V$ )**

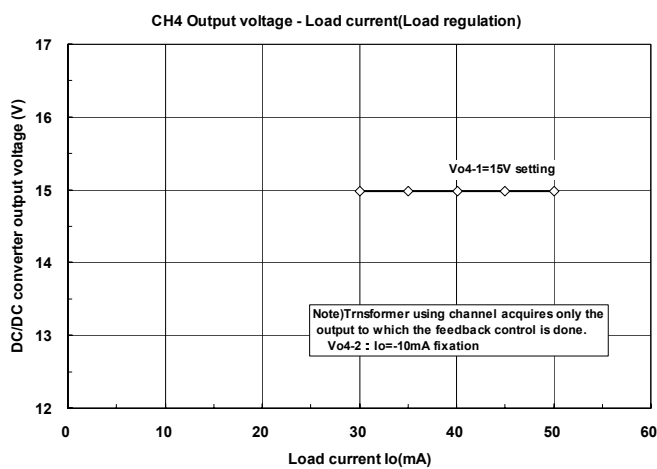
**CH1,CH2**



**CH3**

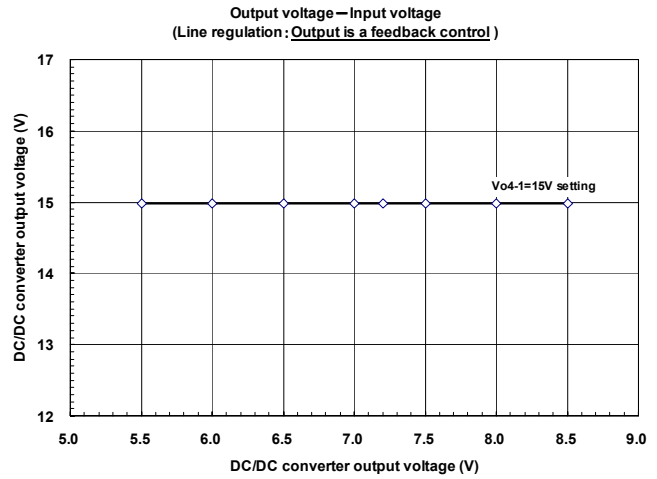
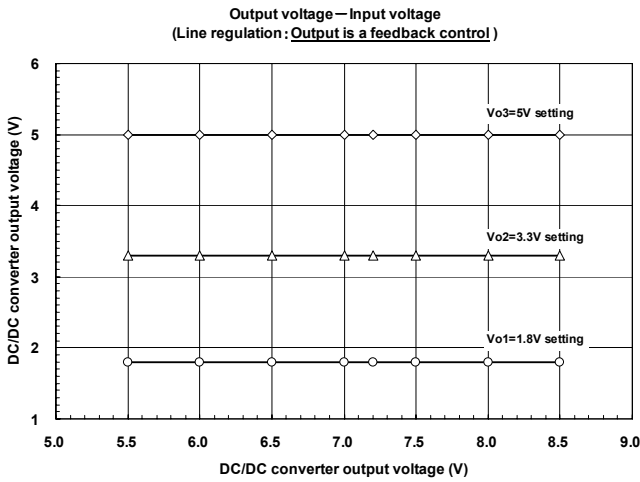


**CH4**

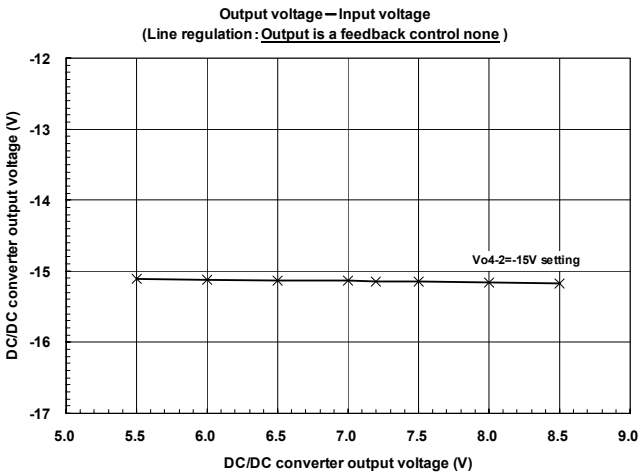


**(3) Line regulation**

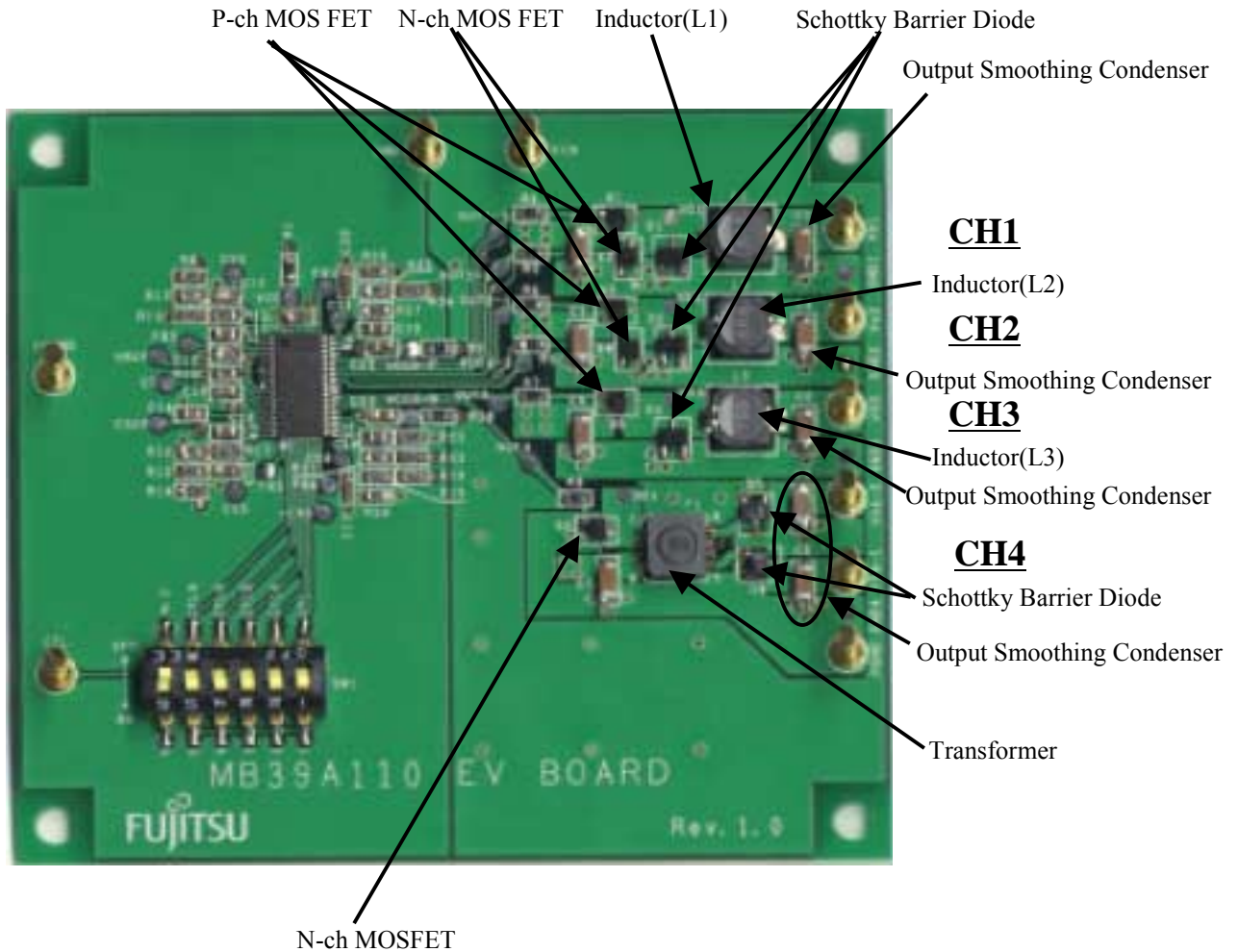
**Output is a feedback control.**



**Output is a feedback control none.**



## 10. Parts Select Method



Board Photograph

The parts selection method is written in the following.

**CH1 : 1.8V output(Down conversion)**

$V_{IN(Max)}=8.5V$ ,  $I_o=730mA$ ,  $f_{osc}=1MHz$

1. P-ch MOS FET(MCH3307(SANYO) )

$V_{DS}=-20V$ ,  $V_{GS}= \pm 10V$ ,  $I_D=-1A$ ,  $R_{DS(on)}=500m\Omega(Max)$ ,  $Q_g=1.5nC$

N-ch MOS FET(MCH3405(SANYO) )

$V_{DS}=20V$ ,  $V_{GS}= \pm 10V$ ,  $I_D=1.8A$ ,  $R_{DS(on)}=210m\Omega(Max)$ ,  $Q_g=4.5nC$

Drain current : Peak value

The peak value of the drain current of FET should be in the rated current value of FET.

When the peak value of the drain current of FET is assumed to be  $I_D$ ,  $I_D$  is obtained by the following formula.

Main side

$$I_D \geq I_o + \frac{V_{IN}-V_o}{2L} \text{ton} \quad * \left( \begin{array}{l} V_o = V_{IN} \times \frac{\text{ton}}{t} \\ \text{ton} = t \times \frac{V_o}{V_{IN}} = \frac{1}{f_{osc}} \times \frac{V_o}{V_{IN}} \end{array} \right)$$

$$\geq 0.73 + \frac{8.5-1.8}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.212$$

$$\geq \underline{0.83A}$$

Synchronous rectification side

$$I_D \geq I_o + \frac{V_o}{2L} \text{toff}$$

$$\geq 0.73 + \frac{1.8}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times (1-0.212)$$

$$\geq \underline{0.83A}$$



### Drain-source voltage and gate-source voltage

Source-drain voltage and gate-source voltage of FET should be in the rated voltage value of FET.

When the source-drain voltage of FET is assumed to be  $V_{DS}$ , and the gate-source voltage is assumed to be  $V_{GS}$ ,  $V_{DS}$  and  $V_{GS}$  are obtained by the following formula.

#### Main side

$$\begin{aligned} V_{DS} &\leq -V_{IN(\text{Max})} \\ &\leq -8.5\text{V} \end{aligned}$$

$$\begin{aligned} V_{GS} &\leq V_{IN(\text{Max})} \\ &\leq -8.5\text{V} \end{aligned}$$

#### Synchronous rectification side

$$\begin{aligned} V_{DS} &\geq V_{IN(\text{Max})} \\ &\geq 8.5\text{V} \end{aligned}$$

$$\begin{aligned} V_{GS} &\geq V_{IN(\text{Max})} \\ &\geq 8.5\text{V} \end{aligned}$$

2. Inductor (L1 : RLF5018T-6R8M1R1 : TDK)

6.8μH(tolerance : ±20%), rated current = 1.1A

The condition of L because of a continuous current in the range of the use voltage

$$\begin{aligned} L &\geq \frac{V_{IN}-V_o}{2I_o} \text{ton} \\ &\geq \frac{8.5-1.8}{2 \times 0.11} \times \frac{1}{1000 \times 10^3} \times 0.212 \\ &\geq \underline{\underline{6.45\mu\text{H}}} \end{aligned}$$

Load current value which becomes continuous current condition.

$$\begin{aligned} I_o &\geq \frac{V_o}{2L} \text{toff} \\ &\geq \frac{1.8}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times (1-0.212) \\ &\geq \underline{\underline{104.3\text{mA}}} \end{aligned}$$

Inductor current : peak value

The peak value of the inductor current should be in the rated current value of the inductor.

When the peak value of the inductor current is assumed to be  $I_L$ ,  $I_L$  is obtained by the following formula.

$$\begin{aligned} I_L &\geq I_o + \frac{V_{IN}-V_o}{2L} \text{ton} \\ &\geq 0.73 + \frac{8.5-1.8}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.212 \\ &\geq \underline{\underline{0.83\text{A}}} \end{aligned}$$

Inductor current : peak to peak value

When the peak to peak value of the inductor current is assumed to be  $\Delta I_L$ ,  $\Delta I_L$  is obtained by the following formula.

$$\begin{aligned} \Delta I_L &= \frac{V_{IN}-V_o}{L} \text{ton} \\ &= \frac{8.5-1.8}{6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.212 \\ &\cong \underline{\underline{208.9\text{mA}}} \end{aligned}$$

**CH2 : 3.3V output(Down conversion)**

$V_{IN(Max)}=8.5V$ ,  $I_o=680mA$ ,  $f_{osc}=1MHz$

1. P-ch MOS FET(MCH3307(SANYO) )

$V_{DS}=-20V$ ,  $V_{GS}= \pm 10V$ ,  $I_D=-1A$ ,  $R_{DS(on)}=500m\Omega(Max)$ ,  $Q_g=1.5nC$

N-ch MOS FET(MCH3405(SANYO) )

$V_{DS}=20V$ ,  $V_{GS}= \pm 10V$ ,  $I_D=1.8A$ ,  $R_{DS(on)}=210m\Omega(Max)$ ,  $Q_g=4.5nC$

Drain current : Peak value

The peak value of the drain current of FET should be in the rated current value of FET.

When the peak value of the drain current of FET is assumed to be  $I_D$ ,  $I_D$  is obtained by the following formula.

Main side

$$I_D \geq I_o + \frac{V_{IN}-V_o}{2L} \cdot ton$$

$$\geq 0.68 + \frac{8.5-3.3}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.388$$

$$\geq \underline{0.83A}$$

\*)

$$\left( \begin{array}{l} V_o = V_{IN} \times \frac{ton}{t} \\ ton = t \times \frac{V_o}{V_{IN}} = \frac{1}{f_{osc}} \times \frac{V_o}{V_{IN}} \end{array} \right)$$

Synchronous rectification side

$$I_D \geq I_o + \frac{V_o}{2L} \cdot toff$$

$$\geq 0.68 + \frac{3.3}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times (1-0.388)$$

$$\geq \underline{0.83A}$$

### Drain-source voltage and gate-source voltage

Source-drain voltage and gate-source voltage of FET should be in the rated voltage value of FET.

When the source-drain voltage of FET is assumed to be  $V_{DS}$ , and the gate-source voltage is assumed to be  $V_{GS}$ ,  $V_{DS}$  and  $V_{GS}$  are obtained by the following formula.

#### Main side

$$\begin{aligned} V_{DS} &\leq -V_{IN(Max)} \\ &\leq -8.5V \end{aligned}$$

$$\begin{aligned} V_{GS} &\leq V_{IN(Max)} \\ &\leq -8.5V \end{aligned}$$

#### Synchronous rectification side

$$\begin{aligned} V_{DS} &\geq V_{IN(Max)} \\ &\geq 8.5V \end{aligned}$$

$$\begin{aligned} V_{GS} &\geq V_{IN(Max)} \\ &\geq 8.5V \end{aligned}$$

2. Inductor (L2 : RLF5018T-6R8M1R1 : TDK)

6.8μH(tolerance : ±20%), rated current = 1.1A

The condition of L because of a continuous current in the range of the use voltage

$$\begin{aligned}
 L &\geq \frac{V_{IN}-V_o}{2I_o} \text{ton} \\
 &\geq \frac{8.5-3.3}{2 \times 0.15} \times \frac{1}{1000 \times 10^3} \times 0.388 \\
 &\geq \underline{\underline{6.72\mu\text{H}}}
 \end{aligned}$$

Load current value which becomes continuous current condition.

$$\begin{aligned}
 I_o &\geq \frac{V_o}{2L} \text{toff} \\
 &\geq \frac{3.3}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times (1-0.388) \\
 &\geq \underline{\underline{148.5\text{mA}}}
 \end{aligned}$$

Inductor current : peak value

The peak value of the inductor current should be in the rated current value of the inductor.

When the peak value of the inductor current is assumed to be  $I_L$ ,  $I_L$  is obtained by the following formula.

$$\begin{aligned}
 I_L &\geq I_o + \frac{V_{IN}-V_o}{2L} \text{ton} \\
 &\geq 0.68 + \frac{8.5-3.3}{2 \times 6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.388 \\
 &\geq \underline{\underline{0.83\text{A}}}
 \end{aligned}$$

Inductor current : peak to peak value

When the peak to peak value of the inductor current is assumed to be  $\Delta I_L$ ,  $\Delta I_L$  is obtained by the following formula.

$$\begin{aligned}
 \Delta I_L &= \frac{V_{IN}-V_o}{L} \text{ton} \\
 &= \frac{8.5-3.3}{6.8 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.388 \\
 &\cong \underline{\underline{296.7\text{mA}}}
 \end{aligned}$$

**CH3 : 5.0V output(Down conversion)**

$V_{IN(Max)}=8.5V$ ,  $I_o=730mA$ ,  $f_{osc}=1MHz$

1. P-ch MOS FET(MCH3307(SANYO) )

$V_{DS}=-20V$ ,  $V_{GS}=\pm 10V$ ,  $I_D=-1A$ ,  $R_{DS(on)}=500m\Omega(Max)$ ,  $Q_g=1.5nC$

Drain current : Peak value

The peak value of the drain current of FET should be in the rated current value of FET.

When the peak value of the drain current of FET is assumed to be  $I_D$ ,  $I_D$  is obtained by the following formula.

$$I_D \geq I_o + \frac{V_{IN}-V_o}{2L} \cdot t_{on} \quad *) \left( \begin{array}{l} V_o = V_{IN} \times \frac{t_{on}}{t} \\ t_{on} = t \times \frac{V_o}{V_{IN}} = \frac{1}{f_{osc}} \times \frac{V_o}{V_{IN}} \end{array} \right)$$

$$\geq 0.73 + \frac{8.5-5.0}{2 \times 10 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.588$$

$$\geq \underline{\underline{0.83A}}$$

Drain-source voltage and gate-source voltage

Source-drain voltage and gate-source voltage of FET should be in the rated voltage value of FET.

When the source-drain voltage of FET is assumed to be  $V_{DS}$ , and the gate-source voltage is assumed to be  $V_{GS}$ ,  $V_{DS}$  and  $V_{GS}$  are obtained by the following formula.

Main side

$$V_{DS} \leq -V_{IN(Max)}$$

$$\leq -8.5V$$

$$V_{GS} \leq V_{IN(Max)}$$

$$\leq 8.5V$$

2. Inductor (L3 : RLF5018T-100MR94 : TDK)

10μH(tolerance : ±20%), rated current = 0.94A

The condition of L because of a continuous current in the range of the use voltage

$$\begin{aligned}
 L &\geq \frac{V_{IN}-V_o}{2I_o} \text{ton} \\
 &\geq \frac{8.5-5.0}{2 \times 0.11} \times \frac{1}{1000 \times 10^3} \times 0.588 \\
 &\geq \underline{\underline{9.36\mu H}}
 \end{aligned}$$

Load current value which becomes continuous current condition.

$$\begin{aligned}
 I_o &\geq \frac{V_o}{2L} \text{toff} \\
 &\geq \frac{5.0}{2 \times 10 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times (1-0.588) \\
 &\geq \underline{\underline{103.0mA}}
 \end{aligned}$$

Inductor current : peak value

The peak value of the inductor current should be in the rated current value of the inductor.

When the peak value of the inductor current is assumed to be  $I_L$ ,  $I_L$  is obtained by the following formula.

$$\begin{aligned}
 I_L &\geq I_o + \frac{V_{IN}-V_o}{2L} \text{ton} \\
 &\geq 0.73 + \frac{8.5-5.0}{2 \times 10 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.588 \\
 &\geq \underline{\underline{0.83A}}
 \end{aligned}$$

Inductor current : peak to peak value

When the peak to peak value of the inductor current is assumed to be  $\Delta I_L$ ,  $\Delta I_L$  is obtained by the following formula.

$$\begin{aligned}
 \Delta I_L &= \frac{V_{IN}-V_o}{L} \text{ton} \\
 &= \frac{8.5-5.0}{10 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times 0.588 \\
 &\cong \underline{\underline{205.8mA}}
 \end{aligned}$$

### 3. Schottky Barrier Diode(SBS004:SANYO)

$$V_{RRM} = 15V, I_F = 1.0A, I_{FSM} = 10A, V_F = 0.35V$$

#### Diode current : Peak value

The peak value of the diode current should be in the rated current value of the diode.

When the peak value of the diode current is assumed to be  $I_{FSM}$ ,  $I_{FSM}$  is obtained by the following formula.

$$\begin{aligned} I_{FSM} &\geq I_o + \frac{V_o}{2L} \text{ toff} \\ &\geq 0.73 + \frac{5.0}{2 \times 10 \times 10^{-6}} \times \frac{1}{1000 \times 10^3} \times (1-0.588) \\ &\geq \underline{0.83A} \end{aligned}$$

#### Diode current : Average value

The average value of the diode current should be in the rated current value of the diode.

When the average value of the diode current is assumed to be  $I_F$ ,  $I_F$  is obtained by the following formula.

$$\begin{aligned} I_F &\geq I_o \times \frac{\text{toff}}{t} \\ &\geq 0.73 \times (1-0.588) \\ &\geq \underline{0.3A} \end{aligned}$$

#### Repetition peak reverse voltage

The repetition peak reverse voltage of the diode should be in the rated voltage value of the diode.

When the repetition peak reverse voltage of the diode is assumed to be  $V_{RRM}$ ,

$V_{RRM}$  is obtained by the following formula.

$$\begin{aligned} V_{RRM} &\geq V_{IN(\text{Max})} \\ &\geq \underline{8.5V} \end{aligned}$$



**CH4 : (Transformer conversion)**

$$\left\{ \begin{array}{lll} V_{IN(\text{Max})}=8.5\text{V} & V_{O4-1} = 15\text{V} & I_{O4-1} = 50\text{mA} \\ V_{IN(\text{Min})}=5.5\text{V} & V_{O4-2} = 5\text{V} & I_{O4-2} = -10\text{mA} \end{array} \right. ,$$

1. N-ch MOS FET(MCH3408(SANYO) )

$V_{DS}=30\text{V}$ ,  $V_{GS}= \pm 20\text{V}$ ,  $I_D=1.4\text{A}$ ,  $R_{DS(\text{on})}=300\text{m}\Omega(\text{Max})$ ,  $Q_g=2.5\text{nC}$

Ratings of the drain current of FET should be 0.4A or more.

Moreover, ratings of drain-source voltage and gate-source voltage of FET should be 16V or more.

2. Schottky Barrier Diode(SB05-05CP(SANYO))

$V_{RRM}=50\text{V}$ ,  $I_F=500\text{mA}$ ,  $I_{FSM}=5\text{A}$ ,

Ratings of the diode are  $V_{RRM}$  (repetition peak reverse voltage)= each 33V,  $I_F$  (average output current)=40mA, and should be  $I_{FSM}$  (surge forward current)=0.2A or more.

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use.

Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

**CAUTION:**

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.