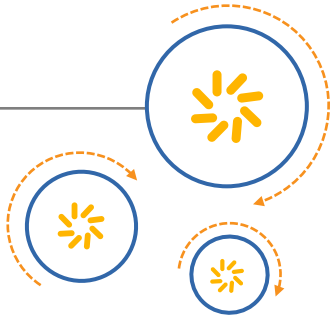
Qualcomm Technologies, Inc.



AR3002 Single Chip Bluetooth v4.0 UART HCI Data Sheet

September 2016

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

LM80-P0598-9 Rev B

Revision history

Revision	Date	Description
B	September 2016	Removed references to Qualcomm Atheros Section 1.1: changed the term ‘mobile applications’ to ‘embedding computing’ Section 1.1: Added two notes Table A-1: Added acronyms and definitions
A	June 1, 2015	Initial release

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1 Introduction

1.1 General description

The AR3002 from Qualcomm® Technologies, Inc. (QTI) is a highly integrated, all-CMOS, single chip Bluetooth™ 4.0+HS solution for mobile, embedded computing, and all other low power applications. It includes a Bluetooth EDR radio, a 32-bit CPU, HCI-UART interface, 1.2 V voltage regulator, and SRAM and ROM. It also has a standard WLAN coexistence and support for QTI proprietary next generation WLAN coexistence interface to ensure coexistence with WLAN devices co-located in the same system. The proprietary coexistence interface provides enhanced performance when paired with WLAN devices that support that interface. The AR3002 supports the standard HCI-UART interface so it is compatible with HCI upper layer Bluetooth stacks. It is also specially optimized for low-power applications. In some applications it is possible to use an on-chip one-time programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and BOM cost. The AR3002 provides mobile, embedded computing, and low-power devices ODM/OEMs with a cost effective Bluetooth solution available. The AR3002 comes in a 5x5 mm QFN package. A Bluetooth reference design is available for quick bring-up and validation.

A Bluetooth upper-layer stack is available through QTI, which supports Blue-Z profiles.

NOTE: This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE: Enabling some features may require additional licensing fees.

1.2 AR3002 features

- Single-chip Bluetooth v4.0 solution
- Bluetooth low energy dual mode radio
- Supports both Class-2 (up to +4 dBm) and Class-1 (up to +10 dBm) operation
- Standard HS-UART HCI interface
- 1.2 V linear voltage regulator (LDO)
- Integrated 32-bit CPU with 128 Kb data RAM and 512 Kb program ROM
- On-chip low power oscillator (LPO)
- On-chip one-time programmable (OTP) memory
- WLAN coexistence interface
- Audio CODEC using PCM interface

- Compatible with standard reference external clock of 19.2 MHz, 26 MHz, and 40 MHz
- 5x5 mm 40-pin QFN package

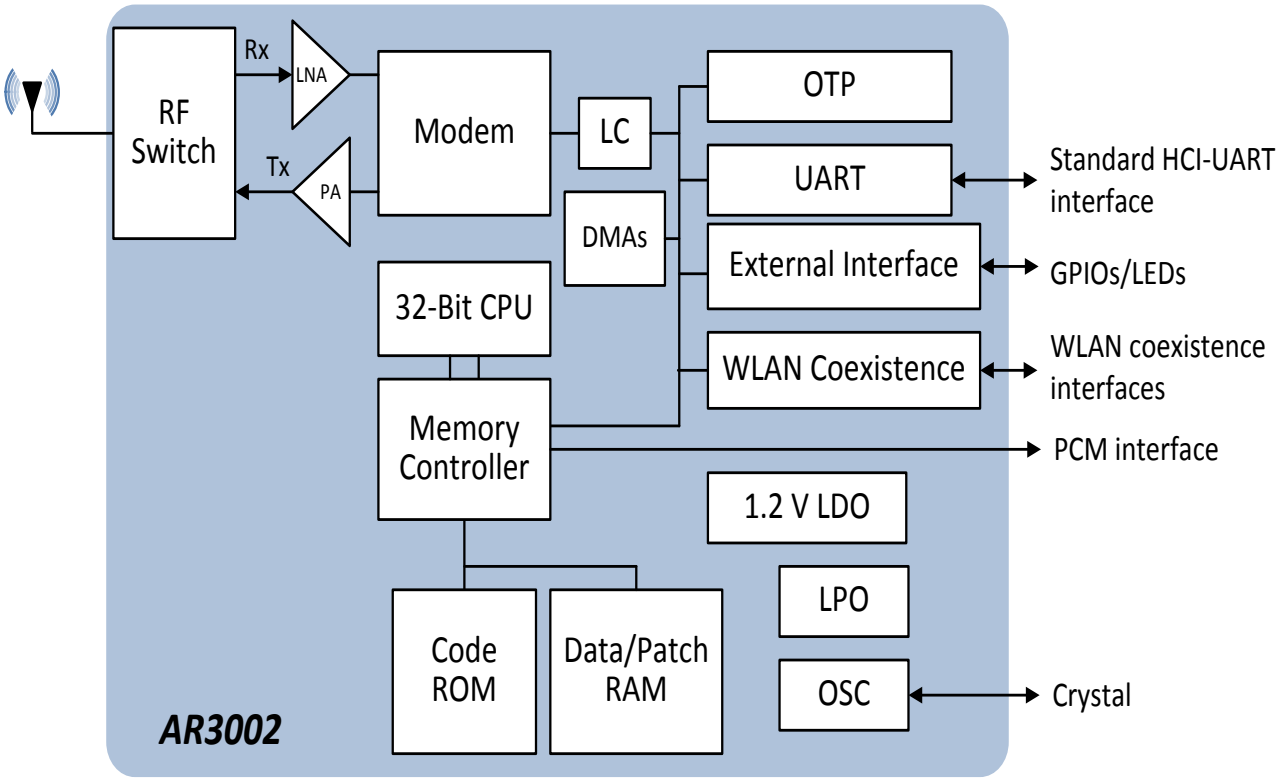

Figure 1-1 AR3002 block diagram

2 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions. The nomenclature listed in Table 2-1 is used for signal types described in Table 2-2:

Table 2-1 Pin types

Type	Description
IA	Analog input signal
I	Digital input signal
I/O	Digital bidirectional signal
OA	Analog output signal
O	Digital output signal
P	Power or ground signal

Figure 2-1 shows the pinout for the AR3002.

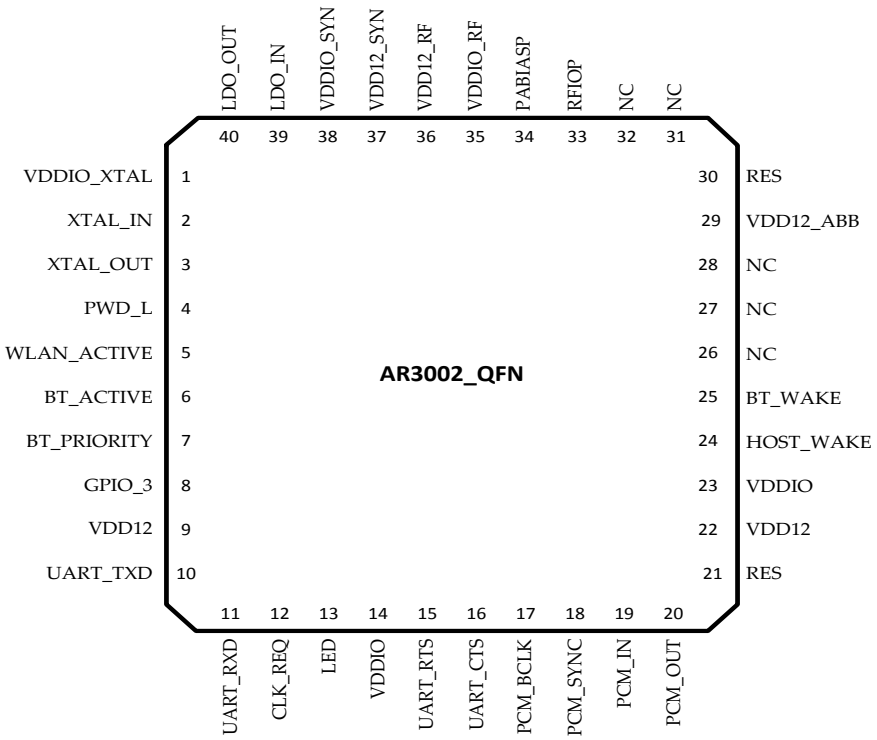

Figure 2-1 AR3002 pinouts

Table 2-2 lists and describes the signal-to-pin relationship information for the AR3002.

Table 2-2 Signal-to-pin relationships and descriptions

Symbol	Pin	Type	Description
Radio Interface			
PABIASP	34	P	Power amplifier bias for RF output power.
PWD_L	4	IA	Chip power-down control; driving this pin low powers down the chip. Belongs to VDDIO_XTAL power domain.
RFIOP	33	IA/OA	RF In/Out.
Clock			
CLK_REQ	12	O	When a reference clock is connected to XTAL_OUT, this pin asserts when the AR3002 requires the reference clock. This clock must be stable within 2 ms after the assertion of CLK_REQ.
Crystal			
XTAL_IN	2	I	Reference clock; can be 19.2 MHz, 26 MHz and 40 MHz. When used, XTAL_OUT should be connected to the reference clock and XTAL_IN should be grounded.
XTAL_OUT	3	I/O	
PCM			
PCM_BCLK	17	I/O	CODEC interface bit clock, input for slave, output for master. Leave as NC if PCM is not used.
PCM_IN	19	I	CODEC interface input data. Tie to VDDIO directly on board or pull-up internally if PCM is not used.
PCM_OUT	20	O	CODEC interface output data. Leave as NC if PCM is not used.
PCM_SYNC	18	I/O	CODEC interface synchronization control, input for slave, output for master. Leave as NC if PCM is not used.
UART			
UART_RXD	11	I	UART receive data.
UART_TXD	10	O	UART transmit data.
UART_CTS	16	I	UART clear_to_send.
UART_RTS	15	O	UART request_to_send.

Symbol	Pin	Type	Description
WLAN Coexistence			
BT_ACTIVE	6	O	If asserted, this signal indicates that BT requests access to the wireless medium to transmit or receive.
BT_PRIORITY	7	O	When asserted along with BT_ACTIVE, this signal indicates the device is transmitting or receiving with high priority.
WLAN_ACTIVE	5	I	Indicates medium busy from an external source; can be asserted (by a WLAN device) to prevent the AR3002 from transmitting a new frame.
GPIO			
HOST_WAKE	24	O	Wake up host. Leave as NC if not used.
BT_WAKE	25	I	Wake up BT. Leave as NC if not used.
GPIO_3	8	I/O	General purpose I/O pin. Leave as NC if not used.
LED	13	O	Status indication. Leave as NC if not used.
RES	21	-	Reserved. Tie to GND when not in use.
Power			
LDO_IN	39	P	LDO input.
LDO_OUT	40	P	LDO output.
VDD12	9, 22	P	Digital supply, should be connected to LDO_OUT pin on the board; all VDD12 pins should be connected on the board.
VDD12_ABB	29	P	Analog supply; all VDD12 pins should be connected on the board.
VDD12_RF	36	P	RF supply; all VDD12 pins should be connected on the board.
VDD12_SYN	37	P	SYN supply; all VDD12 pins should be connected on the board.
VDDIO	14, 23	P	Digital I/O voltage; all VDDIO pins should be connected on the board.
VDDIO_RF	35	P	RF voltage; all VDDIO pins should be connected on the board.
VDDIO_SYN	38	P	Synthesizer voltage; all VDDIO pins should be connected on the board.
VDDIO_XTAL	1	P	Crystal voltage; all VDDIO pins should be connected on the board.
GND_SLUG		—	Ground pad under chip.

Symbol	Pin	Type	Description
Reserved			
NC	26, 27, 28, 31, 32	—	No connection.
RES	30	—	Reserved as LNA2, which is Rx port separated from pin 33 RFIOP. Tie to GND when not in use.

Table 2-3 lists the GPIO status of the AR3002 (v2.2.1).

Table 2-3 GPIO status of AR3002 (v2.2.1)

Pin	Function	Power-on Default (no external pst/rampatch download)	Chip_PWD
17	PCM_BCLK	output low	input (pull up)[4]
18	PCM_SYNC	output low	input (pull up)
19	PCM_IN	input (no pull)	input (pull up)
20	PCM_OUT	output low	input (pull up)
10	UART_TXD	output high	input (pull up)
11	UART_RXD	input (no pull)	input (pull up)
16	UART_CTS	input (pull up)	input (pull up)
15	UART_RTS	output low	input (pull up)
5	WLAN_ACTIVE	input (pull down)[1]	input (pull down)
6	BT_ACTIVE	output low	input (pull down)
7	BT_PRIORITY	output low	input (pull down)
8	GPIO 3	output low	input (pull down)
24	HOST_WAKE	input (pull up)[2]	input (pull up)
25	BT_WAKE	input (pull up)	input (pull up)
13	LED	output high[3]	input (pull up)
12	CLK_REQ	output high	input (pull down)

1. For AR3002 2.2, Coex is disabled by default, and status for PIN5, PIN6, PIN7, and PIN8 when power is on, are input PINs (pull down). There is no other status difference between AR3002 2.2 and AR3002 2.2.1.
2. By default this function is disabled. When HOST_WAKE is enabled, it is configured as output.
3. LED function is enabled by default.
4. Pull-up, pull-down, and no-pull in this table all refer to status in AR3002, not on board.

Figure 2-2 shows the AR3002 schematic.

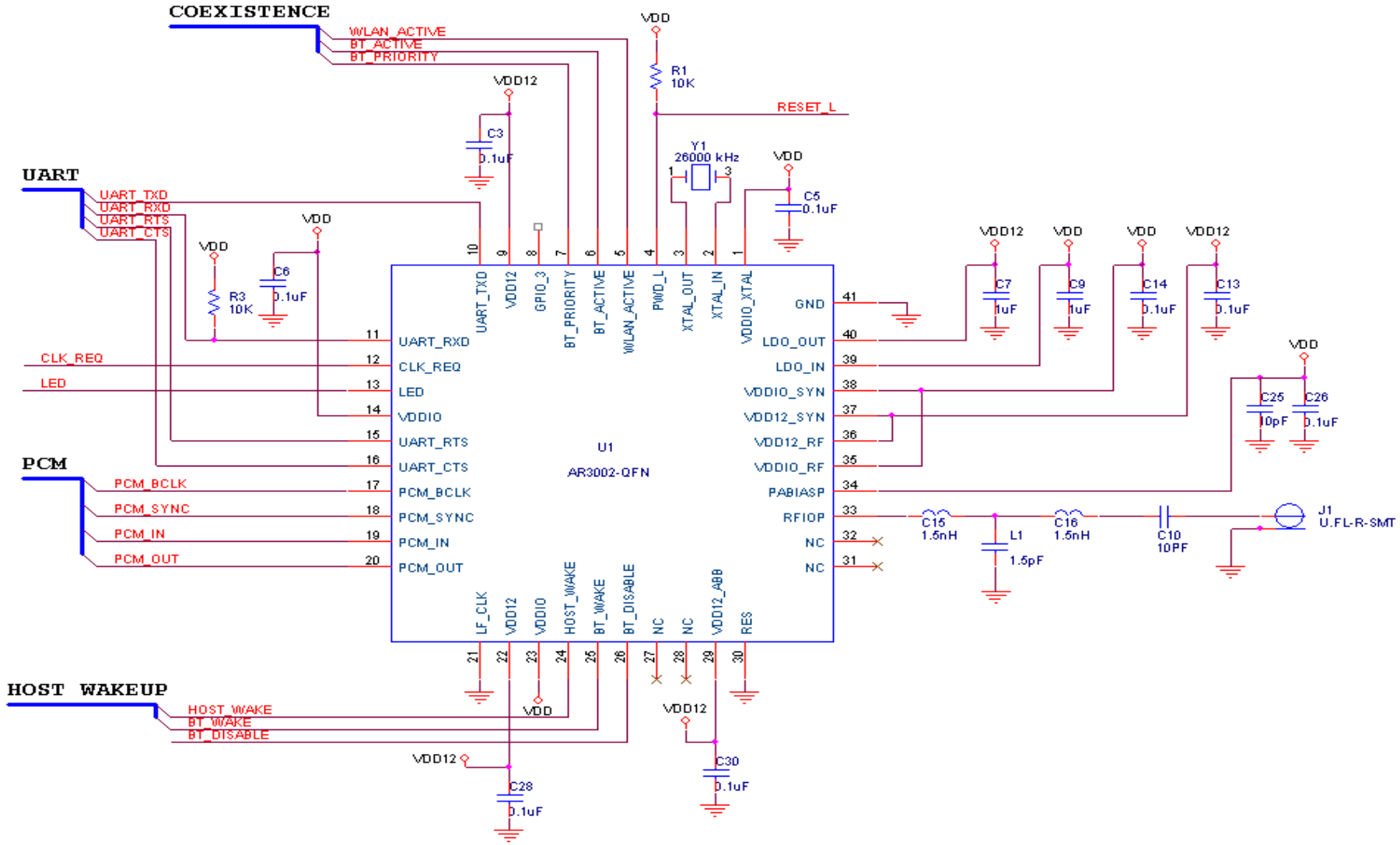

Figure 2-2 AR3002 schematic

3 Functional Description

3.1 HCI-UART interface

The UART interface is a standard high-speed UART interface, able to operate up to 4 Mbps, supporting Bluetooth HCI-UART interface.

3.2 PCM interface

A PCM interface to an external mono-audio CODEC is supported. The AR3002 supports CODECs such as: Winbond W681360, Wolfson WM8974, and Realtek ALC5620. The PCM supports the 8 KHz sample rate.

AR3002 can operate as the PCM interface master generating an output clock or configured as a PCM interface slave. It supports 13-bit, 16-bit, 8-bit, or 14-bit μ-law, A-law, or linear mono-sample formats.

3.3 CPU and memory

The AR3002 uses a 32-bit RISC core with five-stage pipelining and 16-bit and 24-bit instruction encoding. On startup, the AR3002 boots from the boot ROM. Software checks OTP first for configuration information. It then gets configuration from the host and proceeds to execute from on-chip ROM.

3.4 Standard WLAN coexistence

The AR3002 supports standard WLAN coexistence interfaces through the WLAN_ACTIVE, BT_PRIORITY, and BT_ACTIVE pins.

3.5 Reference clock

The AR3002 includes a fractional *N* PLL and supports an external crystal connected between the XTAL_IN and XTAL_OUT pins.

The crystal can use the 19.2 MHz, 26 MHz, and 40 MHz frequencies. The default is 26 MHz. A ± 20 ppm total accuracy across process, temperature, and aging is required for the external crystal.

When an external clock source is used, it should be connected to the XTAL_OUT pin, and the XTAL_IN pin should be grounded.

3.6 BT low energy

The AR3002 supports Low Energy (LE) specification, which allows for connection to devices with single mode LE function, for example, Watch, Sensor, and HID. The implementation is optimized for coexistence with WLAN.

3.7 Power management

These power interfaces exist in the AR3002: LDO_IN, LDO_OUT, VDD12, and VDDIO. Table 3-1 lists and describes the power management pins.

Table 3-1 Power management pins

Pins	Description
LDO_IN	The input to the internal LDO. The LDO_IN pin can be connected to a supply voltage between 1.6 V and 3.6 V.
LDO_OUT	The 1.2 V output from the internal LDO and should be connected to a 1.0 uF bypass capacitor.
VDD12	The core voltage which should be connected to the LDO_OUT pin. (Applies to all VDD12 pins)
VDDIO	The regulated I/O voltage. It can be 1.8 V or 3.3 V. All VDDIO pins should be connected on the board.

3.8 Reset

The pin PWD_L resets and powers down the AR3002.

Holding the PWD_L pin at GND turns off the entire chip and all state information is lost. All core supply voltages are internally gated off in this condition to minimize leakage.

The power-on-reset (POR) circuit detects a low-to-high transition on this pin and executes a reset after VDDIO and VDD12 are stabilized.

3.9 Radio

RFIOP is the RF port used both for Tx output and Rx input. For optimum RF performance, a matching network is required between the RF port and the antenna.

PABIASP is the bias pin for the internal PA and should be connected to the IO supply voltage (either 1.8 V or 3.3 V). A 10 pF bypass capacitor should be placed near PABIASP to provide an AC ground.

3.10 GPIO

A single output pin is provided to drive an indicator LED. This pin indicates Bluetooth activity and status.

3.11 OTP

Using One Time Programmable (OTP) memory can eliminate the need for an external EEPROM.

OTP programming needs 3.3 V (+5%) supply on VDDIO. Cannot program OTP using 1.8 V. OTP reading can be done with 3.3 V or 1.8 V supply on VDDIO.

4 Electrical Characteristics

4.1 Absolute maximum ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR3002 solution. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 4-1 Absolute maximum ratings

Symbol	Parameter	Max. Rating	Unit
LDO_IN	Input for LDO	3.6	V
VDD12	Core voltage	1.32	V
VDDIO	I/O supply voltage	3.6	V
PA_{bias}	Input for PA bias voltage	3.6	V
T_{store}	Storage temperature	125	°C
$T_{junction}$	Junction temperature	125	°C
ESD	Electrostatic discharge tolerance	± 2k	V

4.2 Recommended operating conditions

Table 4-2 Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PABIASP	PA bias V\voltage	—	1.6	1.8/3.3	3.6	V
LDO_IN	LDO Input	—	1.6	1.8/3.3	3.6	V
LDO_OUT[1]	LDO output	—	—	1.2	—	V
VDDIO	I/O supply voltage	—	1.6	1.8/3.3	3.6	V
T_{case}	Standard case temperature	—	–20	25	100	°C

1. VDD12 is the core voltage that should be connected to the LDO_OUT pin.

4.3 Radio receiver characteristics

Table 4-3 through Table 4-9 describe the basic rate transmitter performance, enhanced data transmitter performance, basic rate receiver performance, enhanced rate receiver performance, and current consumption conditions at 25°C.

Table 4-3 Basic rate transmitter performance temperature at 25°C (1.8 V)

Test Parameter	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF output power	0	3	10	0 to +20	dBm
RF power control range	32	34	36	≥ 16	dB
RF power control step size	3	4	5	2 ≤ Step Size ≤ 8	dB
Frequency range	2.4	—	2.4835	2.4 < f < 2.4835	GHz
20 dB bandwidth	—	950	—	≤ 1000	KHz
Adjacent channel TX power $F = F_0 \pm 2$ MHz	—	–49	—	≤ –20	dBm
Adjacent channel TX power $F = F_0 \pm 3$ MHz	—	–50	—	≤ –40	dBm
Δf1avg maximum modulation	—	164	—	140 < Δf1avg < 175	KHz
Δf2max minimum modulation	—	144	—	≥ 115	KHz
Δf2avg/Δf1avg	—	0.88	—	≥ 0.80	—
Initial carrier frequency	—	0	—	≤ ±75	KHz
Drift rate	—	0	—	≤ 20	KHz/50 µs
Drift (DH1 packet)	—	1	—	≤ 25	KHz
Drift (DH5 packet)	—	–1	—	≤ 40	KHz

Table 4-4 Enhanced rate transmitter performance temperature at 25°C (1.8 V)

Test Parameter	Min	Typ	Max	Bluetooth Specification	Unit
Relative transmit power		–2	0	0.5	–4 to +1
Max carrier frequency stability |wo|	π/4 DQPSK	—	0	—	≤ ±10
	8 DPSK	—	0	—	
Max carrier frequency stability |wi|	π/4 DQPSK	—	0	—	≤ ±75
	8 DPSK	—	0	—	
Max carrier frequency stability |w0+wi|	π/4 DQPSK	—	0	—	≤ ±75
	8 DPSK	—	0	—	
RMS DEVM	π/4 DQPSK	—	6	—	≤ 20
	8 DPSK	—	6	—	≤ 13
Peak DEVM	π/4 DQPSK	—	16	—	≤ 35
	8 DPSK	—	17	—	≤ 25
99% DEVM	π/4 DQPSK	—	99.9	—	99% ≤ 30
	8 DPSK	—	99.9	—	99% ≤ 20
EDR differential phase encoding		—	100	—	≥ 99
Adjacent channel power	F≥ ±3MHz	—	–42.5	—	< –40
	F = ± 2MHz	—	–39	—	≤ –20
	F = ±1MHz	—	–40	—	≤ –26

Table 4-5 Low energy transmitter performance

Test Parameter	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF output power	0	3	10	–20 to +10	dBm
Adjacent channel TX power $F = F_0 \pm 2$ MHz	—	–45	—	≤ –20	dBm
Adjacent channel TX power $F = F_0 \pm 3$ MHz	—	–55	—	≤ –30	dBm
Δf1avg maximum modulation	—	248	—	225 < Δf1avg < 275	KHz

Test Parameter	Min	Typ	Max	Bluetooth Specification	Unit
∆f2max minimum modulation	—	250	—	≥ 185	KHz
∆f2avg/∆f1avg	—	0.96	—	≥ 0.8	—
Initial carrier frequency offset	—	0	—	-150 to +150	KHz
Drift rate	—	0	—	≤ 20	KHz/50 µs
Drift ($\|f_0-f_n\|$)	—	0	—	≤ 50	KHz
Drift ($\|\|f_1-f_0\|$ & $\|f_n-f_{n-5}\|\|$)	—	0	—	≤ 20	KHz

Table 4-6 Basic rate receiver performance at 1.8 V

Test parameter	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity	BER ≤ 0.1%	—	–91	—	≤ –70
Maximum input	BER ≤ 0.1%	–20	—	—	≥ –20
Carrier-to-interferer ratio (C/I)	Co-channel	—	—	11	11
	Adjacent channel (±1 MHz)	—	—	0	0
	Second adjacent channel (± 2 MHz)	—	—	–30	–30
	Third adjacent channel (± 3 MHz)	—	—	–40	–40
Maximum level of intermodulation interferers		—	—	–39	< –39

Table 4-7 Enhanced data rate receiver performance 1.8 V

Test parameter	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity (BER ≤ 0.01%)	π/4 DQPSK	—	–92	—	≤ –70
	8 DPSK	—	–87	—	≤ –70
Maximum input (BER ≤ 0.1%)	π/4 DQPSK	–20	—	—	≥ –20
	8 DPSK	–20	—	—	≥ –20
	π/4 DQPSK	—	—	13	≤ ±13

Test parameter	Min	Typ	Max	Bluetooth specification	Unit
Co-channel C/I (BER ≤ 0.1%)	8 DPSK	—	—	20	≤ ± 20
Adjacent channel C/I (BER ≤ 0.1%)	π/4 DQPSK	—	—	0	≤ 0
	8 DPSK	—	—	5	≤ 5
Second adjacent channel C/I (BER ≤ 0.1%)	π/4 DQPSK	—	—	–30	≤ –30
	8 DPSK	—	—	–25	≤ –25
Third adjacent channel C/I (BER ≤ 0.1%)	π/4 DQPSK	—	—	–40	≤ –40
	8 DPSK	—	—	–33	≤ –33

Table 4-8 Low-energy receiver performance

Test parameter	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity	PER ≤ 30.8%	—	–95	—	≤ –70
Maximum input	PER ≤ 30.8%	–10	—	—	≥ –10
Carrier-to-interferer ratio (C/I)	Co-channel	—	—	21	21
	Adjacent channel (±1 MHz)	—	—	15	15
	Second adjacent channel (± 2 MHz)	—	—	-17	-17
	Third adjacent channel (± 3 MHz)	—	—	-27	-27
Maximum level of intermodulation interferers		—	—	-50	-50
Maximum level of blocker	30 – 2000 MHz	—	—	-30	-30
	2003 – 2399 MHz	—	—	-35	-35
	2484 – 2997 MHz	—	—	-35	-35
	3000 MHz – 12.75 GHz	—	—	-30	-30

Table 4-9 Power consumption

Mode for current consumption	Average value (mA)
Idle mode	0.093
Inquiry scan (1.28 sec)	0.498
Page scan (1.28 sec)	0.498
Page and Inq scan (1.28 sec)	0.903
ACL Sniff without scan (1.28 sec Interval, 2 Attempts)	0.119
ACL slave[1]	12.2
Inquiry	22.7
DH1 master	24.5
DH1 slave	23.5
DH5 master	33.0
DH5 slave	29.0
3DH1 master	25.8
3DH1 slave	26.5
3DH5 master[2]	34.5
3DH5 slave[3]	29.1
HV3 master	16.9
HV3 slave	18.6
2EV3 master	14.1
2EV3 slave	17.1
Tx-continuous (100% Duty cycle)[4]	49.0
Rx-continuous (100% Duty cycle)[5]	37.0
LE advertising (2048 slot interval)	0.28
LE scanning (continuous)	38.1
LE master (6 frame interval, 0 byte payload)	8.93

Mode for current consumption	Average value (mA)
LE master (12 frame interval, 0 byte payload)	6.45
LE master (228 frame interval, 0 byte payload)	0.62
LE master (6 frame interval, 27 byte payload)	12.19

1. ACL as slave means AR3002 is in a link (as slave) with another device, only minimum traffic to maintain link.
2. 3DH5 master: the AR3002 sends a 3DH5 packet to the slave, and the slave returns a null packet.
3. 3DH5 slave: the AR3002 receives a 3DH5 packet from the master and returns a null packet.
4. Average power during Tx burst.
5. Average power during Rx burst.

NOTE: Measurement conditions are 25 °C
Vin = 1.8 V, +0 dBm RF output power at the chip, UART baud rate is 3 Mbps for EDR and 1.5 Mbps for BDR.

5 Package Dimensions

5.1 Package dimensions

The AR3002 is packaged in a QFN package. The body size is 5 mm by 5 mm.

The package drawings, dimensions, and pinouts for QFN packages are provided in Figure 5-1 and Table 5-1. The package drawings, dimensions, and pinouts for SPD packages are provided in Figure 5-2 and Table 5-2.

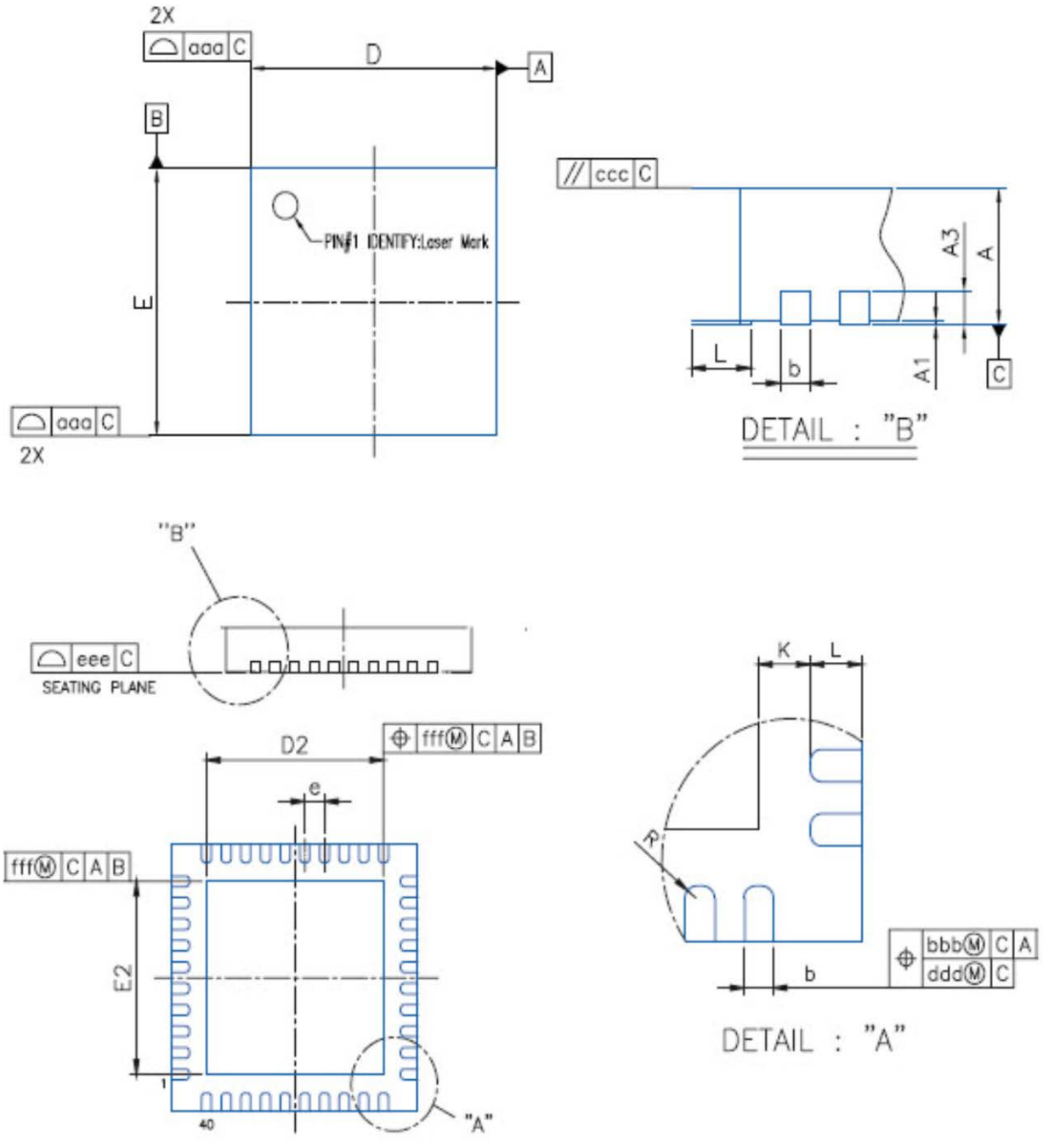

Figure 5-1 Package drawing – QFN

Table 5-1 Package dimensions - QFN

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A3	0.20 REF				0.008 REF			
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	4.90	5.00	5.10	mm	0.193	0.197	0.201	inches
D2/E2	3.45	3.60	3.75	mm	0.136	0.142	0.148	inches
e	0.40 BSC				0.016 BSC			
L	0.25	0.35	0.45	mm	0.010	0.014	0.018	inches
K	0.20	—	—	mm	0.008	—	—	inches
R	0.075	—	—	mm	0.003	—	—	inches
aaa	0.10			mm	0.004			inches
bbb	0.07			mm	0.003			inches
ccc	0.10			mm	0.004			inches
ddd	0.05			mm	0.002			inches
eee	0.08			mm	0.003			inches
fff	0.10			mm	0.004			inches

1. Controlling dimension: millimeters
2. Reference document: JEDEC MO–220

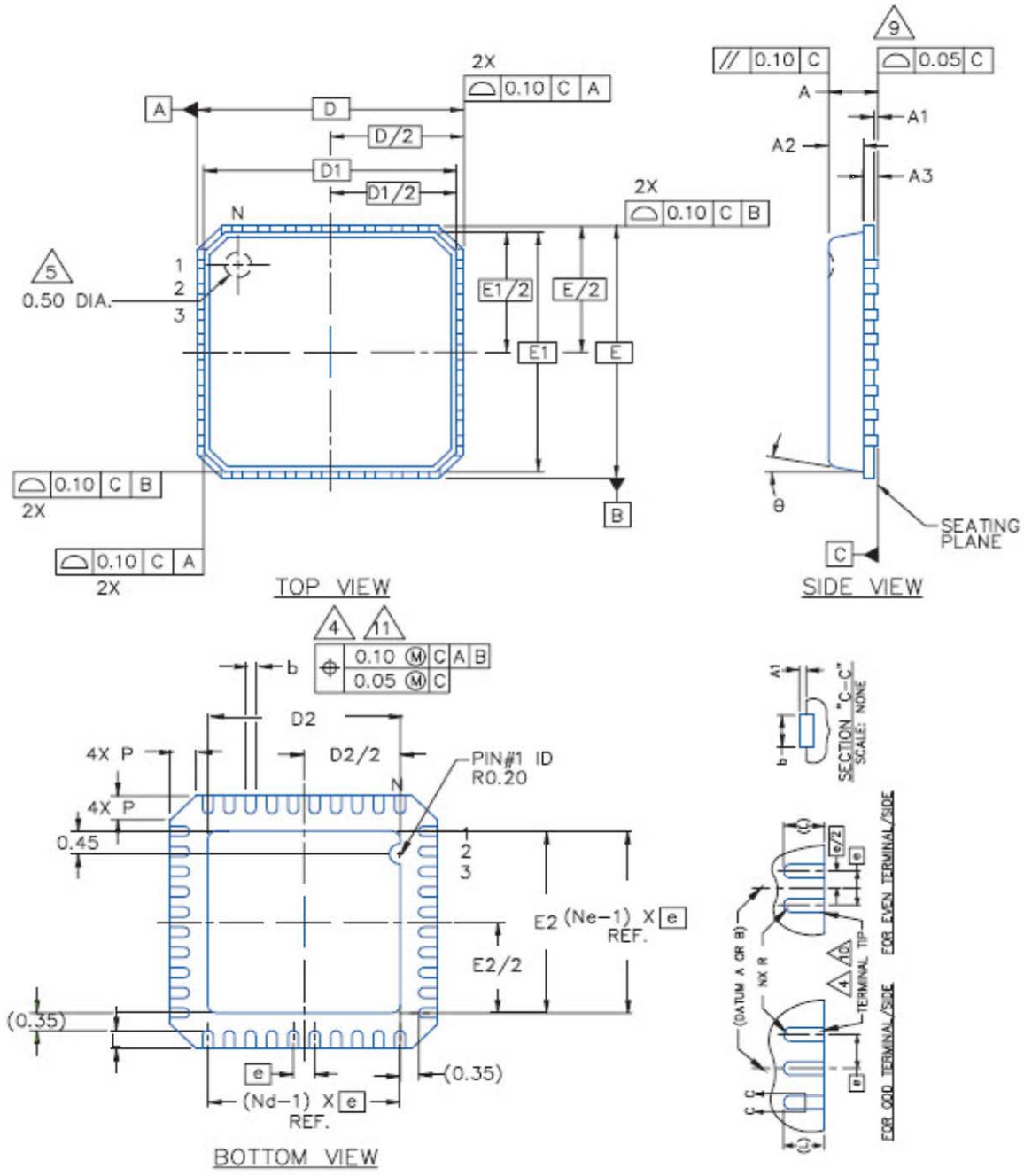

Figure 5-2 Package drawing – SPD

Table 5-2 Package dimensions - SPD

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.01	0.05	mm	0.000	0.000	0.002	inches
A2	0.60	0.65	0.70	mm	0.025	0.026	0.028	inches
A3	0.20 REF				0.008 REF			
D	5.00 BSC							
D1	4.75 BSC							
D2	3.50	3.60	3.70	mm	0.137	0.141	0.145	inches
E	5.00 BSC							
E1	4.75 BSC							
E2	3.50	3.60	3.70	mm	0.137	0.141	0.145	inches
θ	0	—	14	°	0	—	14	°
P	0.24	0.42	0.62	mm				

1. Controlling dimension: millimeters
2. Reference document: JEDEC MO–220

6 Ordering Information

The AR3002 can be ordered by using the following part numbers:

- AR3002-AL3D specifies a halogen-free version of AR3002 QFN (v2.2)
- AR3002-BL3D specifies a halogen-free version of AR3002 QFN (v2.2.1)

A Terms and Acronyms

Table A-1 Acronyms, abbreviations, and terms

Term	Definition
AES	Advanced encryption standard
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
AR	Area ratio
BB	Baseband module
BGA	Ball grid arrays
BIAS	Associated bias/control
BOM	Bill of materials
BT	Bluetooth
CMOS	Complementary metal oxide semiconductor
CODEC	Coder-Decoder
DPSK	Differential Phase Shift Keying
DQPSK	Differential quadrature phase shift keying
EEPROM	Electrically erasable programmable read-only memory
GND	Ground
GPIO	General-purpose input/output
HCI	Host controller interface
LE	Low energy
LDO	Linear voltage regulator
LNA2	Low-noise amplifier
LPO	On-chip low power oscillator
ODM	Original design manufacturer
OEM	Original equipment manufacturer
OTP	One-time programmable
PABIASP	Bias pin for the internal PA
PCM	Pulse-coded modulation
POR	Power-on-reset
QFN	Quad flat no-lead
QTI	Qualcomm Technologies, Inc.
RF	Radio frequency
RFIOP	Radio Frequency Input and Output
RISC	Reduced instruction set computing

Term	Definition
ROM	Read-only database
Rx	Receive, receiver
SRAM	Static random access memory
Tx	Transmit, transmitter
UART	Universal asynchronous receiver/transmitter
VDD	Supply voltage
WLAN	Wireless local area network

B EXHIBIT 1

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