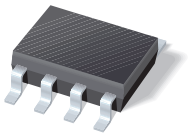


SLOS388B − OCTOBER 2001 − REVISED JUNE 2002

WIDEBAND, FET-INPUT OPERATIONAL AMPLIFIER

FEATURES

- **Gain Bandwidth Product: 180 MHz**
- **Slew Rate: 100 V/μs**
- **Maximum Input Bias Current: 100 pA**
- **Input Voltage Noise: 5.4 nV/√Hz**
- **Maximum Input Offset Voltage: 4 mV**
- **Input Impedance: 10^9 Ω || 10 pF**
- **Power Supply Voltage Range: ±5 to ±15 V**
- **Unity Gain Stable**

APPLICATIONS

- **Wideband Photodiode Amplifier**
- **High-Speed Transimpedance Gain Stage**
- **Test and Measurement Systems**
- **Current-DAC Output Buffer**
- **Active Filtering**
- **High-Speed Signal Integrator**
- **High-Impedance Buffer**

DESCRIPTION

The THS4601 is a high-speed, FET-input operational amplifier designed for applications requiring wideband operation, high-input impedance, and high-power supply voltages. By providing a 180-MHz gain-bandwidth product, ±15-V supply operation, and 100-pA input bias current, the THS4601 is capable of wideband transimpedance gain and large output signal swing simultaneously. Low current and voltage noise allow amplification of extremely low-level input signals while still maintaining a large signal-to-noise ratio.

The characteristics of the THS4601 ideally suit it for use as a wideband photodiode amplifier. Photodiode output current is a prime candidate for transimpedance amplification, an application of which is illustrated in Figure 1. Other potential applications include test and measurement systems requiring high-input impedance, digital-to-analog converter output buffering, high-speed integration, and active filtering.

A SELECTION OF RELATED OPERATIONAL AMPLIFIER PRODUCTS

DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/μs)	VOLTAGE NOISE (nV/√Hz)	DESCRIPTION
OPA627	±15	16	55	4.5	Unity-gain stable FET-input amplifier
OPA637	±15	80	135	4.5	Gain of +5 stable FET-input amplifier
OPA655	±5	400	290	6	Unity-gain stable FET-input amplifier

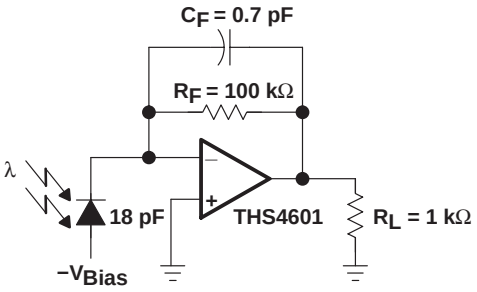
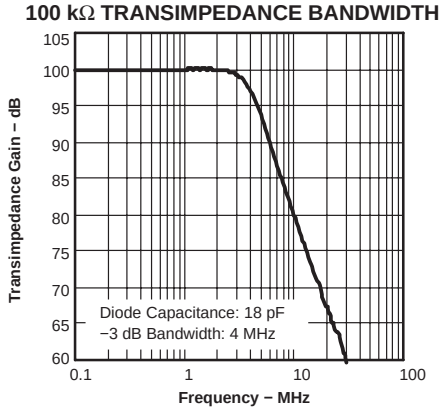
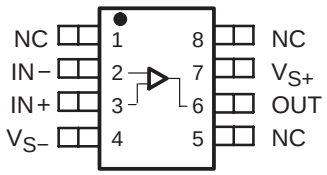


Figure 1. Wideband Photodiode Transimpedance Amplifier



THS4601
D AND DDA PACKAGE
(TOP VIEW)



NC − No internal connection

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
NC	1, 5, 8	These pins have no internal connection.
IN−	2	Inverting input of the amplifier
IN+	3	Noninverting input of the amplifier
V_{S-}	4	Negative power supply
OUT	6	Output of the amplifier
V_{S+}	7	Positive power supply

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{S+} . . . . . 16.5 V
Supply voltage, V_{S-} . . . . . −16.5 V
Input voltage, V_I . . . . . $\pm V_S$
Output current, I_O . . . . . 100 mA
Differential input voltage, V_{ID} . . . . . ±4 V
Maximum junction temperature, T_J . . . . . 150°C
Operating free-air temperature, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . −40°C to 85°C
Storage temperature, T_{stg} . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE AND ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
THS4601CD	SOIC surface mount	8D	0°C to 70°C	4601C
THS4601ID	SOIC surface mount	8D	−40°C to 85°C	4601I
THS4601CDDA	SOIC surface mount with PowerPAD™	8DDA	0°C to 70°C	4601C
THS4601IDDA	SOIC surface mount with PowerPAD™	8DDA	−40°C to 85°C	4601I

NOTE: The THS4601 is available taped and reeled. Add an R suffix to the device type when ordering (e.g., THS4601IDR).

PowerPAD is a trademark of Texas Instruments.

electrical specifications: V_S = ±15 V: R_F = 250 Ω, R_L = 1 kΩ and G = +2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	THS4601					
			TYP	OVER TEMPERATURE				UNIT
			25°C	25°C	0°C to 70°C	−40°C to 85°C	MIN/ MAX	
AC PERFORMANCE								
Small-signal bandwidth		G = +1, V_O = 20 mV_{pp}, R_F = 0 Ω	440				Typ	MHz
		G = +2, V_O = 40 mV_{pp}, R_F = 62 Ω	95				Typ	MHz
		G = +5, V_O = 100 mV_{pp}, R_F = 500 Ω	36				Typ	MHz
		G = +10, V_O = 200 mV_{pp}, R_F = 1 kΩ	18				Typ	MHz
Gain-bandwidth product		G > +10	180				Typ	MHz
Bandwidth for 0.1 dB flatness		G = +2, V_O = 200 mV_{pp}	5				Typ	MHz
Large-signal bandwidth		G = +5, V_O = 10 V_{pp}	3				Typ	MHz
Slew rate, SR		G = +5, 10 V Step	100				Typ	V/µs
Rise/fall time, t_r/t_f		1.0 V Step	7				Typ	ns
Settling time, t_S	0.01%	G = +5, V_O = 5 V Step	170				Typ	ns
	0.1%	G = +5, V_O = 5 V Step	135				Typ	ns
Harmonic distortion		G = +2, f = 1 MHz, V_O = 2V_{pp}						
2^{nd} Harmonic		R_L = 100 Ω	−65				Typ	dBc
		R_L = 1 kΩ	−77				Typ	
3^{rd} Harmonic		R_L = 100 Ω	−73				Typ	dBc
		R_L = 1 kΩ	−96				Typ	
Input voltage noise, V_n		f > 10 kHz	5.4				Typ	nV/√Hz
Input current noise, I_n		f > 10 kHz	5.5				Typ	fA/√Hz
Differential gain (NTSC, PAL)		G = +2, R_L = 150 Ω	0.02%				Typ	
Differential phase (NTSC, PAL)		G = +2, R_L = 150 Ω	0.08				Typ	°
DC PERFORMANCE								
Open-loop voltage gain		G = −10, R_L = 1 kΩ	105	94	92	90	Min	dB
Input offset voltage, V_{IO}		V_{CM} = 0 V	1.0	4.0	4.5	5.0	Max	mV
Average offset voltage drift		V_{CM} = 0 V			±10	±10	Typ	µV/°C
Input bias current, I_{IB}		V_{CM} = 0 V	30	100	550	1100	Max	pA
Average bias current drift		V_{CM} = 0 V			50	50	Typ	pA/°C
Input offset current, I_{IO}		V_{CM} = 0 V	2	100	200	300	Max	pA
Average offset current drift		V_{CM} = 0 V			5	5	Typ	pA/°C
INPUT								
Common-mode input range, V_{IC}			±13.0	12.6 to −12.0	12.5 to −11.9	12.4 to −11.8	Min	V
Common-mode rejection ratio, CMRR			110	100	95	90	Min	dB
Input impedance, Z_{id}	Differential		10^9 || 3.5				Typ	Ω || pF
Input impedance, Z_{ic}	Common-mode		10^9 || 6.5				Typ	Ω || pF

electrical specifications: V_S = ±15 V: R_F = 250 Ω, R_L = 1kΩ and G = +2 (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	THS4601					
			TYP	OVER TEMPERATURE				UNIT
			25°C	25°C	0°C to 70°C	−40°C to 85°C	MIN/ MAX	
OUTPUT								
Voltage output swing		R_L = 1 kΩ	12.8 to –13.4	12.4 to −13.1	12.3 to −13.0	12.1 to −12.8	Min	V
Current output, I_O	Sourcing	R_L = 20 Ω	−80	−60	−60	−59	Min	mA
	Sinking		50	35	35	34	Min	
Closed-loop output impedance, Z_O		G = +1, f = 1 MHz	0.1				Typ	Ω
POWER SUPPLY								
Specified operating voltage			±15	±16.5	±16.5	±16.5	Max	V
Maximum quiescent current			10.0	11.5	11.7	12.0	Max	mA
Minimum quiescent current			10.0	8.5	8.3	8.0	Min	mA
Power supply rejection	+PSRR		115	90	88	86	Min	dB
	−PSRR		115	90	88	86	Min	
TEMPERATURE								
Specified operating range, T_A			−40 to 85				Typ	°C
Thermal resistance, θ_{JA}		Junction-to-ambient						
8D: SO−8			170				Typ	°C/W
8DDA: SO−8 with PowerPAD			66.6				Typ	°C/W

electrical specifications: V_S = ±5 V: R_F = 250 Ω, R_L = 1 kΩ and G = +2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	THS4601					
			TYP	OVER TEMPERATURE				UNIT
			25°C	25°C	0°C to 70°C	−40°C to 85°C	MIN/ MAX	
AC PERFORMANCE								
Small-signal bandwidth		G = +1, V_O = 20 mV_{pp}	400				Typ	MHz
		G = +2, V_O = 40 mV_{pp}	100				Typ	MHz
		G = +5, V_O = 100 mV_{pp}	50				Typ	MHz
		G = +10, V_O = 200 mV_{pp}	18				Typ	MHz
Gain-bandwidth product		G > +10	180				Typ	MHz
Bandwidth for 0.1 dB flatness		G = +2, V_O = 200 mV_{pp}	5				Typ	MHz
Large-signal bandwidth		G = +5, V_O = 5 V_{pp}	6				Typ	MHz
Slew rate, SR		G = +5, 5 V Step	100				Typ	V/μs
Rise/fall time, t_r/t_f		1.0 V Step	8				Typ	ns
Settling time, t_S	0.01%	G = +5, V_O = 2 V Step	140				Typ	ns
	0.1%	G = +5, V_O = 2 V Step	170				Typ	ns
Harmonic distortion		G = +2, f = 1 MHz, V_O = 2V_{pp}						
2^{nd} Harmonic		R_L = 100 Ω	−74				Typ	dBc
		R_L = 1 kΩ	−84				Typ	
3^{rd} Harmonic		R_L = 100 Ω	−79				Typ	dBc
		R_L = 1 kΩ	−94				Typ	
Input voltage noise, V_n		f > 10 kHz	5.4				Typ	nV/√Hz
Input current noise, I_n		f > 10 kHz	5.5				Typ	fA/√Hz
Differential gain (NTSC and PAL)		G = +2, R_L = 150 Ω	0.02%				Typ	
Differential phase (NTSC and PAL)		G = +2, R_L = 150 Ω	0.08				Typ	°
DC PERFORMANCE								
Open-loop voltage gain		G = −10, R_L = 1 kΩ	105	94	92	90	Min	dB
Input offset voltage, V_{IO}		V_{CM} = 0 V	1.0	4.0	4.5	5.0	Max	mV
Average offset voltage drift		V_{CM} = 0 V			±10	±10	Typ	μV/°C
Input bias current, I_{IB}		V_{CM} = 0 V	20	100	550	1100	Max	pA
Average bias current drift		V_{CM} = 0 V			50	50	Typ	pA/°C
Input offset current, I_{IO}		V_{CM} = 0 V	1	100	200	300	Max	pA
Average offset current drift		V_{CM} = 0 V			5	5	Typ	pA/°C
INPUT								
Common-mode input range, V_{IC}			±2.2	2.7 to −2.0	2.6 to −1.9	2.5 to −1.8	Min	V
Common-mode rejection ratio, CMRR			110	100	95	90	Min	dB
Input impedance, Z_{id}	Differential		10^9 || 3.5				Typ	Ω || pF
Input impedance, Z_{ic}	Common-mode		10^9 || 6.5				Typ	Ω || pF
OUTPUT								
Voltage output swing		R_L = 1 kΩ	2.9 to −3.5	2.6 to −3.3	2.5 to −3.2	2.3 to −3.1	Min	V
Current output, I_O	Sourcing	R_L = 20 Ω	−65	−48	−48	−47	Min	mA
	Sinking		45	30	30	29	Min	
Closed-loop output impedance, Z_o		G = +1, f = 1 MHz	0.1				Typ	Ω

electrical specifications: V_S = ±5 V; R_F = 250 Ω, R_L = 1 kΩ and G = +2 (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	THS4601					
			TYP	OVER TEMPERATURE				UNIT
			25°C	25°C	0°C to 70°C	−40°C to 85°C	MIN/ MAX	
POWER SUPPLY								
Specified operating voltage			±5	±16.5	±16.5	±16.5	Max	V
Maximum quiescent current			9.6	11.2	11.4	11.7	Max	mA
Minimum quiescent current			9.6	8.2	8.0	7.7	Min	mA
Power supply rejection	+PSRR		110	90	88	86	Min	dB
	−PSRR		110	90	88	86	Min	
TEMPERATURE								
Specified operating range, T_A			−40 to 85				Typ	°C
Thermal resistance, θ_{JA}		Junction-to-ambient						
8D: SO−8			170				Typ	°C/W
8DDA: SO−8 with PowerPAD			67				Typ	°C/W

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

measurement conditions: T_A = 25°C, R_L = 1 kΩ, V_S = ±15 V (unless otherwise noted)

SMALL-SIGNAL UNITY GAIN FREQUENCY RESPONSE

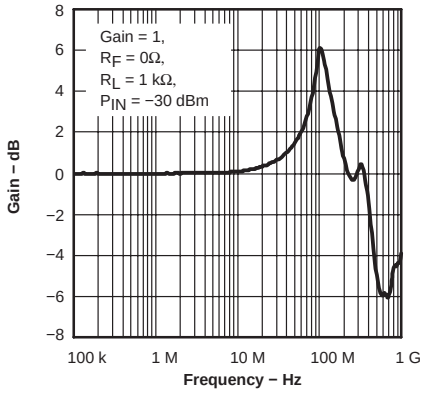


Figure 2

LARGE-SIGNAL UNITY GAIN FREQUENCY RESPONSE

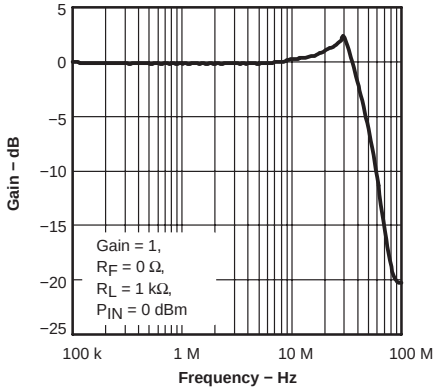


Figure 3

SMALL-SIGNAL FREQUENCY RESPONSE, GAIN = +2

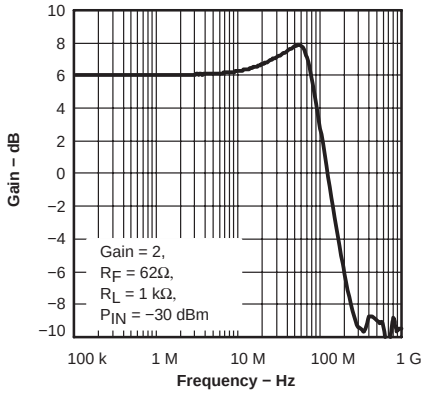


Figure 4

SMALL-SIGNAL FREQUENCY RESPONSE, GAIN = +5

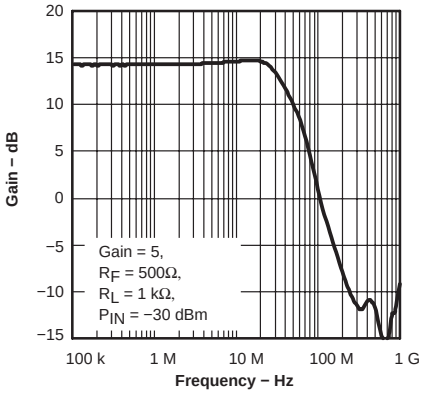


Figure 5

SMALL-SIGNAL FREQUENCY RESPONSE, GAIN = +10

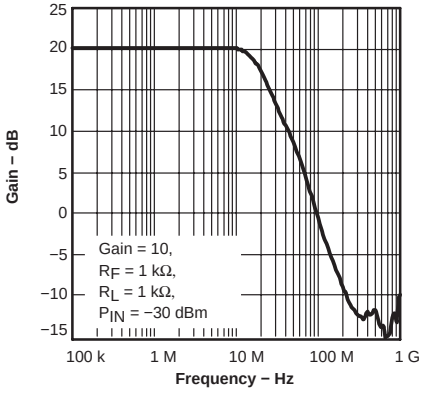


Figure 6

SMALL-SIGNAL FREQUENCY RESPONSE, GAIN = +100

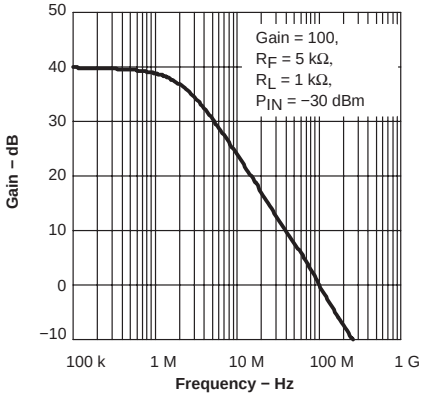


Figure 7

TYPICAL CHARACTERISTICS

measurement conditions: T_A = 25°C, R_L = 1 kΩ, V_S = ±15 V (unless otherwise noted)

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

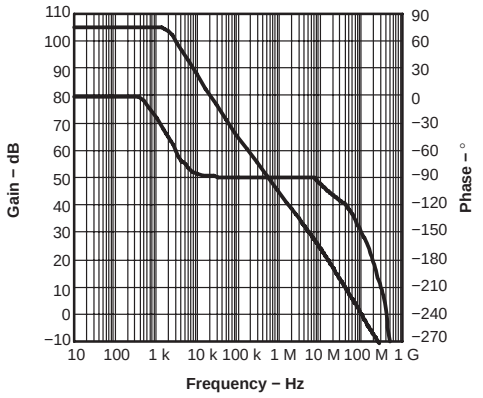


Figure 8

VOLTAGE NOISE vs FREQUENCY

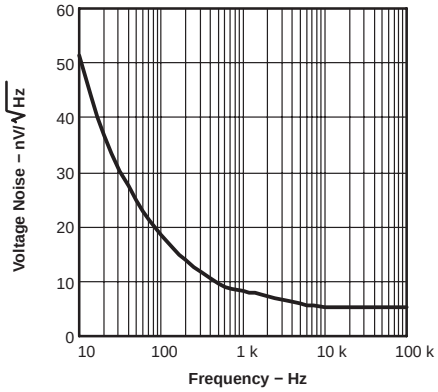


Figure 9

REJECTION RATIOS vs FREQUENCY

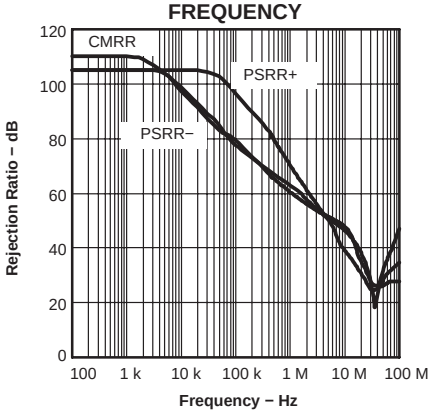


Figure 10

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

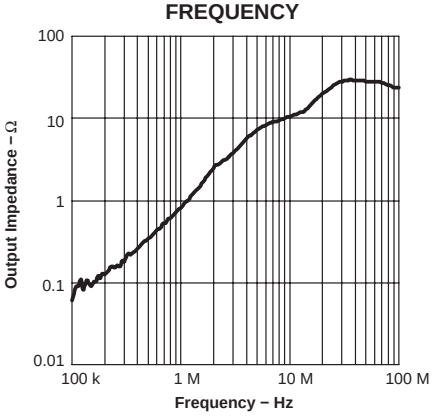


Figure 11

LARGE-SIGNAL PULSE RESPONSE

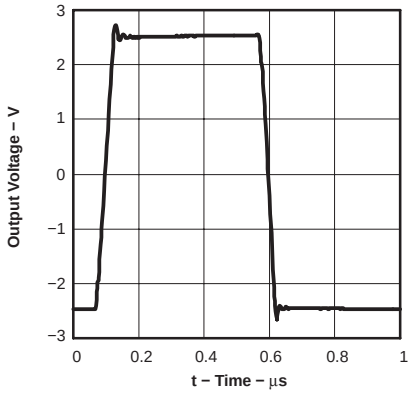


Figure 12

HARMONIC DISTORTION vs FREQUENCY

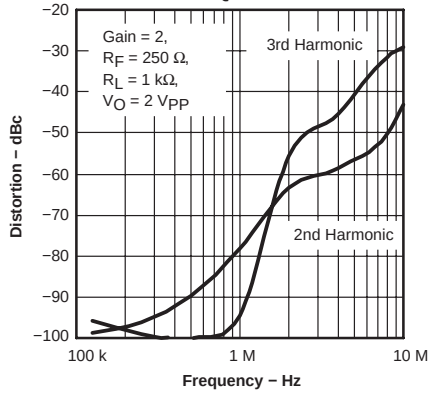


Figure 13

TYPICAL CHARACTERISTICS

measurement conditions: T_A = 25°C, R_L = 1 kΩ, V_S = ±15 V (unless otherwise noted)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

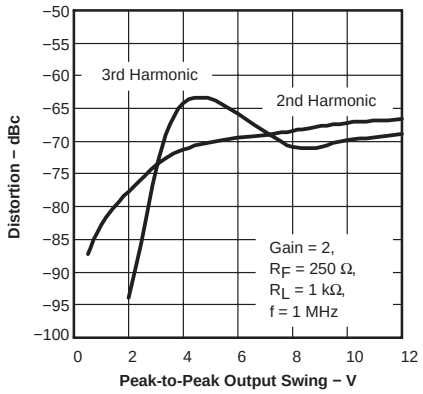


Figure 14

SLEW RATE vs OUTPUT VOLTAGE STEP

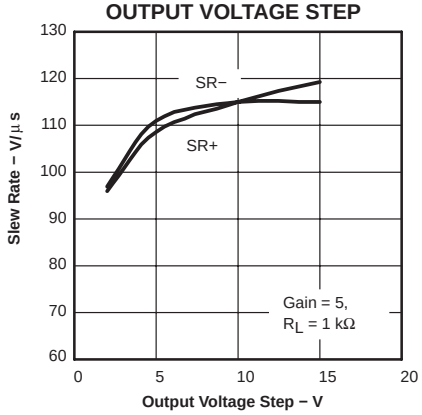


Figure 15

INPUT BIAS CURRENT vs INPUT COMMON-MODE RANGE

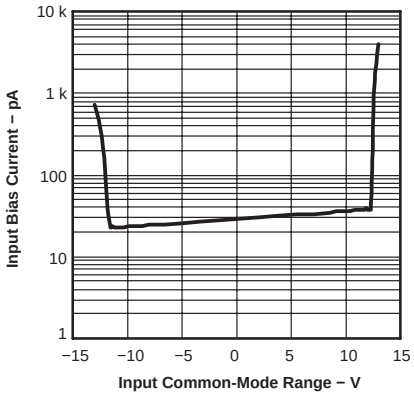


Figure 16

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

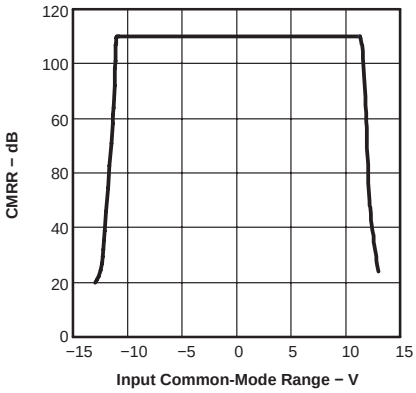


Figure 17

OPEN-LOOP GAIN vs TEMPERATURE

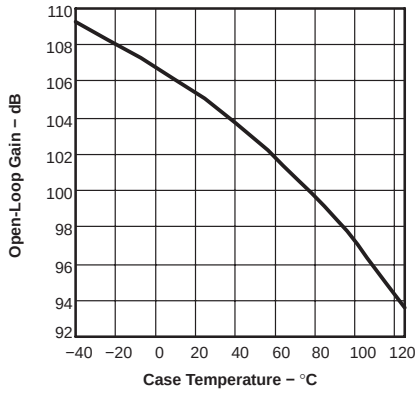


Figure 18

INPUT BIAS CURRENT vs TEMPERATURE

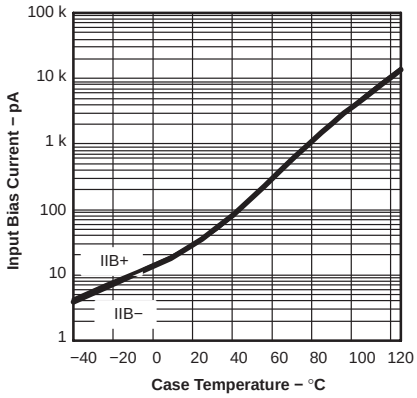


Figure 19

TYPICAL CHARACTERISTICS

measurement conditions: T_A = 25°C, R_L = 1 kΩ, V_S = ±15 V (unless otherwise noted)

INPUT OFFSET CURRENT vs TEMPERATURE

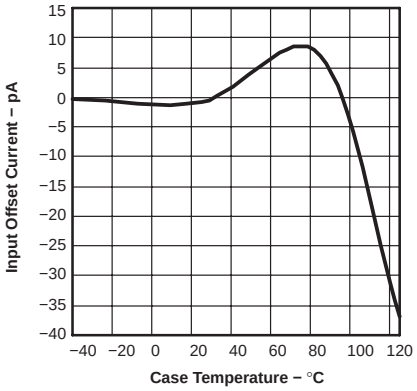


Figure 20

OFFSET VOLTAGE vs TEMPERATURE

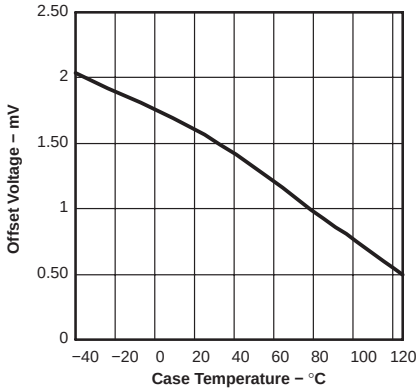


Figure 21

QUIESCENT CURRENT vs TEMPERATURE

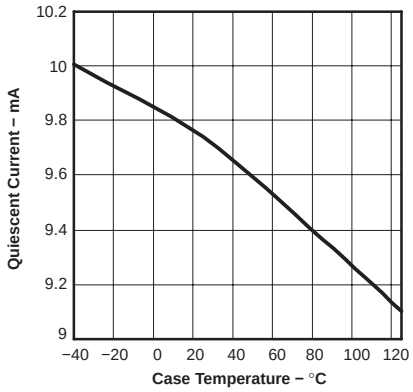


Figure 22

OUTPUT CURRENT vs TEMPERATURE

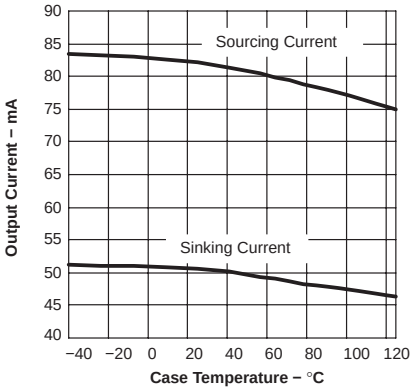


Figure 23

OUTPUT VOLTAGE SWING vs TEMPERATURE

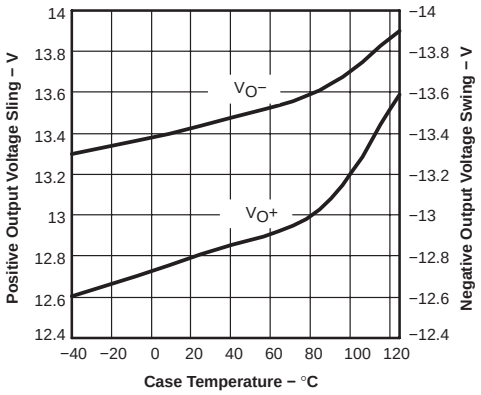


Figure 24

REJECTION RATIOS vs TEMPERATURE

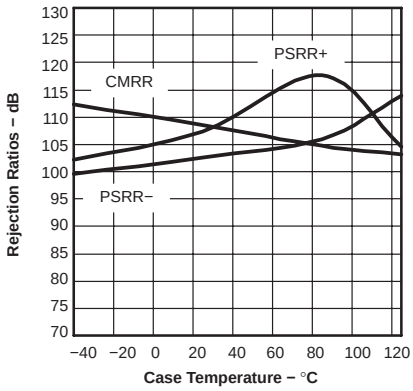


Figure 25

APPLICATION INFORMATION

introduction

The THS4601 is a high-speed, FET-input operational amplifier. The combination of its high frequency capabilities and its DC precision make it a design option for a wide variety of applications, including test and measurement, optical monitoring, transimpedance gain circuits, and high-impedance buffers. The applications section of the data sheet discusses these particular applications in addition to general information about the device and its features.

transimpedance fundamentals

FET-input amplifiers are often used in transimpedance applications because of their extremely high input impedance. A transimpedance block accepts a current as an input and converts this current to a voltage at the output. The high-input impedance associated with FET-input amplifiers minimizes errors in this process caused by the input bias currents, I_{IB}, of the amplifier.

designing the transimpedance circuit

Typically, design of a transimpedance circuit is driven by the characteristics of the current source that provides the input to the gain block. A photodiode is the most common example of a capacitive current source that would interface with a transimpedance gain block. Continuing with the photodiode example, the system designer traditionally chooses a photodiode based on two opposing criteria: speed and sensitivity. Faster photodiodes cause a need for faster gain stages, and more sensitive photodiodes require higher gains in order to develop appreciable signal levels at the output of the gain stage.

These parameters affect the design of the transimpedance circuit in a few ways. First, the speed of the photodiode signal determines the required bandwidth of the gain circuit. However, the required gain, based on the sensitivity of the photodiode, limits the bandwidth of the circuit. Additionally, the larger capacitance associated with a more sensitive signal source also detracts from the achievable speed of the gain block. The dynamic range of the input signal also places requirements on the amplifier's dynamic range. Knowledge of the source's output current levels, coupled with a desired voltage swing on the output, dictates the value of the feedback resistor, R_F. The transfer function from input to output is $V_{OUT} = I_{IN}R_F$.

The large gain-bandwidth product of the THS4601 provides the capability for achieving both high transimpedance gain and wide bandwidth simultaneously. In addition, the high power supply rails provide the potential for a very wide dynamic range at the output, allowing for the use of input sources which possess wide dynamic range. The combination of these characteristics makes the THS4601 a design option for systems that require transimpedance amplification of wideband, low-level input signals. A standard transimpedance circuit is shown in Figure 26.

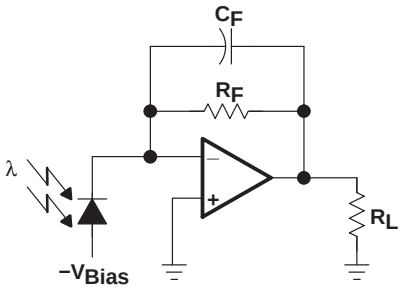


Figure 26. Wideband Photodiode Transimpedance Amplifier

APPLICATION INFORMATION

designing the transimpedance circuit (continued)

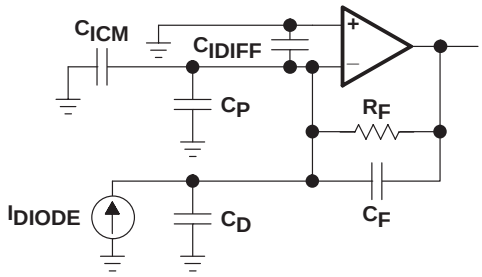
As indicated, the current source typically sets the requirements for gain, speed, and dynamic range of the amplifier. For a given amplifier and source combination, achievable performance is dictated by the following parameters: the amplifier's gain-bandwidth product, the amplifier's input capacitance, the source capacitance, the transimpedance gain, the amplifier's slew rate, and the amplifier's output swing. From this information, the optimal performance of a transimpedance circuit using a given amplifier can be determined. Optimal is defined here as providing the required transimpedance gain with a maximally flat frequency response.

For the circuit shown in Figure 26, all but one of the design parameters is known; the feedback capacitor must be determined. Proper selection of the feedback capacitor prevents an unstable design, controls pulse response characteristics, provides maximally flat transimpedance bandwidth, and limits broadband integrated noise. The maximally flat frequency response results with C_F calculated as shown in equation 1, where C_F is the feedback capacitor, R_F is the feedback resistor, C_S is the total source capacitance (including amplifier input capacitance and parasitic capacitance at the inverting node), and GBP is the gain-bandwidth product of the amplifier in hertz.

$$C_F = \frac{\frac{1}{\pi R_F GBP} + \sqrt{\left(\frac{1}{\pi R_F GBP}\right)^2 + \frac{4C_S}{\pi R_F GBP}}}{2} \quad (1)$$

Once the optimal feedback capacitor has been selected, the transimpedance bandwidth can be calculated with equation 2.

$$F_{-3\ dB} = \sqrt{\frac{GBP}{2\pi R_F \left(C_S + C_F\right)}} \quad (2)$$



$C_S = C_{ICM} + C_{IDIFF} + C_P + C_D$

Where: C_{ICM} is the common-mode input capacitance.
C_{IDIFF} is the differential input capacitance.
C_D is the diode capacitance.
C_P is parasitic capacitance at the inverting node.

NOTE: The total source capacitance is the sum of several distinct capacitances.

Figure 27. Transimpedance Analysis Circuit

APPLICATION INFORMATION

designing the transimpedance circuit (continued)

The feedback capacitor provides a pole in the noise gain of the circuit, counteracting the zero in the noise gain caused by the source capacitance. The pole is set such that the noise gain achieves a 20 dB per decade rate-of-closure with the open-loop gain response of the amplifier, resulting in a stable circuit. As indicated, the formula given provides the feedback capacitance for maximally flat bandwidth. Reduction in the value of the feedback capacitor can increase the signal bandwidth, but this occurs at the expense of peaking in the AC response.

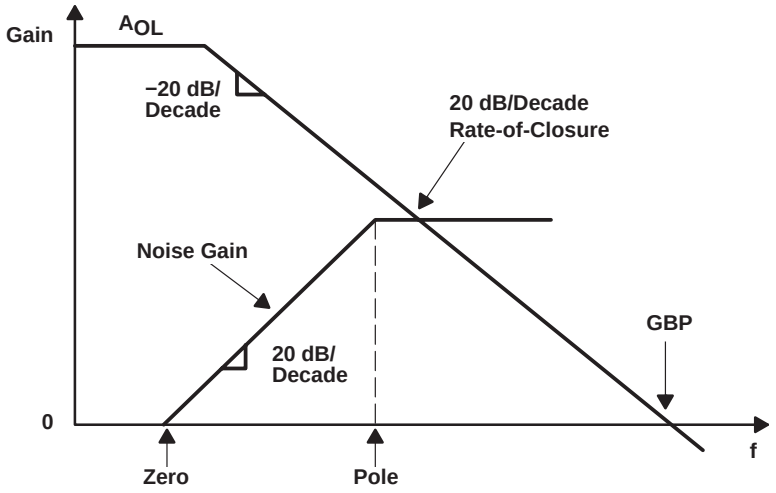


Figure 28. Transimpedance Circuit Bode Plot

The performance of the THS4601 has been measured for a variety of transimpedance gains with a variety of source capacitances. The achievable bandwidths of the various circuit configurations are summarized numerically in the table. The frequency responses are presented in the Figures 27, 28, and 29.

Note that the feedback capacitances do not correspond exactly with the values predicted by the equation. They have been tuned to account for the parasitic capacitance of the feedback resistor (typically 0.2 pF for 0805 surface mount devices) as well as the additional capacitance associated with the PC board. The equation should be used as a starting point for the design, with final values for C_F optimized in the laboratory.

APPLICATION INFORMATION

designing the transimpedance circuit (continued)

Table 1. Transimpedance Performance Summary for Various Configurations

SOURCE CAPACITANCE (pF)	TRANSIMPEDANCE GAIN (Ω)	FEEDBACK CAPACITANCE (pF)	−3 dB FREQUENCY (MHz)
18	10k	2.2	10.4
18	100k	0.6	3.3
18	1M	0	1.1
47	10k	3.3	7.6
47	100k	0.6	2.8
47	1M	0	0.88
100	10k	3.9	5.9
100	100k	1.5	1.3
100	1M	0	0.62
220	10k	5.6	3.8
220	100k	1.8	1.1
220	1M	0.4	0.36

10 kΩ TRANSIMPEDANCE BANDWIDTH FOR VARIOUS SOURCE CAPACITANCES

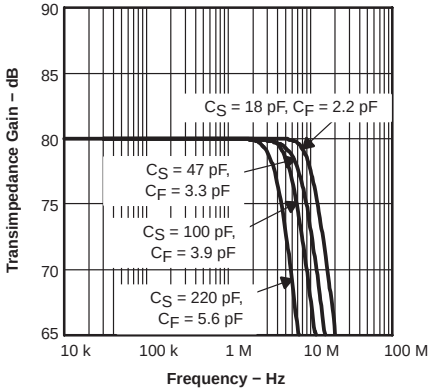


Figure 29

100 kΩ TRANSIMPEDANCE BANDWIDTH FOR VARIOUS SOURCE CAPACITANCES

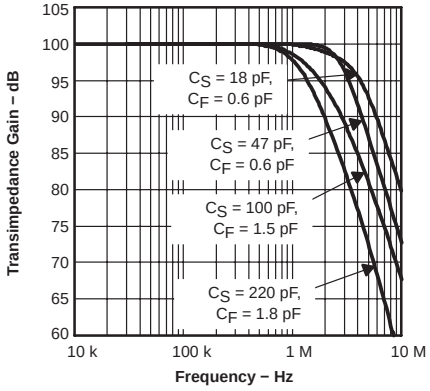


Figure 30

1 MΩ TRANSIMPEDANCE BANDWIDTH FOR VARIOUS SOURCE CAPACITANCES

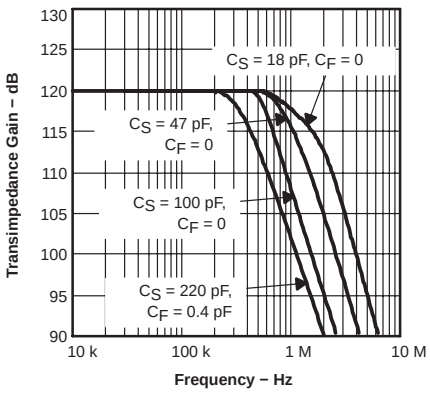


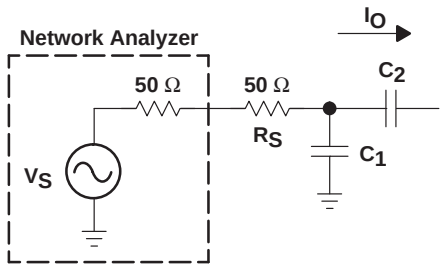
Figure 31

measuring transimpedance bandwidth

While there is no substitute for measuring the performance of a particular circuit under the exact conditions that are used in the application, the complete system environment often makes measurements harder. For transimpedance circuits, it is difficult to measure the frequency response with traditional laboratory equipment because the circuit requires a current as an input rather than a voltage. Also, the capacitance of the current source has a direct effect on the frequency response. A simple interface circuit can be used to emulate a capacitive current source with a network analyzer. With this circuit, transimpedance bandwidth measurements are simplified, making amplifier evaluation easier and faster.

APPLICATION INFORMATION

measuring transimpedance bandwidth (continued)



$$\frac{I_O}{V_S} = \frac{1}{2R_S\left(1 + \frac{C_1}{C_2}\right)} \text{ (above the pole frequency)}$$

NOTE: This interface network creates a capacitive, constant current source from a network analyzer and properly terminates the network analyzer at high frequencies.

Figure 32. Emulating a Capacitive Current Source With a Network Analyzer

The transconductance transfer function of the interface circuit is

$$\frac{I_O}{V_s}(s) = \frac{\frac{s}{2R_S\left(1+\frac{C_1}{C_2}\right)}}{s + \frac{1}{2R_S(C_1 + C_2)}}.$$

This transfer function contains a zero at DC and a pole at $s = \frac{1}{2R_S(C_1 + C_2)}$. The transconductance is constant at $\frac{1}{2R_S\left(1 + \frac{C_1}{C_2}\right)}$, above the pole frequency, providing a controllable AC current source. This circuit also properly terminates the network analyzer with 50 Ω at high frequencies. The second requirement for this current source is to provide the desired output impedance, emulating the output impedance of a photodiode or other current source. The output impedance of this circuit is given by

$$Z_O(s) = \frac{C_1 + C_2}{C_1 C_2}\left[\frac{s + \frac{1}{2R_s(C_1 + C_2)}}{s\left(s + \frac{1}{2R_s C_1}\right)}\right].$$

Assuming $C_1 >> C_2$, the equation reduces to $Z_O \approx \frac{1}{sC_2}$, giving the appearance of a capacitive source at higher frequency.

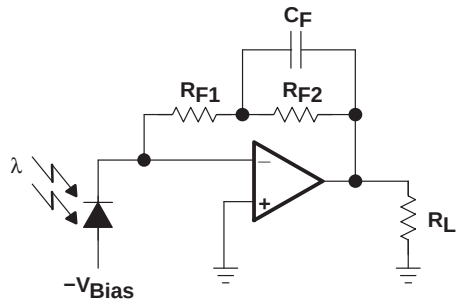
Capacitor values should be chosen to satisfy two requirements. First, C_2 should represent the anticipated capacitance of the true source. C_1 should then be chosen such that the corner frequency of the transconductance network is much less than the transimpedance bandwidth of the circuit. Choosing this corner frequency properly leads to more accurate measurements of the transimpedance bandwidth. If the interface circuit's corner frequency is too close to the bandwidth of the circuit, determining the power level in the flatband is difficult. A decade or more of flat bandwidth provides a good basis for determining the proper transimpedance bandwidth.

APPLICATION INFORMATION

alternative transimpedance configurations

Other transimpedance configurations are possible. Three possibilities are shown below.

The first configuration is a slight modification of the basic transimpedance circuit. By splitting the feedback resistor, the feedback capacitor value becomes more manageable and easier to control. This type of compensation scheme is useful when the feedback capacitor required in the basic configuration becomes so small that the parasitic effects of the board and components begin to dominate the total feedback capacitance. By reducing the resistance across the capacitor, the capacitor value can be increased. This mitigates the dominance of the parasitic effects.

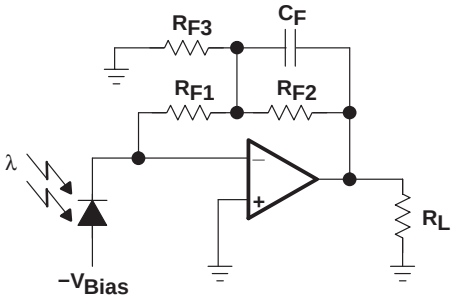


NOTE: Splitting the feedback resistor enables use of a larger, more manageable feedback capacitor.

Figure 33. Alternative Transimpedance Configuration #1

The second configuration uses a resistive T-network to achieve very high transimpedance gains using relatively small resistor values. This topology can be very useful when the desired transimpedance gain exceeds the value of available resistors. The transimpedance gain is given by equation 3.

$$R_{EQ} = R_{F1}\left(1 + \frac{R_{F2}}{R_{F3}}\right) \quad (3)$$



NOTE: A resistive T-network enables high transimpedance gain with reasonable resistor values.

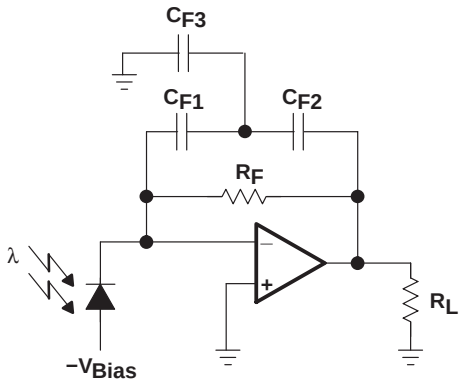
Figure 34. Alternative Transimpedance Configuration #2

APPLICATION INFORMATION

alternative transimpedance configurations (continued)

The third configuration uses a capacitive T-network to achieve fine control of the compensation capacitance. The capacitor C_{F3} can be used to tune the total effective feedback capacitance to a very fine degree. This circuit behaves the same as the basic transimpedance configuration, with the effective C_F given by equation 4.

$$\frac{1}{C_{FEQ}} = \frac{1}{C_{F1}}\left(1 + \frac{C_{F3}}{C_{F2}}\right) \tag{4}$$



NOTE: A capacitive T-network enables fine control of the effective feedback capacitance using relatively large capacitor values.

Figure 35. Alternative Transimpedance Configuration #3

summary of key decisions in transimpedance design

The following is a quick, simplified process for basic transimpedance circuit design. This process gives a quick start to the design process, though it does ignore some aspects that may be critical to the circuit.

Step 1: Determine the capacitance of the source.

Step 2: Calculate the total source capacitance, including the amplifier input capacitance, C_{ICM} and C_{IDIFF}.

Step 3: Determine the magnitude of the possible current output from the source, including the minimum signal current anticipated and maximum signal current anticipated.

Step 4: Choose a feedback resistor value such that the input current levels create the desired output signal voltages, and ensure that the output voltages can accommodate the dynamic range of the input signal.

Step 5: Calculate the optimum feedback capacitance using equation 1.

Step 6: Calculate the bandwidth given the resulting component values.

Step 7: Evaluate the circuit to see if all design goals are satisfied.

APPLICATION INFORMATION

selection of feedback resistors

Feedback resistor selection can have a significant effect on the performance of the THS4601 in a given application, especially in configurations with low closed-loop gain. If the amplifier is configured for unity gain, the output should be directly connected to the inverting input. Any resistance between these two points interacts with the input capacitance of the amplifier and causes an additional pole in the frequency response. For non-unity gain configurations, low resistances are desirable for flat frequency response. However, care must be taken not to load the amplifier too heavily with the feedback network if large output signals are expected. In most cases, a tradeoff will be made between the frequency response characteristics and the loading of the amplifier. For a gain of 2, a 250 Ω feedback resistor is a suitable operating point from both perspectives.

If resistor values are chosen too large, the THS4601 is subject to oscillation problems. For example, an inverting amplifier configuration with a 1-kΩ gain resistor and a 1-kΩ feedback resistor develops an oscillation due to the interaction of the large resistors with the input capacitance. In low gain configurations, avoid feedback resistors this large or anticipate using an external compensation scheme to stabilize the circuit.

overdrive recovery

The THS4601 has an overdrive recovery period when the output is driven close to one power supply rail or the other. The overdrive recovery time period is dependent upon the magnitude of the overdrive and whether the output is driven towards the positive or the negative power supply. The four graphs shown here depict the overdrive recovery time in two cases, an attempted 28 V_{PP} signal on the output and an attempted 30 V_{PP} signal on the output. Note that in both of these cases, the output does not achieve these levels as the output voltage swing is limited to less than these values, but these values are representative of the desired signal swing on the output for the given inputs. As shown in the figures, the recovery period increases as the magnitude of the overdrive increases, with the worst case recovery occurring with the negative rail. The recovery times are summarized in Table 2.

Table 2. Overdrive Recovery Characteristics

VOLTAGE RAIL	IDEAL OUTPUT SWING (V_{PP})	OVERDRIVE RECOVERY TIME (ns)
$+V_S$	28	320
$-V_S$	28	340
$+V_S$	30	540
$-V_S$	30	680

APPLICATION INFORMATION

overdrive recovery (continued)

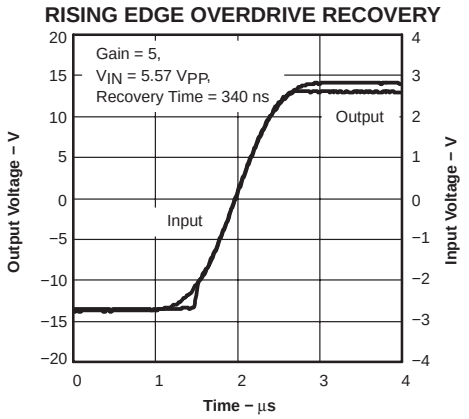


Figure 36

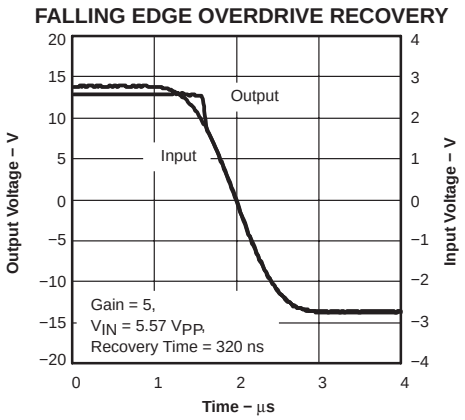


Figure 37

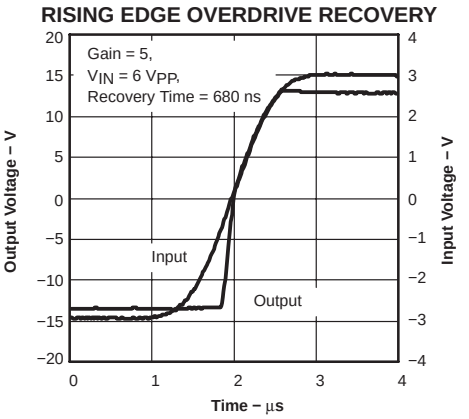


Figure 38

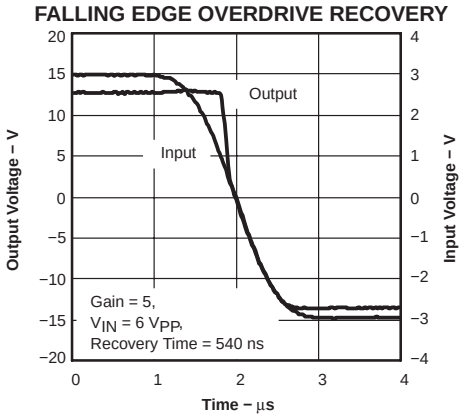


Figure 39

high frequency continuous wave amplification

When presented with high frequency sinusoids in low-gain configurations (G < 5), the THS4601 experiences a relatively large differential input voltage between the two input terminals of the amplifier. As this differential input voltage increases, the internal slew-boosting circuitry can cause some transistors in the signal path to enter the cutoff region of operation. As the derivative of the signal changes signs, these transistors suffer from a short recovery time period, generating appreciable levels of distortion. This behavior is depicted in the graph Harmonic Distortion vs Frequency. At 2 MHz with a 2 V_{PP} output signal, the distortion rises significantly. For most high-gain configurations including transimpedance applications, this phenomena is not problematic.

slew rate performance with varying input step amplitude and rise/fall time

Some FET input amplifiers exhibit the peculiar behavior of having a larger slew rate when presented with smaller input voltage steps and slower edge rates due to a change in bias conditions in the input stage of the amplifier under these circumstances. This phenomena is most commonly seen when FET input amplifiers are used as voltage followers. As this behavior is typically undesirable, the THS4601 has been designed to avoid these issues. Larger amplitudes lead to higher slew rates, as would be anticipated, and fast edges do not degrade the slew rate of the device.

APPLICATION INFORMATION

power dissipation and thermal characteristics

The THS4601 does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

Where:

P_{Dmax} is the maximum power dissipation (W)

T_{max} is the absolute maximum junction temperature (°C)

T_A is the ambient temperature (°C)

θ_{JA} is the thermal coefficient from the silicon junctions to the ambient air (°C/W)

For systems where heat dissipation is more critical, the THS4601 is offered in an 8-pin SOIC with PowerPAD. The thermal coefficient for the SOIC PowerPAD is substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the two packages. The data for the 8DDA package assumes a board layout that follows the PowerPAD layout guidelines.

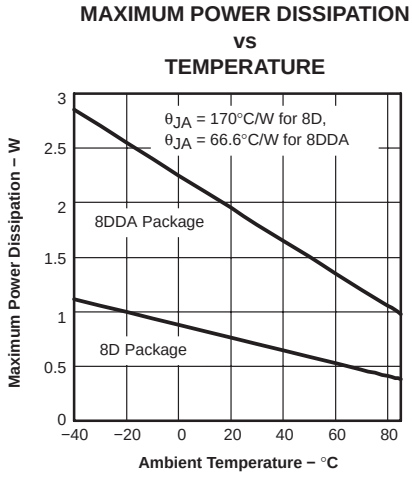


Figure 40

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

APPLICATION INFORMATION

PC board layout guidelines

Achieving optimum performance with a high frequency amplifier requires careful attention to board layout parasitics and external component selection. Recommendations that optimize performance include the following.

- Use of a ground plane—It is highly recommended that a ground plane be used on the board to provide all components with a low impedance connection to ground. However, the ground plane should be cleared around the amplifier inputs and outputs to minimize parasitic capacitance. A solid ground plane is recommended wherever possible.
- Proper power supply decoupling—A 6.8 μF tantalum capacitor and a 0.1 μF ceramic capacitor should be used on each power supply node. Good performance is possible if the 6.8 μF capacitor is shared among several amplifiers, but each amplifier should have a dedicated 0.1 μF capacitor for each supply. The 0.1 μF capacitor should be placed as close to the power supply pins as possible. As the distance from the device increases, the trace inductance rises and decreases the effectiveness of the capacitor. A good design has less than 2.5 mm separating the ceramic capacitor and the power supply pin. The tantalum capacitors can be placed significantly further away from the device.
- Avoid sockets—Sockets are not recommended for high-speed amplifiers. The lead inductance associated with the socket pins often leads to stability problems. Direct soldering to a printed-circuit board yields the best performance.
- Minimize trace length and place parts compactly—Shorter traces minimize stray parasitic elements of the design and lead to better high-frequency performance.
- Use of surface mount passive components—Surface mount passive components are recommended due to the extremely low lead inductance and the small component footprint. These characteristics minimize problems with stray series inductance and allow for a more compact circuit layout. Compact layout reduces both parasitic inductance and capacitance in the design.
- Minimize parasitic capacitance on the signal input and output pins—Parasitic capacitance on the input and output pins can degrade high frequency behavior or cause instability in the circuit. Capacitance on the inverting input or the output is a common cause of instability in high performance amplifiers, and capacitance on the noninverting input can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance around these pins, a window should be opened up in the signal/power layers that are underneath those pins. Power and ground planes should otherwise be unbroken.

PowerPAD design considerations

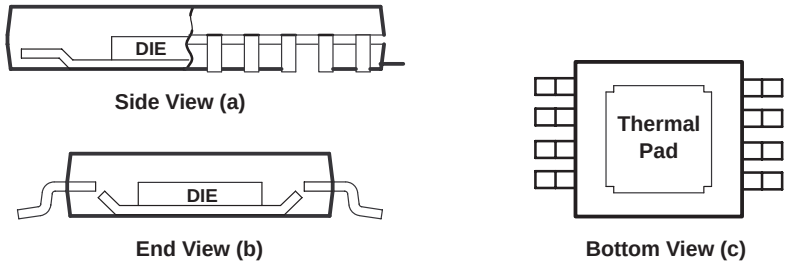
The THS4601 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted (see Figure 39). This arrangement results in the lead frame exposed as a thermal pad on the underside of the package. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. The PowerPAD is electrically insulated from the amplifier circuitry, but connection to the ground plane is recommended due to the high thermal mass typically associated with a ground plane.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

PowerPAD design considerations (continued)



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 41. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

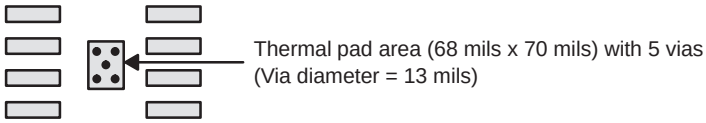


Figure 42. PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 42. There should be etch for the leads as well as etch for the thermal pad.
2. Place five vias in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes does not occur during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. Larger vias are permissible here because they are not susceptible to solder wicking as the vias underneath the device.
4. Connect all vias to the internal ground plane for best thermal characteristics
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

evaluation module and applications support

An evaluation board is available for quick laboratory verification of performance. An evaluation module can be ordered from Texas Instruments' web site (www.ti.com) or from your local TI sales representative. Applications support is also available for designers. The Product Information Center (PIC) can put designers in touch with applications engineers at Texas Instruments. The PIC be contacted via the web site as well.

additional reference material

- *PowerPAD Made Easy*, application brief, Texas Instruments Literature Number SLMA004.
- *PowerPAD Thermally Enhanced Package*, technical brief, Texas Instruments Literature Number SLMA002.
- *Noise Analysis of FET Transimpedance Amplifiers*, application bulletin, Texas Instruments Literature Number SBOA060.
- *Tame Photodiodes With Op Amp Bootstrap*, application bulletin, Texas Instruments Literature Number SBBA002.
- *Designing Photodiode Amplifier Circuits With OPA128*, application bulletin, Texas Instruments Literature Number SBOA061.
- *Photodiode Monitoring With Op Amps*, application bulletin, Texas Instruments Literature Number SBOA035.
- *Comparison of Noise Performance Between a FET Transimpedance Amplifier and a Switched Integrato*r, Application Bulletin, Texas Instruments Literature Number SBOA034.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4601CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4601C	Samples
THS4601ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4601I	Samples
THS4601IDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	4601I	Samples
THS4601IDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	4601I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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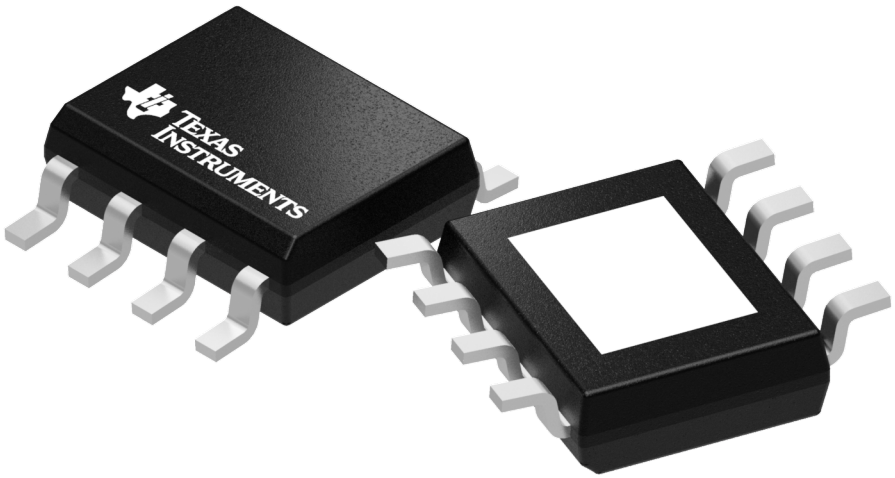
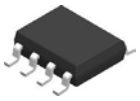
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

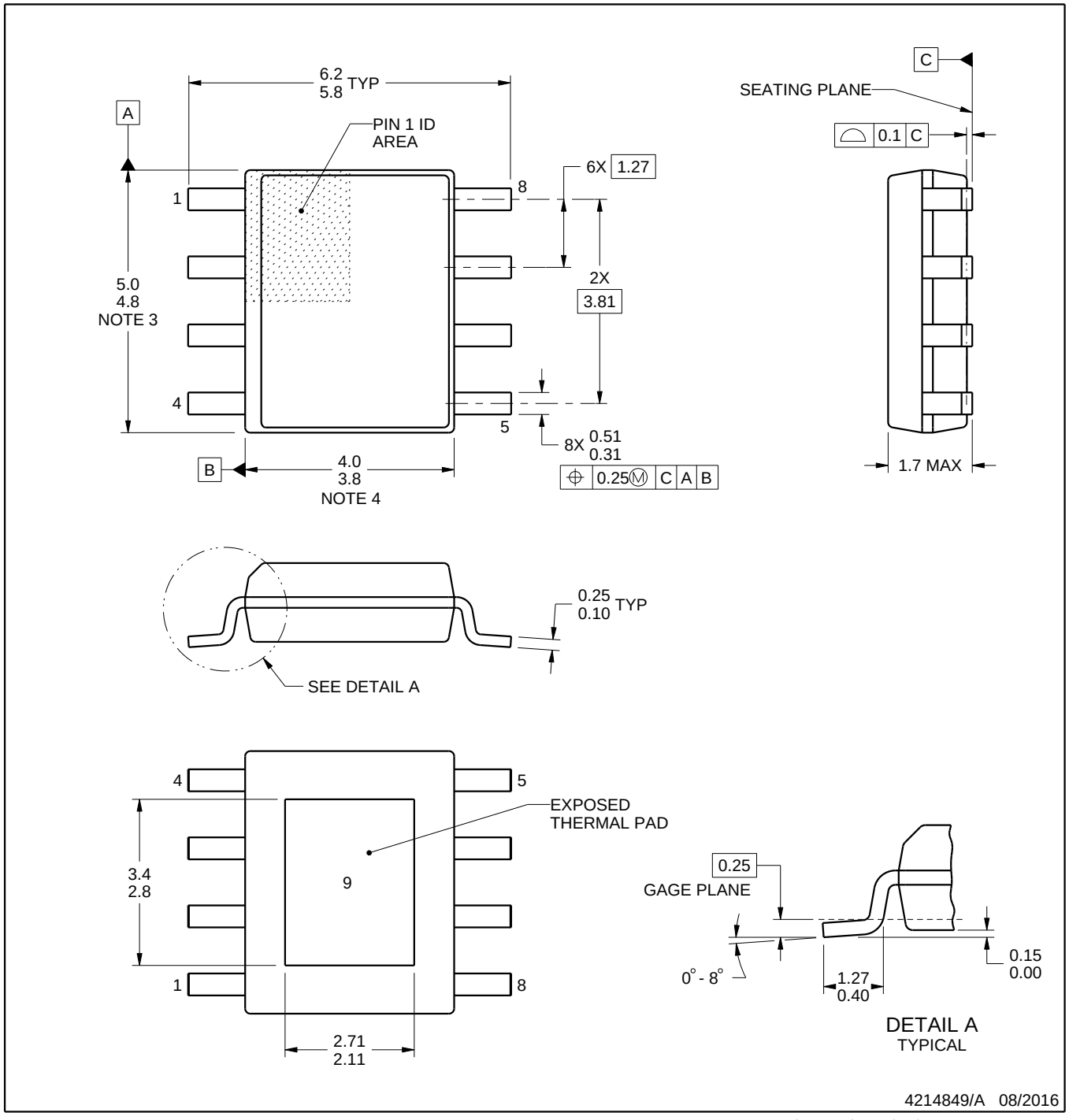


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

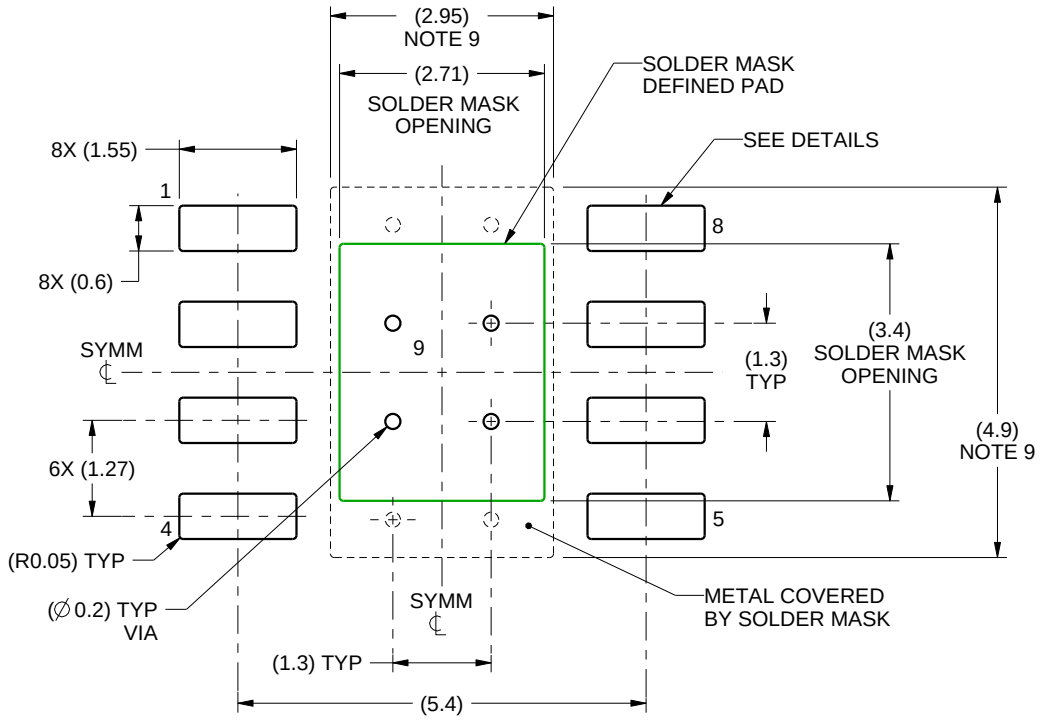
PLASTIC SMALL OUTLINE



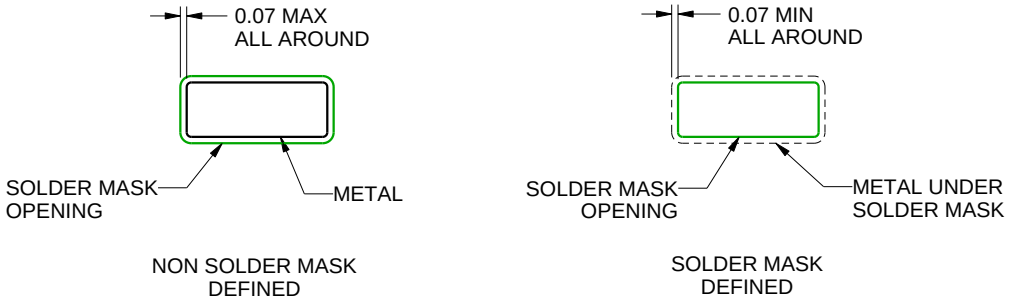
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

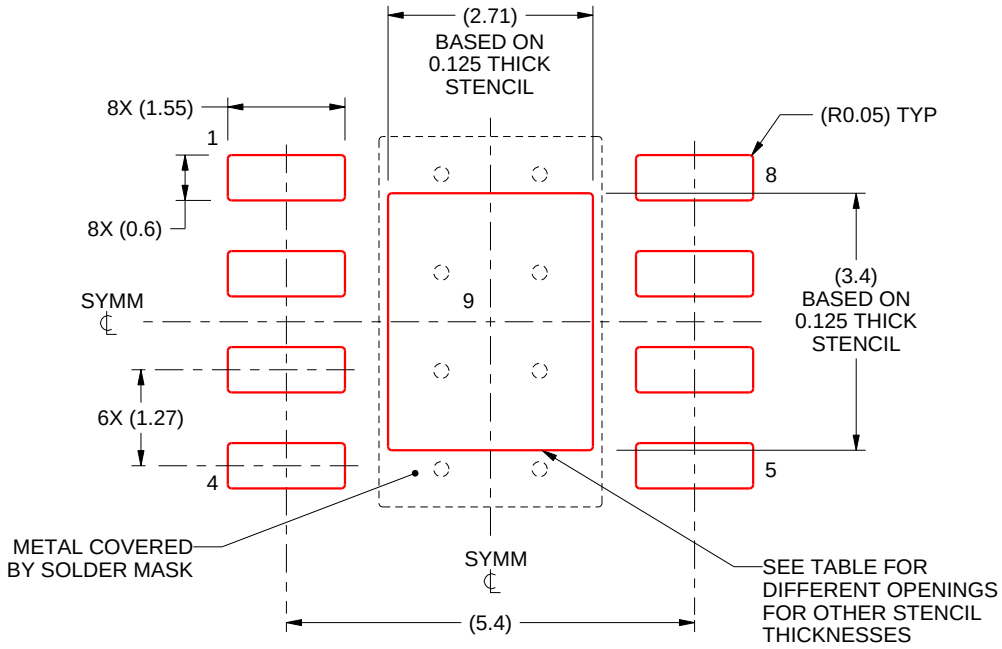
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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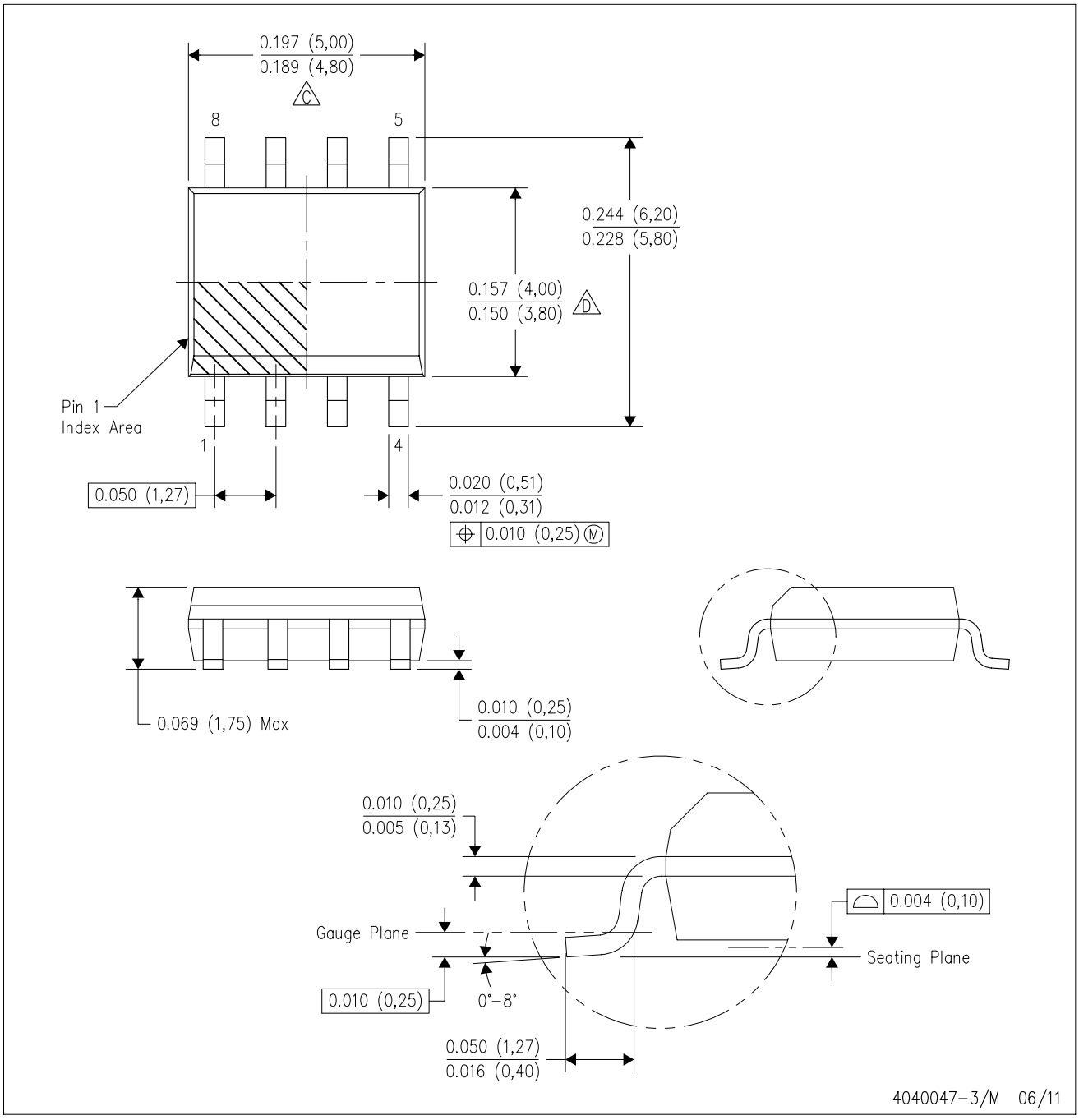
NOTES: (continued)

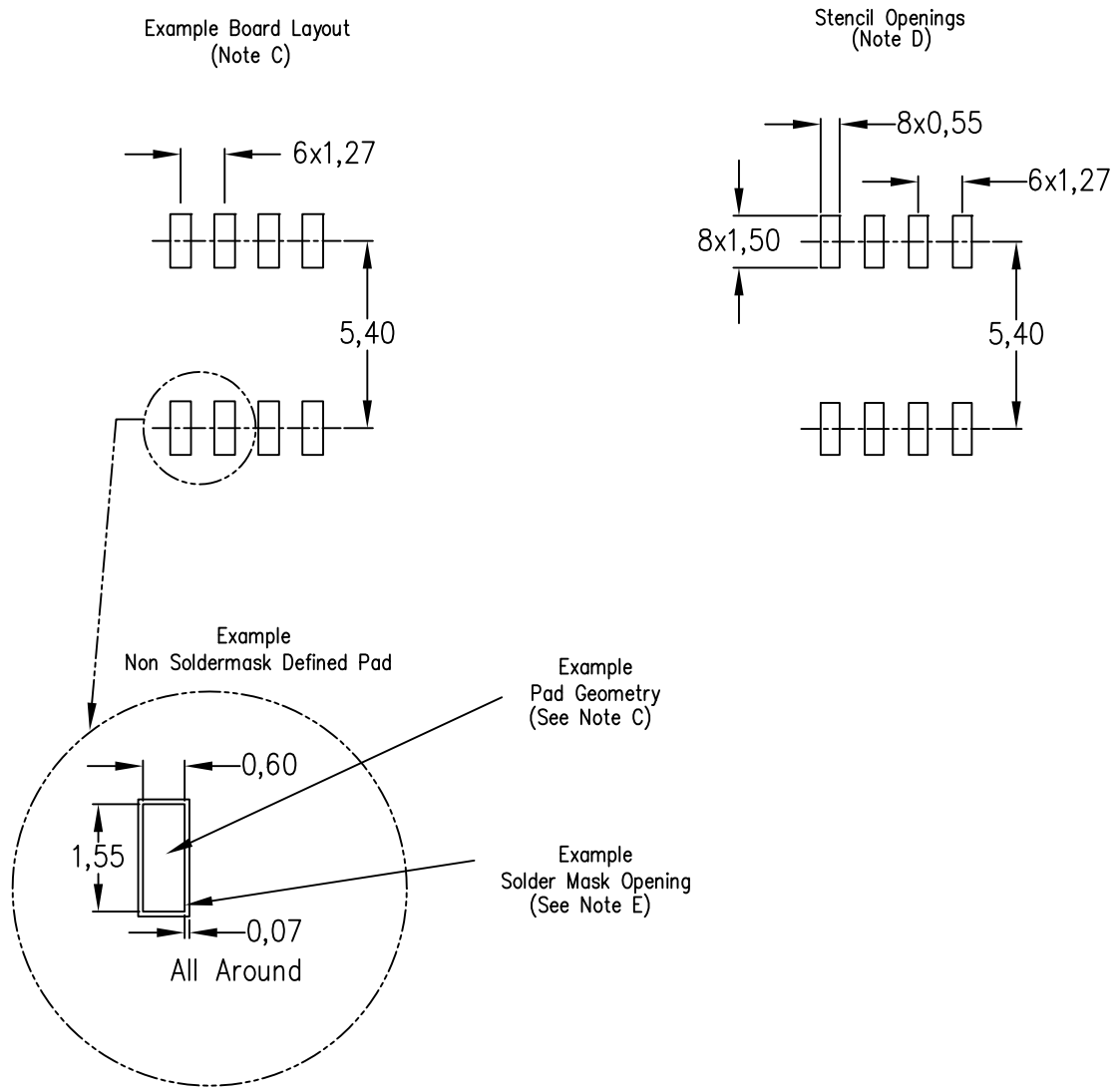
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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