ad semiconductor

ASRG08-QC, QD

8-Ch Auto Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION
PRELIMINARY

February 2009

1 Specification

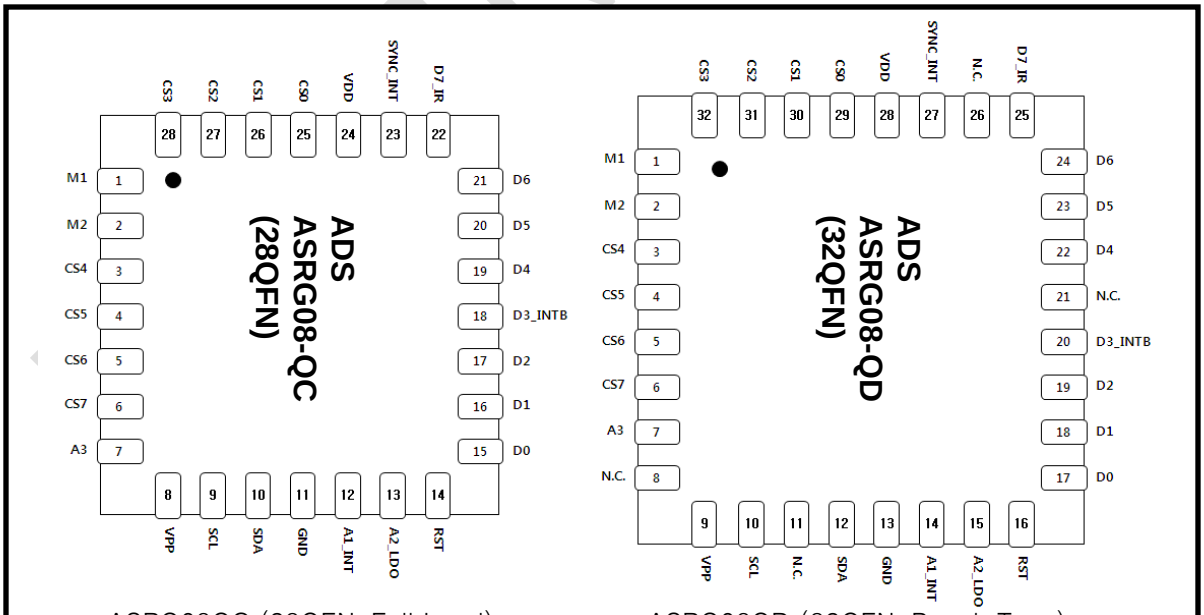
1.1 General Feature

- 8-Channel capacitive sensor with auto sensitivity calibration
- Available LED PWM drive up to 16 / 2-color LED PWM drive up to 8
- Multi interface (Parallel outputs / I^2C serial interface / Analog outputs)
- Programmable analog outputs
- Selectable output operation mode (Single output /Multi output)
- Selectable output logic level (Active high / Active low)
- Uniformly adjustable 64 steps sensitivity
- No IR interference from sensing operation signal
- Almost no external component needed
- Low current consumption
- Embedded common and normal noise elimination circuit
- RoHS compliant 28QFN (Full lead type) and 32QFN (Punch type) package

1.2 Application

- Home appliances (TV, Monitor keypads)i
- Mobile applications (PMP, MP3, Car navigation)
- Membrane switch replacement
- Sealed control panels, keypads
- Touch screen replacement application

1.3 Package (28QFN/32QFN)



ASRG08QC (28QFN-Full Lead) ASRG08QD (32QFN-Punch Type)

※ Drawings not to scale

2 Pin Description

VDD, GND
Supply voltage and ground pin

CS0~CS7
Capacitive sensor input pins.

VPP
VPP is external supply voltage for OTP writing.

RST
System reset input pin. High digital level on this pin makes internal system reset signal. ASRG08 has another internal reset block which is for the power reset. So, RST connection is not always necessary and in case of not use, this pin must be not connected to any circuitry.

A1_INT
Programmable 32 levels analog output pin1 / Touch sensing interrupt output pin. User can select A1_INT function by "**global_ctrl3**"[1] register setting. Analog output voltage level and CS allocation of A1_INT is controlled by "Analog output control register[2]" setting.

A2_LDO
Programmable 32 levels analog output pin2 / LDO on-off control output pin for MCU wake-up. User can select A2_LDO function by "**global_ctrl2**"[3] register setting. Analog output voltage level and CS allocation of A2_LDO is controlled by "Analog output control register[2]" setting.

A3
Programmable 32 levels analog output pin3. Analog output voltage level and CS allocation of A3 is controlled by "Analog output control register[2]" setting.

D0~D7
Parallel output ports of CS0~CS7 respectively / LED PWM drive output ports. The structure of these parallel output ports are can be selected open drain NMOS for active low output level operation as well as open drain PMOS for active high output level operation. Special function of D3 is for the touch sensing interrupt output. Special function of D7 is for the IR operation period input. User can control these pins by "**global_ctrl2**" register[3] setting.

SCL, SDA
SCL is I^2C clock input pin and SDA is I^2C data input-output pin. These ports have internal pull-up resistor which can be activated by "**global_ctrl1**" register[4] setting.
In case of not use, this pin must be not connected to any circuitry.

SYNC_INT
Touch sensing interrupt output pin / LDO on-off control output pin / IR operation period input pin. User can control this pin by "**global_ctrl2**" register[3] setting.

M1, M2
2-color LED control pin. User can control this pin by "**global_ctrl2**" register[3] setting.

[1] Refer to the chapter 8.2.8. Global option control 3 register
[2] Refer to the chapter 8.2.14. Analog output control register
[3] Refer to the chapter 8.2.7. Global option control 2 register
[4] Refer to the chapter 8.2.6. Global option control 1 register

2.1 ASRG08-QC (28QFN package)

Pin No.	Name	I/O	Description	Protection
1	M1	Digital Output	2 Color LED Control Port 1. Push-Pull	VDD/GND
2	M2	Digital Output	2 Color LED Control Port 2. Push-Pull	VDD/GND
3	CS4	Analog Input	Capacitive sensor input4	VDD/GND
4	CS5	Analog Input	Capacitive sensor input5	VDD/GND
5	CS6	Analog Input	Capacitive sensor input6	VDD/GND
6	CS7	Analog Input	Capacitive sensor input7	VDD/GND
7	A3	Analog Output	32 level analog output3	VDD/GND
8	VPP	Power	External OTP writing Power (11.5V)	GND
9	SCL	Digital Input	I^2C clock input	VDD/GND
10	SDA	Digital Input / Output	I^2C data input-output Open drain NMOS structure	VDD/GND
11	GND	Ground	Supply ground	VDD
12	A1_INT	Analog Output	32 level analog output1 Touch sensing interrupt output2	VDD/GND
13	A2_LDO	Analog Output	32 level analog output2 LDO on-off control output1	VDD/GND
14	RST	Digital Input	External system reset input(High active)	VDD/GND
15	D0	Digital Output	Parallel output of CS0 (Active high/Active low) LED PWM drive output0 Open drain NMOS/ PMOS structure	VDD/GND
16	D1	Digital Output	Parallel output of CS1 (Active high/Active low) LED PWM drive output1 Open drain NMOS/ PMOS structure	VDD/GND
17	D2	Digital Output	Parallel output of CS2 (Active high/Active low) LED PWM drive output2 Open drain NMOS/ PMOS structure	VDD/GND
18	D3_INTB	Digital Output	Parallel output of CS3 (Active high/Active low) LED PWM drive output3 Touch sensing interrupt output1 Open drain NMOS/ PMOS structure	VDD/GND
19	D4	Digital Output	Parallel output of CS4 (Active high/Active low) LED PWM drive output4 Open drain NMOS/ PMOS structure	VDD/GND
20	D5	Digital Output	Parallel output of CS5 (Active high/Active low) LED PWM drive output5 Open drain NMOS/ PMOS structure	VDD/GND
21	D6	Digital Output	Parallel output of CS6 (Active high/Active low) LED PWM drive output6 Open drain NMOS/ PMOS structure	VDD/GND
22	D7_IR	Digital Input / Output	Parallel output of CS7 (Active high/Active low) LED PWM drive output7 IR operation period input1	VDD/GND
23	SYNC_INT	Digital Input / Output	Touch sensing interrupt output3 LDO on-off control output2 IR operation period input2 Open drain NMOS structure	VDD/GND
24	VDD	Power	Power (2.5V~5.5V)	GND
25	CS0	Analog Input	Capacitive sensor input0	VDD/GND
26	CS1	Analog Input	Capacitive sensor input1	VDD/GND
27	CS2	Analog Input	Capacitive sensor input2	VDD/GND
28	CS3	Analog Input	Capacitive sensor input3	VDD/GND

2.2 ASRG08-QD (32QFN package)

Pin No.	Name	I/O	Description	Protection
1	M1	Digital Output	2 Color LED Control Port 1. Push-Pull, GPIO	VDD/GND
2	M2	Digital Output	2 Color LED Control Port 2. Push-Pull, GPIO	VDD/GND
3	CS4	Analog Input	Capacitive sensor input4	VDD/GND
4	CS5	Analog Input	Capacitive sensor input5	VDD/GND
5	CS6	Analog Input	Capacitive sensor input6	VDD/GND
6	CS7	Analog Input	Capacitive sensor input7	VDD/GND
7	A3	Analog Output	32 level analog output3	VDD/GND
8	N.C.	-	No Connection	-
9	VPP	Power	External OTP writing Power (11.5V)	GND
10	SCL	Digital Input	I^2C clock input	VDD/GND
11	N.C.	-	No Connection	-
12	SDA	Digital Input / Output	I^2C data input-output Open drain NMOS structure	VDD/GND
13	GND	Ground	Supply ground	VDD
14	A1_INT	Analog Output	32 level analog output1 Touch sensing interrupt output2	VDD/GND
15	A2_LDO	Analog Output	32 level analog output2 LDO on-off control output1	VDD/GND
16	RST	Digital Input	External system reset input(High active)	VDD/GND
17	D0	Digital Output	Parallel output of CS0 (Active high/Active low) LED PWM drive output0 Open drain NMOS/ PMOS structure	VDD/GND
18	D1	Digital Output	Parallel output of CS1 (Active high/Active low) LED PWM drive output1 Open drain NMOS/ PMOS structure	VDD/GND
19	D2	Digital Output	Parallel output of CS2 (Active high/Active low) LED PWM drive output2 Open drain NMOS/ PMOS structure	VDD/GND
20	D3_INTB	Digital Output	Parallel output of CS3 (Active high/Active low) LED PWM drive output3 Touch sensing interrupt output1 Open drain NMOS/ PMOS structure	VDD/GND
21	N.C.	-	No Connection	-
22	D4	Digital Output	Parallel output of CS4 (Active high/Active low) LED PWM drive output4 Open drain NMOS/ PMOS structure	VDD/GND
23	D5	Digital Output	Parallel output of CS5 (Active high/Active low) LED PWM drive output5 Open drain NMOS/ PMOS structure	VDD/GND
24	D6	Digital Output	Parallel output of CS6 (Active high/Active low) LED PWM drive output6 Open drain NMOS/ PMOS structure	VDD/GND
25	D7_IR	Digital Input / Output	Parallel output of CS7 (Active high/Active low) LED PWM drive output7 IR operation period input1	VDD/GND
26	N.C.	-	No Connection	-
27	SYNC_INT	Digital Input / Output	Touch sensing interrupt output3 LDO on-off control output2 IR operation period input2 Open drain NMOS structure	VDD/GND
28	VDD	Power	Power (2.5V~5.5V)	GND
29	CS0	Analog Input	Capacitive sensor input0	VDD/GND
30	CS1	Analog Input	Capacitive sensor input1	VDD/GND
31	CS2	Analog Input	Capacitive sensor input2	VDD/GND
32	CS3	Analog Input	Capacitive sensor input3	VDD/GND

3 Absolute Maximum Rating

Battery supply voltage	6V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note : Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	Pos / Neg	600V	VDD
		625V	VSS
		500V	P to P
C.D.M	-	1000V	Field Induced Charge

4.2 Latch-up Characteristics

Mode	Polarity	Max	Reference
I Test	Positive	100mA	JESD78A
	Negative	−100mA	
V supply over 5.0V	Positive	14.0V	

5 Electrical Characteristics

▪ **Note :** V_{DD}=3.3V, Typical system frequency (Unless otherwise noted), T_A = 25℃

Characteristics	Symbol	Test Condition		Min	Typ	Max	Units
Power supply requirement and current consumption							
Operating voltage	V_{DD}			2.5	3.3	5.5	V
OTP writing voltage	V_{PP}			11	11.5	12	V
Current consumption	I_{DD}	V_{DD} = 3.3V	Slow calibration speed[5]	–	55	85	μA
			Normal calibration speed	–	90	120	
			Fast calibration speed	–	160	210	
		V_{DD} = 5.0V	Slow calibration speed	–	80	130	
			Normal calibration speed	–	120	180	
			Fast calibration speed	–	210	280	
Reset and input level							
Internal reset voltage	V_{DD_RST}	T_A = 25℃		–	1.8	2.0	V
Input high level	VIH	| I_{IH} | ≤ +5μA		V_{DD}*0.7		V_{DD}+0.3	V
Input low level	VIL	| I_{IL} | ≤ +5μA		-0.3		V_{DD}*0.3	V
Self calibration time after system reset	T_{CAL}	Slow calibration speed		–	100	–	msec
		Normal calibration speed		–	80	–	
		Fast calibration speed		–	60	–	
Internal P/U resister of SDA and SYNC_INT	$R_{P/U}$			–	30	–	kΩ
Touch sensing performance							
Minimum detective capacitance difference	ΔC_{MIN}			0.1	–	–	pF
Sense input capacitance range[6]	C_S			–	–	50	pF
Output impedance (open drain)	Zo	$\Delta C > \Delta C_{MIN}$		–	12	–	Ω
		$\Delta C < \Delta C_{MIN}$		–	30M	–	
System performance							
Max. output current (LED drive current)	I_{OUT}	Per unit drive output port		–	–	8.0	mA
LED PWM control[7]	N_{PWM}			–	16	–	step
2 color LED control[7]				–	256	–	color
Sensitivity control[8]				–	64	–	step
Analog output voltage steps[9]	ΔV_{AO}			–	V_{DD}/32	–	V
Max. I^2C SCL clock speed	f_{SCL_MAX}	Maximum internal I^2C clock		–	–	2	MHz
Touch expired time	T_{EX}	Normal calibration speed		–	30	–	sec
LDO control output high level(A1_INT, A2_LDO)	V_{OH}			V_{DD}*0.9	–	–	V
LDO control output high level(A1_INT, A2_LDO)	V_{LH}			–	–	V_{DD}*0.1	V

[5] Slow calibration speed isn't recommended if it has not problem of current consumption.

[6] The sensitivity can be decreased with higher parallel capacitance of CS pin including parasitic capacitance made by neighbor GND or other pattern. The series resistor(under 1kΩ) of CS can be used in noisy condition to avoid mal-function from external surge and ESD.

[7] Refer to the chapter 8.2.7. Global option control 2 register
Refer to the chapter 8.2.13. 2-color LED luminance control register

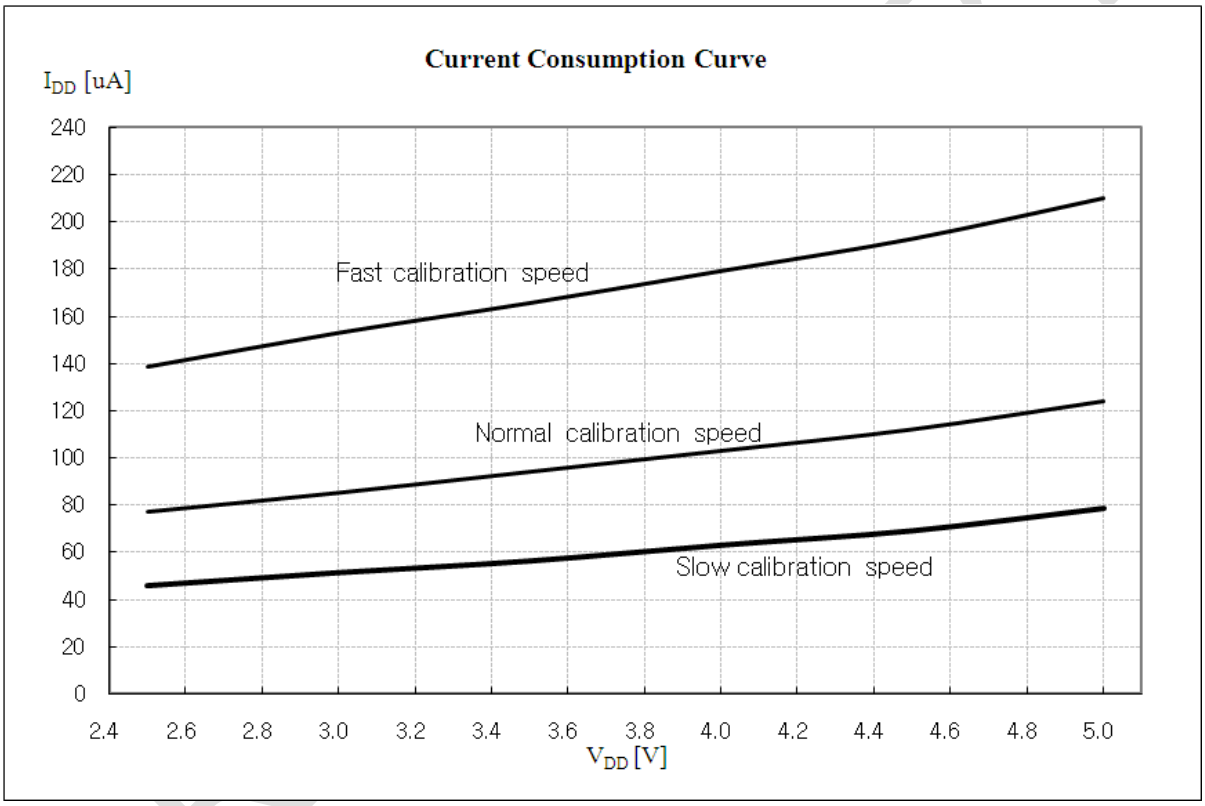
[8] Refer to the chapter 8.2.11. Sensitivity register

[9] Refer to the chapter 8.2.14. Analog output control register

6 ASRG08 Implementation

6.1 Typical current consumption

ASRG08 uses internal bias circuit, so internal clock frequency and current consumption is fixed and no external bias circuit is needed. ASRG08 has three optional calibrations speed. Faster calibration speed needs more current consumption than normal or slower calibration speed. Internal clock frequency and calibration speed can be changed by I^2C register setting[10]. Slow calibration speed isn't recommended if it has not problem of current consumption. The typical current consumption curve of ASRG08 is represented in accordance with V_{DD} voltage as below. Internal bias circuit can make the circuit design simple and reduce external components.



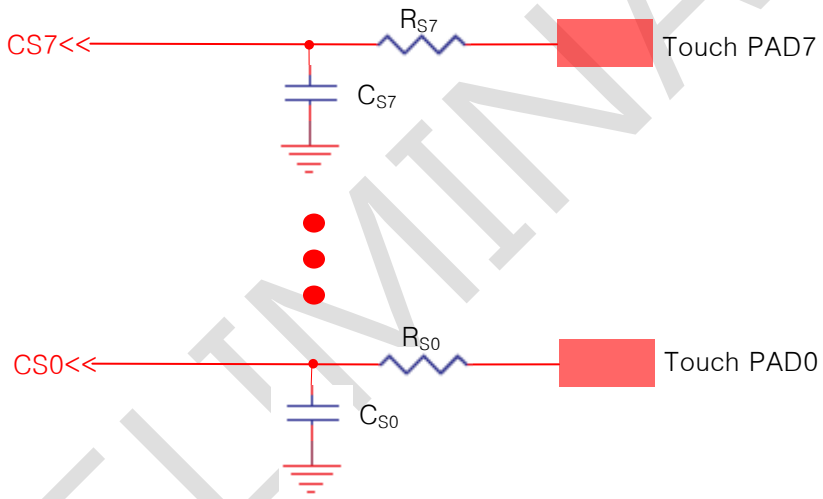
Typical current consumption curve of ASRG08

[10] Refer to 8.2.6 Global option control 1

6.2 CS implementation

ASRG08 has 64 step selections of sensitivity and internal surge protection resister. Sensitivity of each sensing channel (CS) can be independently controlled on others. External components of CS pin such as series resistor or parallel capacitor isn't necessary. The parallel parasitic capacitance of CS pins caused by touch line, touch pad and neighbor GND or other pattern may affect sensitivity. The sensitivity will be decreased when bigger parallel parasitic capacitance of CS pin is added.

Parallel capacitor ($C_{S0\sim S7}$) of CS pin is useful in case of detail sensitivity mediation is required such as for complementation sensitivity difference between channels. Same as above parallel parasitic capacitance, sensitivity will be decreased when a big value of parallel capacitor ($C_{S1\sim S8}$) is used. Under 50pF capacitor can be used as sensitivity meditation capacitor and a few pF is usually used. The R_S, serial connection resistor of CS pins, may be used to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. Refer to below CS pins application figure.

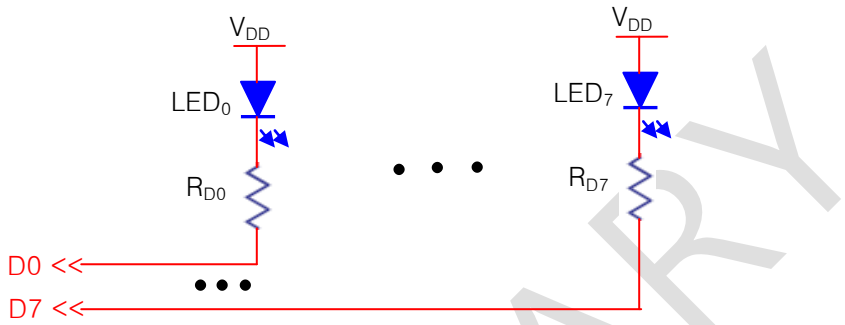


The ASRG08 has eight independent touch sensor input from CS0 to CS7. The internal touch decision process of each channel is separated from others. Therefore eight channel touch key board application can be designed by using only one ASRG08 without coupling problems.

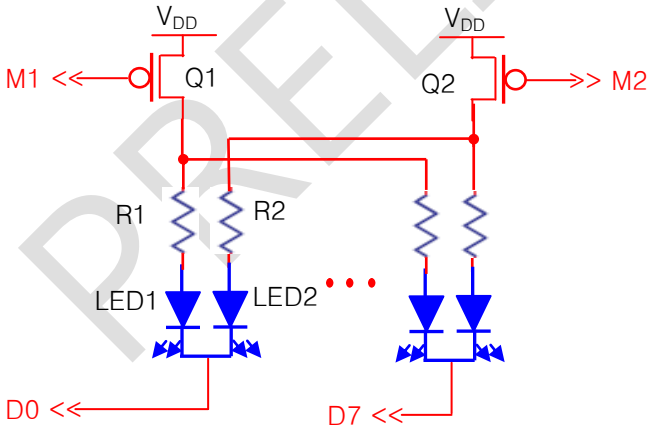
The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.

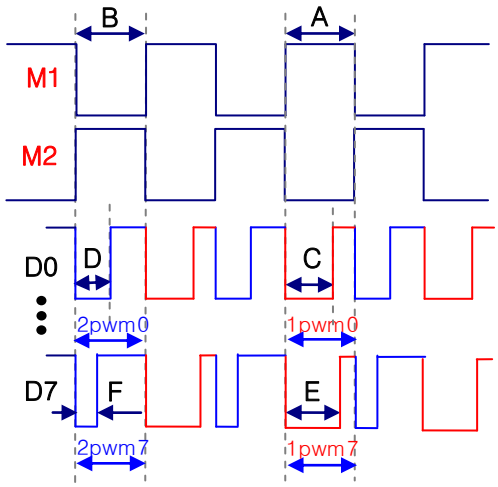
6.3 LED drive & 2-color LED drive (M1, M2, D0~D7 implementation)

ASRG08 has a function to control the LED, and 2-color LED using D0~D7, M1, M2 ports. For using D0~D7 as LED driver ports, LEDs and resisters must be equipped as below figure, and write the **'par_output_mode'** bit of **'global_ctrl2'** register[11] as **'0'**. D0 ~ D7 ports can drive LEDs by **'LED enable'** register[12] control. ASRG08 can drive up to 8 LED as below method.



In the case of 2-color LED drive M1, M2 and D0~D7 must be equipped as below figure, and write the **'par_output_mode'** bit of **'global_ctrl2'** register as **'0'** and the **'pwm_sel'** bit of **'global_ctrl2'** register as **'1'**. M1 and M2 have alternatively high and low pulse and the pulse duty is 50%. During M1 is high M2 is low, D0~D7 has 1pwm pulse of each D0~D7. During M1 is low M2 is high, D0~D7 has 2pwm pulse of each D0~D7.
During period 'A' M1 is high and M2 is low, Q1 is turned off and Q2 is turned on. So, LED2 is turned on during 1pwm low period 'C(E)'. During period 'B' M2 is high and M1 is low, Q1 is turned on and Q2 is turned off. So, LED1 is turned on during 2pwm low period 'D(F)'. Duty of M1 signal and M2 signal is fixed as 50%. But duty of 1pwm signal and 2pwm signal of each D0~D7 can be independently controlled by **'1pwmx'**, **'2pwmx'** (1pwm0 means 1pwm of D0) registers[13] by 16 steps. As the result, 2-color LED can get 256(16x16) colors by resister control. In addition, same method of above description ASRG08 can drive single LED up to sixteen.

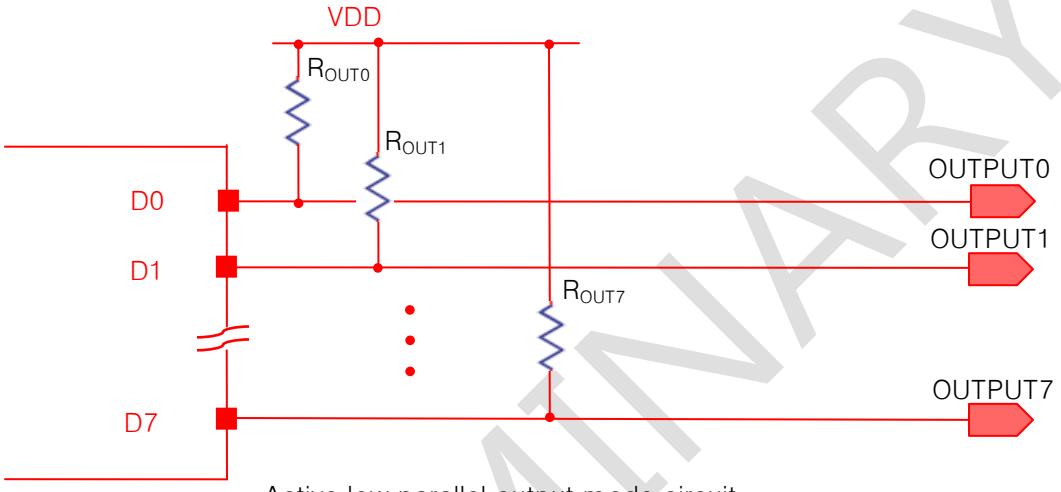




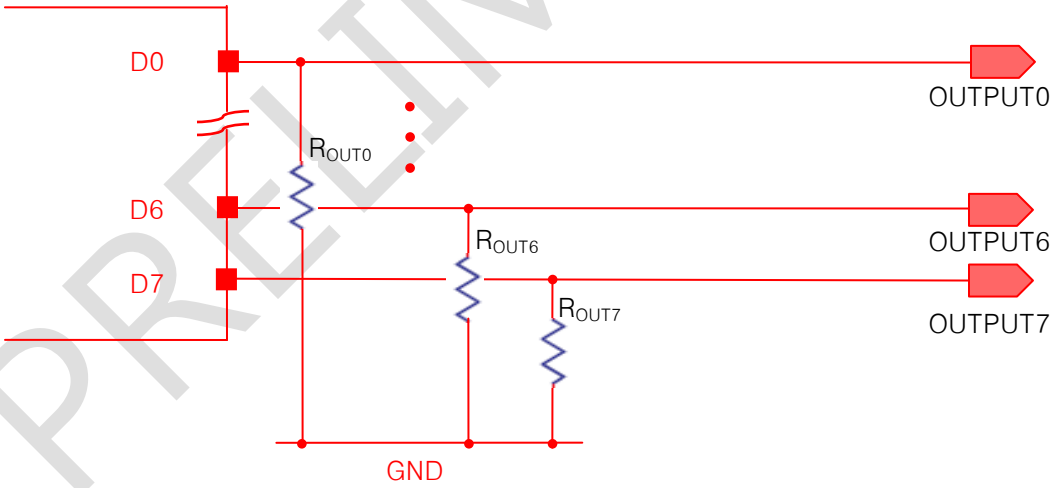
[11] Refer to the chapter 8.2.7.
[12] Refer to the chapter 8.2.4.
[13] Refer to the chapter 8.2.14, x means channel 1 ~ channel 8.

6.4 Parallel output (D0~D7 implementation)

ASRG08 has 2 parallel output mode controlled by 'par_output_pol' bit of 'global_ctrl2' register[14] setting. One is active high parallel output mode and the other is active low parallel output mode. Structures of D0~D7 are same. In case of active high parallel output mode, parallel output ports (D0~D7) have an open drain PMOS structure. In other case of active low parallel output mode, parallel output ports (D0~D7) have an open drain NMOS structure. For this reason, both parallel output modes of ASRG08 need R_{OUT} as below figures. The maximum output drive current is 8mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}.



Active low parallel output mode circuit

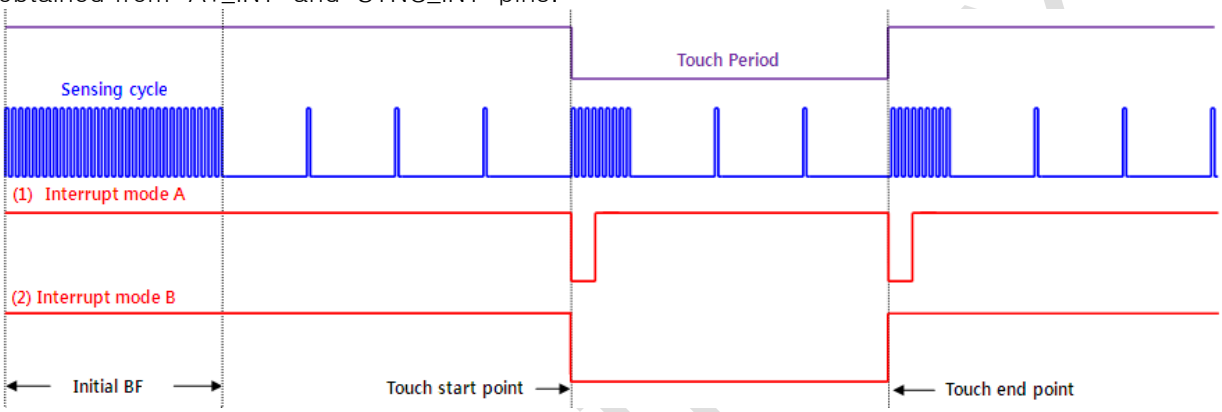


Active high parallel output mode circuit

[14] Refer to the chapter 8.2.7. Global option control 2.

6.5 Special function of D3_INTB (Interrupt output)

Special function of D3_INTB is for the touch sensing interrupt output. Functions of D3_INTB can be controlled by **'global_ctrl2'** register[15] setting. There are two interrupt operation is possible and can be selected by **'global_ctrl3'** register[16] setting. In first interrupt operation case, the interrupt pulse is generated only during short period of every each channel touch start points and touch end point. In other interrupt operation case, the interrupt pulse is generated during every each channel touch duration. Interrupt pulse has logical low level in both two interrupt modes. Pull-up resister about a few kΩ is required for interrupt output. These interrupt functions can be obtained from 'A1_INT' and 'SYNC_INT' pins.



6.6 Special function of D7_IR (IR sync input)

Special function of D7_IR is for IR sync input. Functions of D7_IR can be controlled by **'global_ctrl2'** register setting. In case of application with infrared receiver (IR) circuit, IR operation signal can be input to D7_IR pin to prevent from interference caused by capacitive touch sensing signal or other system noise. Logical low level signal input in IR input mode makes all operation of touch sensor stop and wait until 90msec after this IR input change to logical high when **'ir_time_ctrl'** bits of **'global_ctrl3'** register[16] are **'00'** or until 160msec after this IR input change to logical high when **'ir_time_ctrl'** bits of **'global_ctrl3'** register[16] are **'01'**. This IR sync input function can be obtained from 'SYNC_INT' pin also.

6.7 SYNC_INT implementation

SYNC_INT pin acts as touch sensing interrupt output pin, IR sync input pin, and LDO on-off control output pin. Role of SYNC_INT can be selected by **'global_ctrl2'** register[15] setting. Touch sensing interrupt output operation of SYNC_INT is same as that of D3_INTB. Because of internal pull-up resister of SYNC_INT which can be activated by **'global_ctrl1'** register[17] setting, external pull-up resister can be removed. IR sync input operation of SYNC_INT is exactly same as that of D7_IR. LDO on-off control output operation can help power saving in mobile application. Writing **'1'** on **'micom_sleep'** bit of **'global_ctrl0'** register[18] make SYNC_INT output low. This low

[15] Refer to the chapter 8.2.7. Global option control 2.
[16] Refer to the chapter 8.2.8. Global option control 3.
[17] Refer to the chapter 8.2.6. Global option control 1.
[18] Refer to the chapter 8.2.2. Global option control 0.

SYNC_INT output can be used as LDO which offers MCU power off signal. Any touch output writes '0' on 'micom_sleep' bit of 'global_ctrl0' register, and SYNC_INT output level becomes high again.

6.8 RST implementation

ASRG08 has both internal and external reset. Internal reset is for the power reset of initial power on time. External reset by RST pin input is for abrupt reset that is required for intensive system reset. If abrupt reset is not required, there is no need to use RST pin and this RST pin has only to be floating. High pulse signal of RST pin reset internal system.

6.9 Analog output implementation (A1_INT, A2_LDO, A3 implementation)

ASRG08 has three internal digital to analog converters (DAC) and three analog output ports. A1_INT, A2_LDO and A3 are these analog output ports. Channels (CS0~CS7) assignment to these analog output ports (A1_INT, A2_LDO, A3) is programmable by 'ad_sel0 ~ ad_sel7' bits of 'Aout0 ~ Aout7' registers[19] settings. And output analog voltage of every each channels is also programmable by 'adout_data0 ~ adout_data7' bits of 'Aout0 ~ Aout7' registers settings. Programmable DAC analog output voltage resolution is one over thirty two V_{DD}.

A1_INT has another operation of touch sensing interrupt output. This touch sensing interrupt output operation is same as that of D3_INTB and SYNC_INT. Because touch sensing interrupt output voltage level of A1_INT is obtained from DAC, A1_INT must be connected MCU input port without any pull-up/down circuitry. When 'ad1_int_sel' bit of 'global_ctrl2' register[20] is '1', A1_INT pin operates as touch sensing interrupt output port.

A2_LDO has another operation of LDO on-off control output. This LDO on-off control output operation is same as that of SYNC_INT. Because LDO on-off control output voltage level of A2_LDO is obtained from DAC, A2_LDO must be connected LDO on-off control input without any pull-up/down circuitry. When 'ad2_ldo_sel' bit of 'global_ctrl3' register[21] is '1', A2_LDO pin operates as LDO on-off control output port.

6.10 Change initial reset register values (OTP writing)

ASRG08 has eight integrated OTP (One Time Programmable) ROM cells. So, initial reset register values can be rewritten up to eight times. One OTP ROM cell size is 64-byte. User can write the data eight times to the OTP.

There are three operation modes about OTP read/write. These are automatically load operation mode, writing operation mode and reading operation mode.

Automatically load operation mode

After power reset, ASRG08 start to read the LSB of 00H address in each OTP ROM cells from 8th to 1st. ASRG08 automatically loads the data of the first OTP ROM cell of which LSB of 00H address has '0' into the control register. And then ASRG08 is starting to work with control register values that are loaded from OTP ROM cell. If there are no OTP ROM cell which has '0' in LSB of 00H address, ASRG08 is working with initial control register value.

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[19] Refer to the chapter 8.2.14. Analog output control register.

[20] Refer to the chapter 8.2.7. Global option control 2.

[21] Refer to the chapter 8.2.8. Global option control 3.

Writing operation mode

OTP ROM cell writing provides the flexible reset register values that control all the operation options of ASRG08. So, additional communication programs on MCU for operation option select or register value setting are not required.

There are two writing operation modes. When the 'write_all' bit of 'mtp_cmd' register[22] is '0', single byte writing mode is activated. User can select OTP ROM cell and address on which new register value is wanted to be written. OTP ROM cell selection is enabled by writing 'mtp_sel_en' bit of 'usr_mtp_sel' register[23] '1'. When 'mtp_sel_en' bit of 'usr_mtp_sel' register is '0', OTM ROM cell is automatically selected from 1st to 8th. And, 'org_usr_mtp_sel' bits of 'usr_mtp_sel' register are for the OTP ROM selection. Read or write command register is 'mtp_cmd' registers and user can start writing by 'wr_start' bit of 'mtp_cmd' register setting as '1'. This 'wr_start' bit of 'mtp_cmd' register is recovered as '0' at ending of writing.

When the 'write_all' bit of 'mtp_cmd' register is '1', all bytes writing operation mode is activated. User can write all register frame data on selected OTP ROM cell. At this writing operation mode, only OTP ROM cell has to be selected. Writing start is same as single byte writing mode.

OTP ROM writing needs another 11.5V power supply voltage. VPP pin is for this writing 11.5V power.

Reading operation mode

When OTP ROM data is required to be read, user can read all the OTP ROM cell date by reading operation. When the 'read_all' bit of 'mtp_cmd' register is '0', user can read one byte data that is written on selected address of selected OTP ROM cell. OTP ROM cell and address selection are same as single byte writing operation mode. When 'mtp_sel_en' bit of 'usr_mtp_sel' register is '0', OTM ROM cell is automatically selected from 8th to 1st.

When the 'read_all' bit of 'mtp_cmd' register is '1', user can read all data on selected OTP ROM cell.

OTP ROM read start command bit is 'rd_start' bit of 'mtp_cmd' register. When the 'rd_start' bit of 'mtp_cmd' register is '1', ASRG08 starts to read. This 'rd_start' bit of 'mtp_cmd' register is recovered as '0' at ending of reading.

6.11 SCL, SDA implementation

SCL is I^2C clock input and SDA is I^2C data input-output. These ports have internal pull-up resistor which can be activated by 'global_ctrl1' register[24] setting. SCL has Schmitt trigger input structure to prevent clock signal from being broken. Maximum supported I^2C clock frequency is 2MHz. SDA has NMOS open drain structure and internal pull-up resister of which value is 30kΩ typical. So, according to communication speed a few kΩ resister must be used as pull-up resister for proper data pulse rising time. For more details refer to 'Chapter 7. I^2C Interface'.

[22] Refer to the chapter 8.2.17. OTP ROM control register.

[23] Refer to the chapter 8.2.17. OTP ROM cell select register.

[24] Refer to the chapter 8.2.6. Global option control 1.

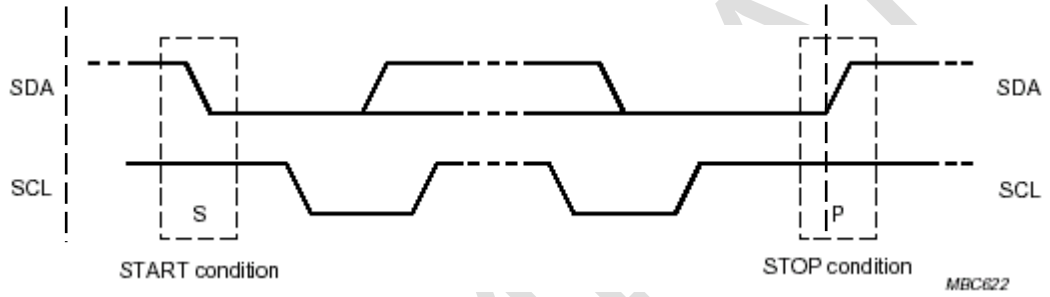
7 I²C Interface

7.1 I²C Enable / Disable

If the SDA or SCL signal goes to low, I²C control block is enabled automatically. And if the SDA and SCL signal maintain high during about 2 us, I²C control block is disabled automatically also.

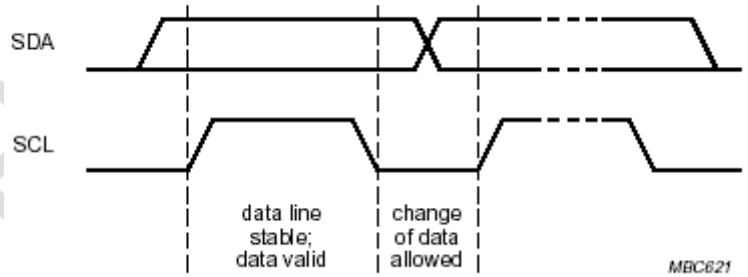
7.2 Start & stop condition

- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

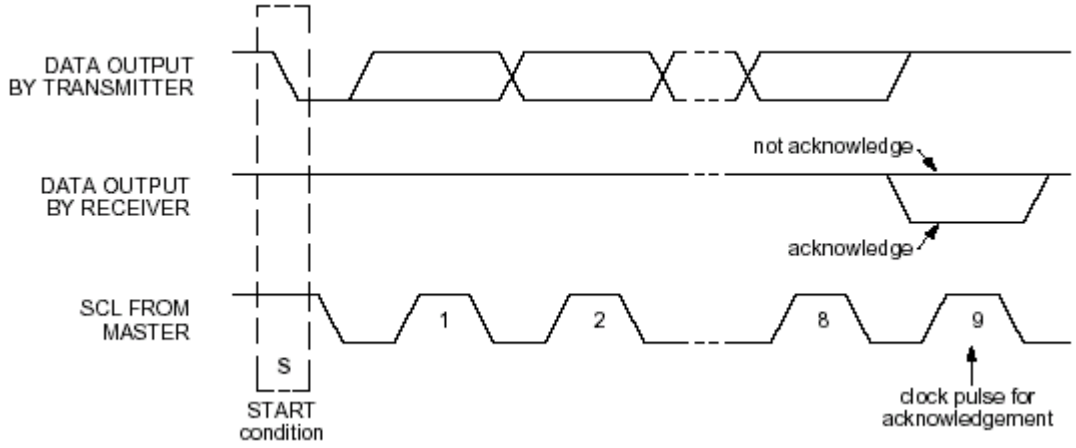


7.4 Byte format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write **'0'** when it received the data successfully and **'1'** if not.



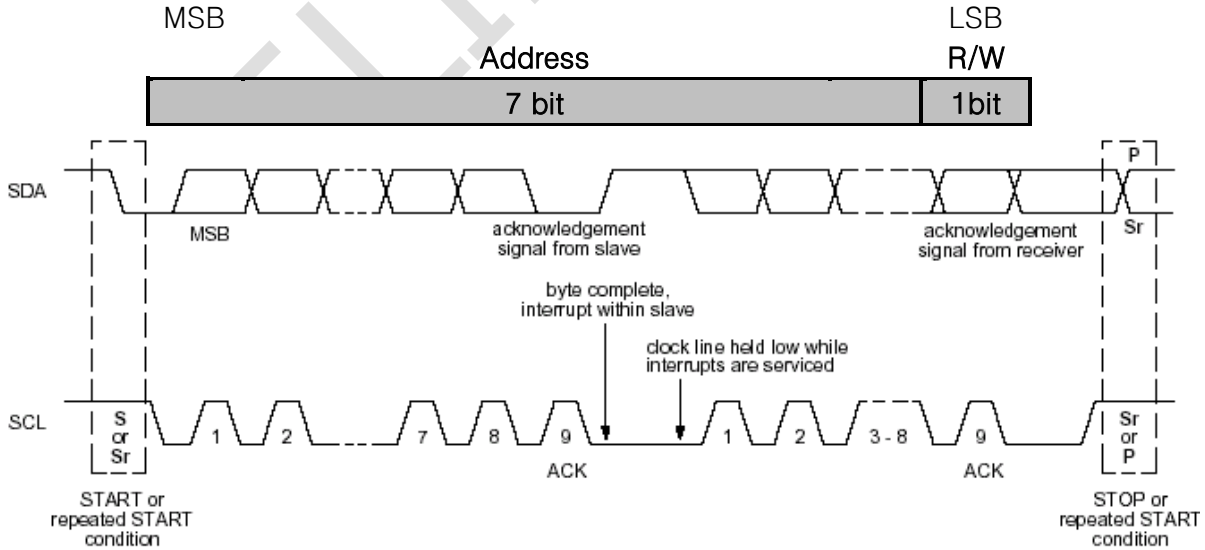
7.6 First byte

7.6.1 Slave address

It is the first byte from the start condition. It is used to access the slave device. The initial chip address of ASRG08 is **'48'** hex number and the chip address is possible to change with "I^2C Address of ASRG08" register[25].

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.



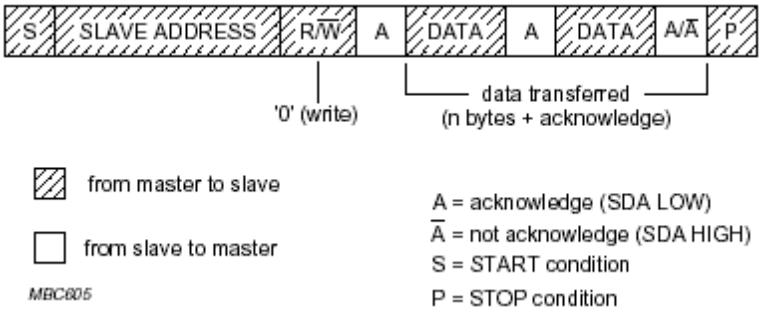
[25] Refer to the chapter 8.2.3.

7.7 Transferring data

7.7.1 Write operation

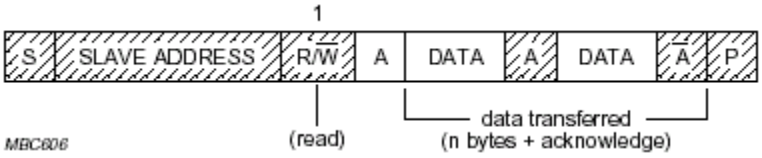
The byte sequence is as follows:

1. The first byte gives the device address plus the direction bit (R/W = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Following bytes are written in successive internal registers.
4. The transfer lasts until stop conditions are encountered.
5. The ASRG08 acknowledges every byte transfer.

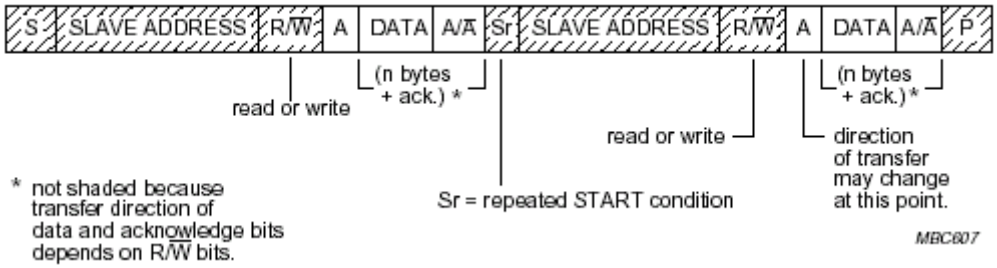


7.7.2 Read operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.7.3 Read/Write Operation



7.8 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0x48	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

Read register 0x00 and 0x01

Start	Device Address 0x48	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0x49	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave From Slave to Master

8 ASRG08 Control Register List

◂ Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Bit name of each bytes							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ch_enable /soft_rst	01H	1111 1111	ch7_en	ch6_en	ch5_en	ch4_en	ch3_en	ch2_en	ch1_en	ch0_en
global_ctrl0	05H	---- 0--0	-	-	-	-	micom_sleep	-	-	bf_option
i2c_id	06H	0100 1000	i2c_id							wr_bit
LED_enable	07H	0000 0000	dl7_en	dl6_en	dl5_en	dl4_en	dl3_en	dl2_en	dl1_en	dl0_en
output	2AH	0000 0000	o_ch7	o_ch6	o_ch5	o_ch4	o_ch3	o_ch2	o_ch1	o_ch0
global_ctrl1	34H	0000 1010	syn_pu_up	sda_pu_up	imp_sel_opt	irb_mode	irb_sel		rb_sel	
global_ctrl2	35H	0100 0001	ad1_int_sel	int_pin_sel		d3_int_sel	d7_ir_sel	pwm_sel	par_output_pol	par_output _mode
global_ctrl3	36H	0001 0000	ad2_ldo_sel	int_out_mode	ir_time_ctrl		led_mode	0	0	0
global_ctrl4	37H	--00 1100	-	-	sts_clr_en	response_ctrl			clk_off	sw_rst
global_ctrl5	38H	0101 0100	cal_hold	sin_multi_mode	cal_hold_time				exp_op_en	exp_op_mode
Sensitivity0	39H	--00 1001			sensitivity00					
Sensitivity1	3AH	--00 1001	-	-	sensitivity01					
Sensitivity2	3BH	--00 1001	-	-	sensitivity02					
Sensitivity3	3CH	--00 1001	-	-	sensitivity03					
Sensitivity4	3DH	--00 1001	-	-	sensitivity04					
Sensitivity5	3EH	--00 1001	-	-	sensitivity05					
Sensitivity6	3FH	--00 1001	-	-	sensitivity06					
Sensitivity7	40H	--00 1001	-	-	sensitivity07					
cal_speed	41H	1111 1010	bf_up		bf_down		bs_up		bs_down	
pwm0	43H	0000 0000	2pwm0				1pwm0			
pwm1	44H	0000 0000	2pwm1				1pwm1			
pwm2	45H	0000 0000	2pwm2				1pwm2			
pwm3	46H	0000 0000	2pwm3				1pwm3			
pwm4	47H	0000 0000	2pwm4				1pwm4			
pwm5	48H	0000 0000	2pwm5				1pwm5			
pwm6	49H	0000 0000	2pwm6				1pwm6			
pwm7	4AH	0000 0000	2pwm7				1pwm7			
Aout0	4BH	-001 1111	-	ad_sel0	adout_data0					
Aout1	4CH	-001 1111	-	ad_sel1	adout_data1					
Aout2	4DH	-001 1111	-	ad_sel2	adout_data2					
Aout3	4EH	-001 1111	-	ad_sel3	adout_data3					
Aout4	4FH	-001 1111	-	ad_sel4	adout_data4					
Aout5	50H	-001 1111	-	ad_sel5	adout_data5					
Aout6	51H	-001 1111	-	ad_sel6	adout_data6					
Aout7	52H	-001 1111		ad_sel7	adout_data7					

Name	Addr. (Hex)	Reset Value (Bin)	Bit name of each bytes							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
rd_ch_H1	53H	0000 0000	rd_ch_H1							
rd_ch_L1	54H	---- ---0	-	-	-	-	-	-	-	rd_ch_L1
sen_H	55H	--00 0000	-	-	sen_count[13:8]					
sen_L	56H	0000 0000	sen_count[7:0]							
ref_H	57H	--00 0000	-	-	ref_count[13:8]					
ref_L	58H	0000 0000	ref_count[7:0]							
rd_ch_H2	59H	0000 0000	rd_ch_H2							
rd_ch_L2	5AH	---- ---0	-	-	-	-	-	-	-	rd_ch_L2
usr_mtp_sel	5BH	0000 0000	0	0	0	mtp_sel_en	org_usr_mtp_sel			
mtp_cmd	5CH	0000 0000	0	0	write_all	read_all	0	0	wr_start	rd_start
mtp_status	5DH	---- ----	-	org_mtp_sel				wr_done_sts	rd_done_sts	no_load_sts
otp_add_sel	5EH	0000 0000	0	0	otp_add_sel					
otp_wr_data	5FH	0000 0000	otp_wr_data							
otp_rd_data	60H	---- ----	otp_rd_data							

8.2 Details

8.2.1 Channel enable / reset register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	**ch_enable /soft_rst**	ch7_en	ch6_en	ch5_en	ch4_en	ch3_en	ch2_en	ch1_en	ch0_en

Description
Enable, disable and reset of each channel control register.

Bit name	Reset value	Function
chx_en	1	Channel enable / disable and Channel reset (chx_en is control bit for CSx channel) 0 : Channel disable and sensing channel reset 1 : Channel enable

8.2.2 Global option control register 0

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	**global_ctrl0**	-	-	-	-	micom_ sleep	-	-	bf_opt

Description
Operation mode selection and LDO ON/OFF signal control register.

Bit name	Reset value	Function
bf_opt	0	Operation mode selection - 0 : Normal mode - 1 : BF mode
micom_ sleep	0	LDO output control register. This signal can go out through SYNC_INT port or A2_LDO port. For more details about selection LDO output port, Refer to chapter 8.2.7 and 8.2.8. - 0 : LDO ON - 1 : LDO OFF

8.2.3 I²C address of ASRG08

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	**i2c_id**	i2c_id							wr_bit

Description
Chip address of ASRG08 control register. User can change this address value with OTP ROM write. During reset period OTP ROM data is loaded to registers.

Bit name	Reset value	Function
wr_bit	0	Write/Read address selection - 0 : Write address, 1 : Read address
i2c_id	0100100	Chip address of ASRG08.

8.2.4 LED enable

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	**LED_enable**	dl7_en	dl6_en	dl5_en	dl4_en	dl3_en	dl2_en	dl1_en	dl0_en

Description
LED ON/OFF control registers of D0~D7. Firstly LSB of 35H must be '0'.

Bit name	Reset value	Function
dlx_en	0	LED enable control (dlx_en is LED enable bit for DX output port) - 0 : LED disable - 1 : LED enable

8.2.5 Output data

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	**output**	o_ch7	o_ch6	o_ch5	o_ch4	o_ch3	o_ch2	o_ch1	o_ch0

Description

The output data register from channel 0 to channel 7.

Bit name	Reset value	Function
o_chx	0	o_chx is output bit for CSx channel - 0 : No touch detected - 1 : Touch detected

8.2.6 Global option control 1

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	**global_ctrl1**	syn_pu_up	sda_pu_up	imp_sel_opt	irb_mode	irb_sel		rb_sel	

Description

This register controls the global options of ASRG08

Bit name	Reset value	Function
rb_sel	10	ASRG08 provides three internal calibration speeds and user can control the ASRG08 calibration speed by using these bits. - 00, 01 : Fast - 10 : Normal - 11 : Slow
[irb_mode : irb_sel]	010	ASRG08 provides six internal I^2C clock frequencies. Slower one reduces current consumption. - 000 : Fast - 001 : Faster - 010 , 011 : Fastest - 100 : Slowest - 101 : Slower - 110,111: Slow
imp_sel_opt	0	Impedance of the sensing wire of all channels control bit. - 0 : High impedance - 1 : Low impedance except sensing period.
sda_pu_up	0	Pull-up resistor enable control bit on the SDA port. - 0 : Disable pull-up resistor - 1 : Enable pull-up resistor
syn_pu_up	0	Pull-up resistor enable control bit on the SYNC_INT port. - 0 : Disable pull-up resistor - 1 : Enable pull-up resistor

8.2.7 Global option control 2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35h	**global_ctrl2**	ad1_int_sel	int_pin_sel		d3_int_sel	d7_ir_sel	pwm_sel	par_output_pol	par_output_mode

Description

This register controls the global options of ASRG08.

Bit name	Reset value	Function
par_output_mode	1	Parallel outputs enable bit. If user wants to use D0~D7 ports as LED PWM drive ports, this bit has to be '0'. - 0 : Disable parallel output mode - 1 : Enable parallel output mode
par_output_pol	0	Polarity of parallel outputs selection bit. - 0 : Active low - 1 : Active high
pwm_sel	0	LED PWM outputs enable bit. If user wants to use D0~D7 ports as a LED PWM drive ports, this bit has to be '1' under condition of the LSB of 35H is '0'. - 0 : Disable LED PWM output - 1 : Enable LED PWM output
d7_ir_sel	0	D7 port action selection bit. - 0 : Parallel output port of CS7 channel - 1 : IR input port
d3_int_sel	0	D3 port action selection bit. - 0 : Parallel output port of CS3 channel - 1 : Touch sensing interrupt output port
int_pin_sel	10	SYNC_INT port action selection bit. - 00 : Do not use - 01 : LDO output port - 10 : Interrupt output port - 11 : IR input port
ad1_int_sel	0	A1_INT port function selection bit. - 0 : Analog output port 1 - 1 : Touch sensing interrupt output port

8.2.8 Global option control 3

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	**global_ctrl3**	ad2_ldo_sel	int_out_mode	ir_time_ctrl		led_mode	0	0	0

Description
This register controls the global options of ASRG08.

Bit name	Reset value	Function
led_mode	0	LED turn off mode control bit. 0 : LEDs' remains ON state even if the IR input signal goes low 1 : LED's go OFF state if IR input signal goes low
ir_time_ctrl	01	IR input waiting time control bits when the IR input signal is high. 00 : 90mS 01 : 160mS 1x : 0mS
int_out_mode	0	Interrupt output mode selection. 0 : Pulse mode (Interrupt mode A) 1 : Level mode (Interrupt mode B)
ad2_ldo_sel	0	A2_LDO port function selection bit. 0 : Analog output port 2 1 : LDO on-off control output port

8.2.9 Global option control 4

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37h	**global_ctrl4**	-	-	sts_clr_en	response_ctrl			clk_off	sw_rst

Description
This register controls the global options of ASRG08.

Bit name	Reset value	Function
sw_rst	0	Software reset control bit. 0 : Not reset 1 : Reset
clk_off	0	System clock off control bit. 0 : Not clock off 1 : Clock off
response_ctrl	011	Numbers of continuous touch detections for touch decision. Response ctrl[2:0] + 1 (Maximum time : 7)
sts_clr_en	0	Clear the 'mtp_status' register (Address: 5DH) control bit. 0 : Not clear 1 : Clear

8.2.10 Global option control 5

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	**global_ctrl5**	cal_hold	sin_multi _mode	cal_hold_time				exp_op_ en	exp_op_ mode

Description

This register controls the global options of ASRG08.

Bit name	Reset value	Function
exp_op_mode	0	Output expiration time count mode selection bit. - 0 : Expiration time counter is reset when any touch output is not appeared. - 1 : Expiration time counter is reset when any output state is changed.
exp_op_en	0	Output expiration enable control bit. - 0 : Don't use output expiration - 1 : Use output expiration
cal_hold_ time	0101	Output expiration Time control. - cal_hold_time[3:0] x 4 (seconds)
sin_multi_ mode	1	Single/Multi output operation mode selection bit. - 0 : Single output mode - 1 : Multi output mode
cal_hold	0	Calibration hold of all channels control bit. - 0 : Calibration - 1 : Calibration hold

8.2.11 Sensitivity

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39h ~ 40h	**Sensitivity0 ~ sensitivity7**	-	-	sensitivity00 ~ sensitivity07					

Description

ASRG08 can control the sensitivities of all channels independently.

Bit name	Reset value	Function
sensitivity00 ~ sensitivity07	001001	Sensitivities of each channel. - Sensitivity of CSx channel: {(sensitivity0x[5:0] x 0.1) + 0.05} (%).

8.2.12 Calibration speed control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41h	cal_speed	bf_up		bf_down		bs_up		bs_down	

Description

Calibration speed of each operation mode can be controlled by this 'cal_speed' register.

Bit name	Reset value	Function
bs_down	10	Down calibration speed in BS mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : ref. count ← sen. count. (Most priority)
bs_up	10	Up calibration speed in BS mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
bf_down	11	Down calibration speed in BF mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
bf_up	11	Up calibration speed in BF mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow

8.2.13 2-color LED luminance control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h ~ 4Ah	**pwm0~pwm7**	2pwm0 ~ 2pwm7				1pwm0 ~ 1pwm7			

Description

1pwmx register data is valid on M1 high period and 2pwmx register data is valid on M2 high period.

Bit name	Reset value	Function
1pwmx	0000	The LED PWM control bits of Dx port during M1 high period. - 0000 : The minimum low duty - 1111 : The maximum low duty
2pwmx	0000	The LED PWM control bits of Dx port during M2 high period. - 0000 : The minimum low duty - 1111 : The maximum low duty

8.2.14 Analog output control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Bh ~ 52h	**Aout0 ~ Aout7**	-	ad_sel0 ~ ad_sel7		adout_data0 ~ adout_data7				

Description

Analog output channel and voltage level of each channel control register.

Bit name	Reset value	Function
adout_datax	11111	Analog output voltage level of each CSx channel. - [(adout_datax[4:0] +1)/32] x VDD (Volts)
ad_selx	00	Analog output port selection of CSx channel. - 00 : Analog output disable - 01 : Using A1_INT port - 10 : Using A2_LDO port - 11 : Using A3 port

8.2.15 Sense, reference count read register

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
53h	rd_ch_H1	rd_ch_H1							
54h	rd_ch_L1	-	-	-	-	-	-	-	rd_ch_L1
55h	sen_H	-	-	sen_count[13:8]					
56h	sen_L	sen_count[7:0]							
57h	ref_H	-	-	ref_count[13:8]					
58h	ref_L	ref_count[7:0]							
59h	rd_ch_H2	rd_ch_H2							
5Ah	rd_ch_L2	-	-	-	-	-	-	-	rd_ch_L2

Description

ASRG08 provides the special function to read sense count of each channels or reference count.

Bit name	Reset value	Function
rd_ch_H1	00000000	Read channel indication register. - 00000001 : Dummy channel - 00000010 : CS0 channel - 00000100 : CS1 channel - 00001000 : CS2 channel - 00010000 : CS3 channel - 00100000 : CS4 channel - 01000000 : CS5 channel - 10000000 : CS6 channel
rd_ch_L1	0	Read channel indication register. - 1 : CS7 channel
sen_count[13:8]	000000	Sense count data of most significant six bits. - Sense count [13:8]
sen_count[7:0]	00000000	Sense count data of least significant eight bits. - Sense count [7:0]
ref_count[13:8]	000000	Reference count data of most significant six bits. - Reference count [13:8]
ref_count[7:0]	00000000	Reference count data of least significant eight bits. - Reference count [7:0]
rd_ch_H2	00000000	Read channel confirm register. - 00000001 : Dummy channel - 00000010 : CS0 channel - 00000100 : CS1 channel - 00001000 : CS2 channel - 00010000 : CS3 channel - 00100000 : CS4 channel - 01000000 : CS5 channel - 10000000 : CS6 channel
rd_ch_L2	0	Read channel confirm register. - 1 : CS7 channel

8.2.16 OTP ROM cell select register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Bh	usr_mtp_sel	0	0	0	mtp_sel_en	org_usr_mtp_sel			

Description

The OTP ROM cells of ASRG08 are made up of eight memory cells of 64 bytes. ASRG08 provides the way to access OTP ROM cells with this register. User can select the OTP ROM cell with 'org_usr_mtp_sel' bits and if user doesn't want to select the OTP ROM cell directly, 'mtp_sel_en' bit leaves '0', then OTP ROM cell is selected the automatically.

Bit name	Reset value	Function
org_usr_mtp_sel	0000	OTP ROM cell selection bits. 0000, 0001 : 1st OTP ROM cell 0010 : 2nd OTP ROM cell 0011 : 3rd OTP ROM cell 0100 : 4th OTP ROM cell 0101 : 5th OTP ROM cell 0110 : 6th OTP ROM cell 0111 : 7th OTP ROM cell 1000 : 8th OTP ROM cell
mtp_sel_en	0	OTP ROM cell selection enable bit. 0 : Select OTP ROM cell automatically 1 : Select OTP ROM cell by user

8.2.17 OTP ROM control register (OTP ROM command)

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ch	mtp_cmd	0	0	write_all	read_all	0	0	wr_start	rd_start

Description

OTP ROM commands to access.

Bit name	Reset value	Function
rd_start	0	Reading selected OTP ROM cell start command bit. 0 : Don't start 1 : Start to read
wr_start	0	Writing on selected OTP ROM cell start command bit. 0 : Don't write 1 : Start to write
read_all	0	Unit of reading the selected OTP ROM cell control bit. 0 : 1-Byte reading 1 : All bytes of selected OTP ROM cell reading
write_all	0	Unit of writing on selected OTP ROM cell control bit. 0 : 1-Byte writing 1 : All bytes of selected OTP ROM cell writing

8.2.18 OTP ROM status register.

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Dh	mtp_status	-	org_mtp_sel				wr_done_sts	rd_done_sts	no_load_sts

Description

This register indicates the status of operation of selected one OTP ROM cell.

Bit name	Reset	Function
no_load_sts	-	This bit indicates whether some data are loaded from OTP ROM cells. 0 : There is some data loaded from OTP ROM cells 1 : No data loaded from OTP ROM cells
rd_done_sts	-	This bit indicates the end of reading. 0 : 1 : End of reading
wr_done_sts	-	This bit indicates the end of writing. 0 : 1 : End of writing
org_mtp_sel	-	These bits indicate that OTP ROM cell is loaded at initial time. 0000 : No loaded 0001 : 1st OTP ROM cell 0010 : 2nd OTP ROM cell 0011 : 3rd OTP ROM cell 0100 : 4th OTP ROM cell 0101 : 5th OTP ROM cell 0110 : 6th OTP ROM cell 0111 : 7th OTP ROM cell 1000 : 8th OTP ROM cell

8.2.19 OTP ROM data address select register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Eh	otp_add_sel	0	0	otp_add_sel					

Description

Register for the specific address of selected OTP ROM cell. User can access OTP ROM data of specific address by leaving ‘read_all’ and ‘write_all’ bits in the ‘mtp_cmd’ register ‘0’, selecting the OTP ROM cell with ‘usr_mtp_sel’ register and selecting the specific address with this register.

Bit name	Reset	Function
otp_add_sel	000000	Select specific address of selected OTP ROM cell. otp_add_sel[5:0] : Address

8.2.20 OTP ROM data register to write

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Fh	otp_wr_data	otp_wr_data							

Description

The data register to write on specific address of selected OTP ROM cell.

Bit name	Reset	Function
otp_wr_data	00000000	Data register to write. otp_wr_data[7:0] : Data

8.2.21 OTP data register to read

Type: R

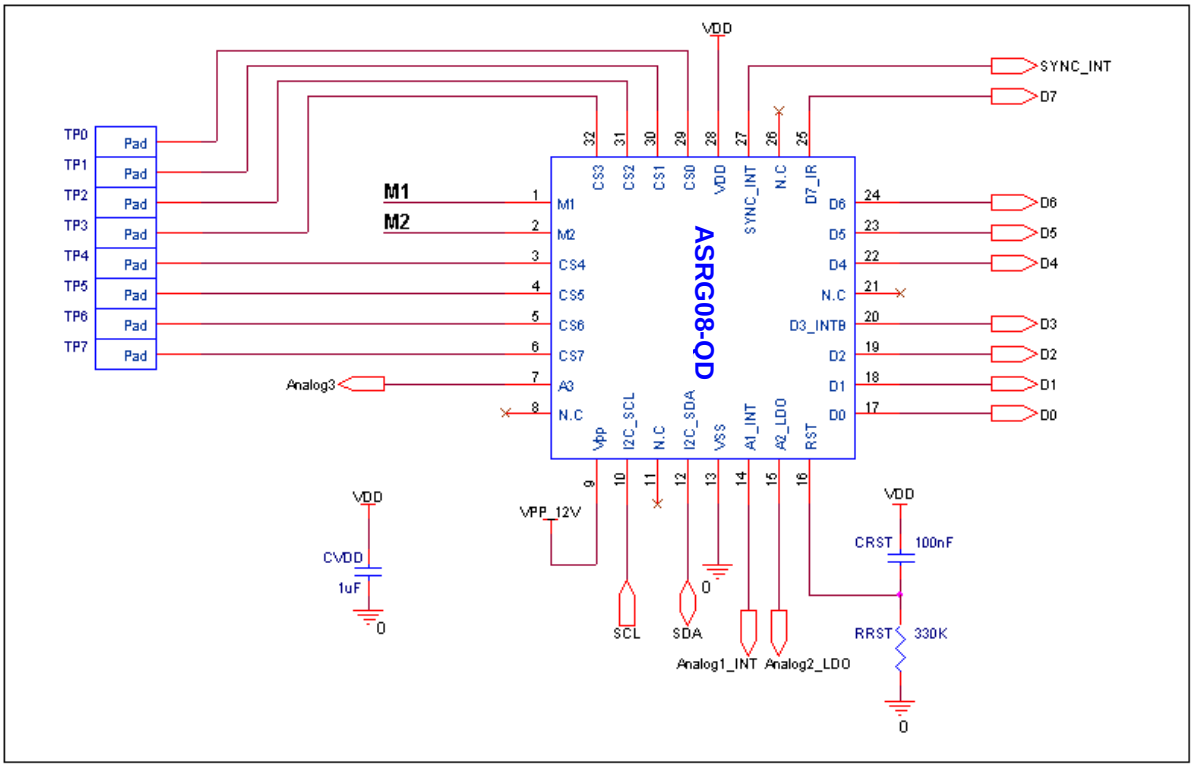
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60h	otp_rd_data	otp_rd_data							

Description

The data register for reading data from specific address of selected OTP ROM cell.

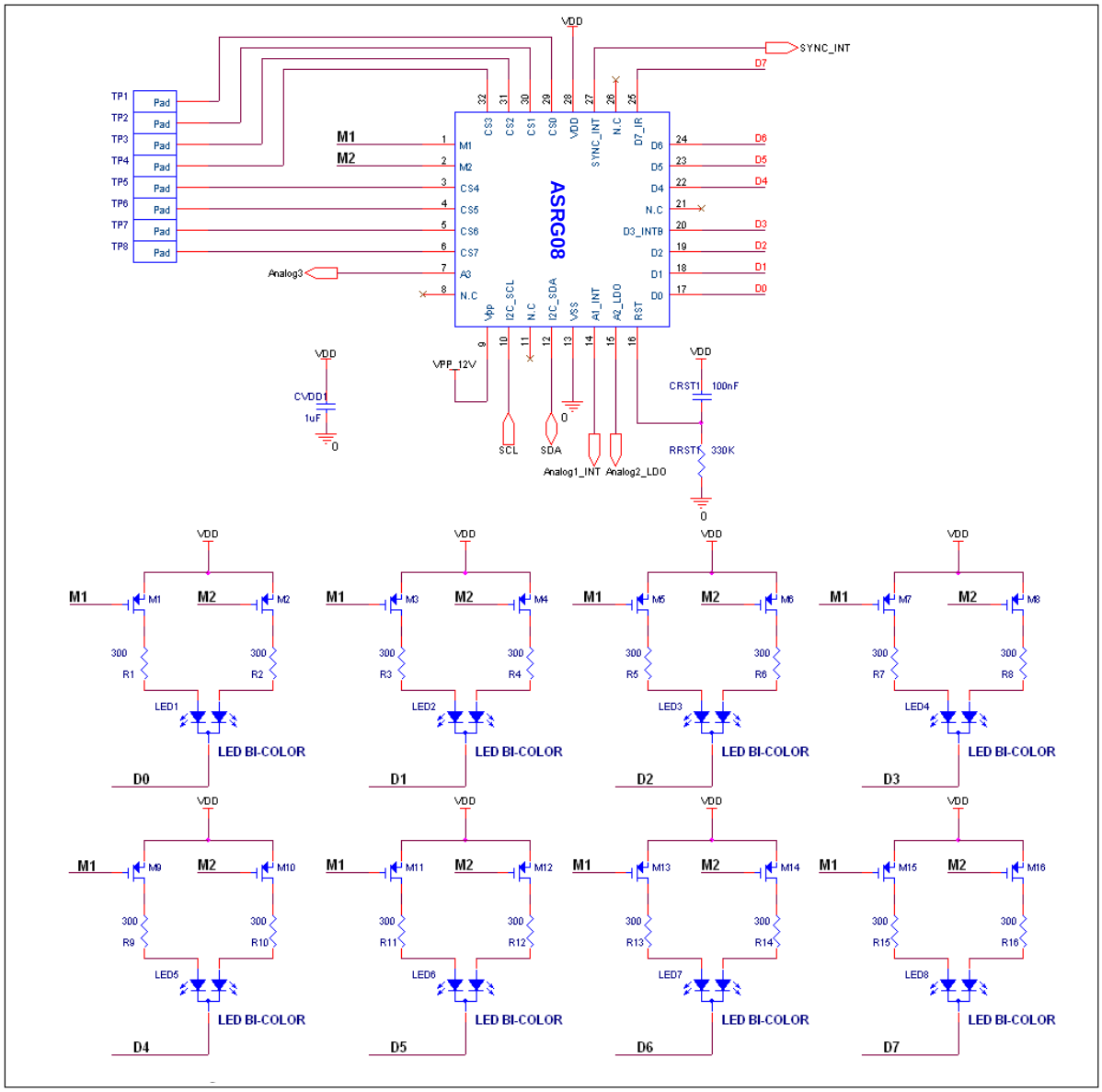
Bit name	Reset	Function
otp_rd_data	---- ----	Data register for reading OTP ROM data. otp_rd_data [7:0] : Data

9 Recommended Circuit Diagram



ASRG08-QD (32QFN) Application Example Circuit for parallel output

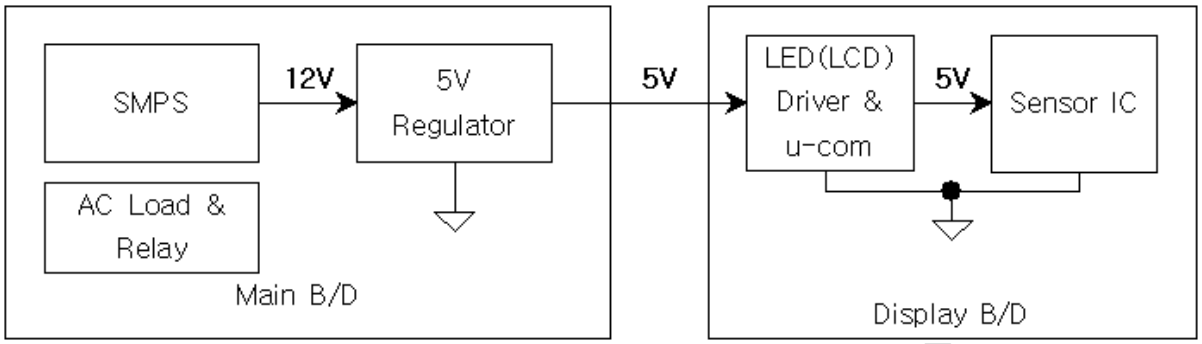
- ASRG08 is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from ASRG08.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The D0 ~ D7 are open drain output ports. Therefore, in the case of active high output or active low output, the pull-up or pull-down resistor should be needed as above figure.
- Unused CS pins may be connected to GND for stable operation.



ASRG08-QD (32QFN) Application Example Circuit for 2-color LED

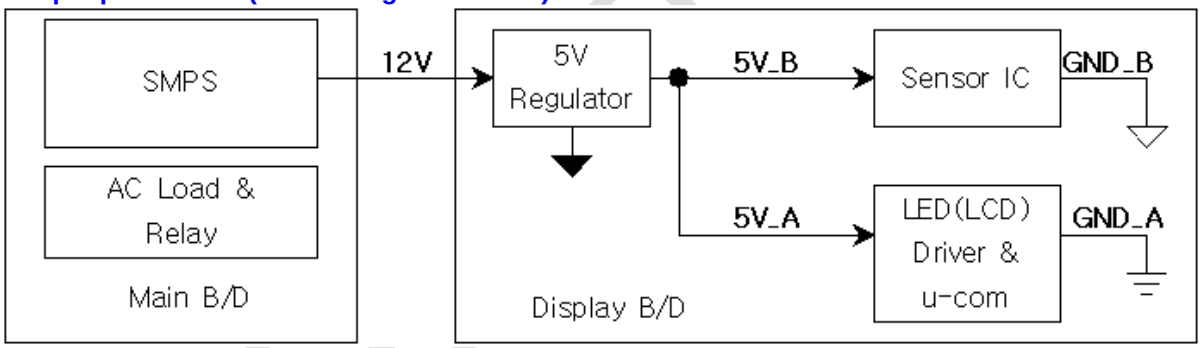
9.1 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

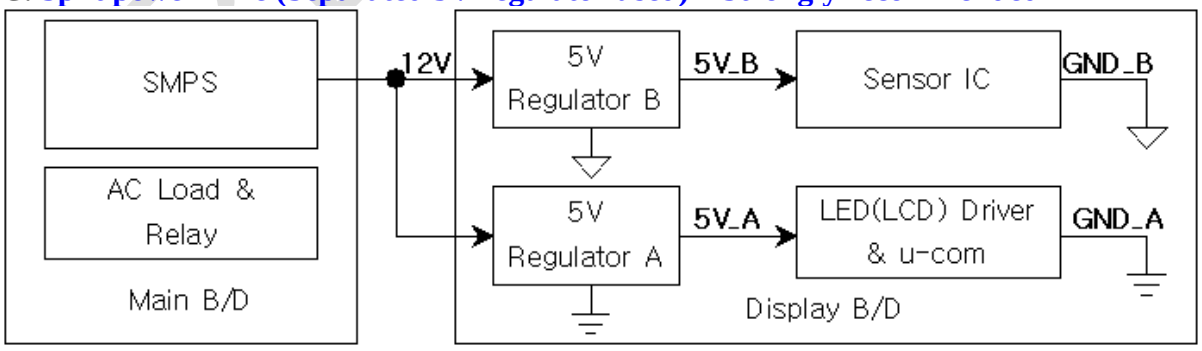


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power Line (One 5V regulator used) – Recommended

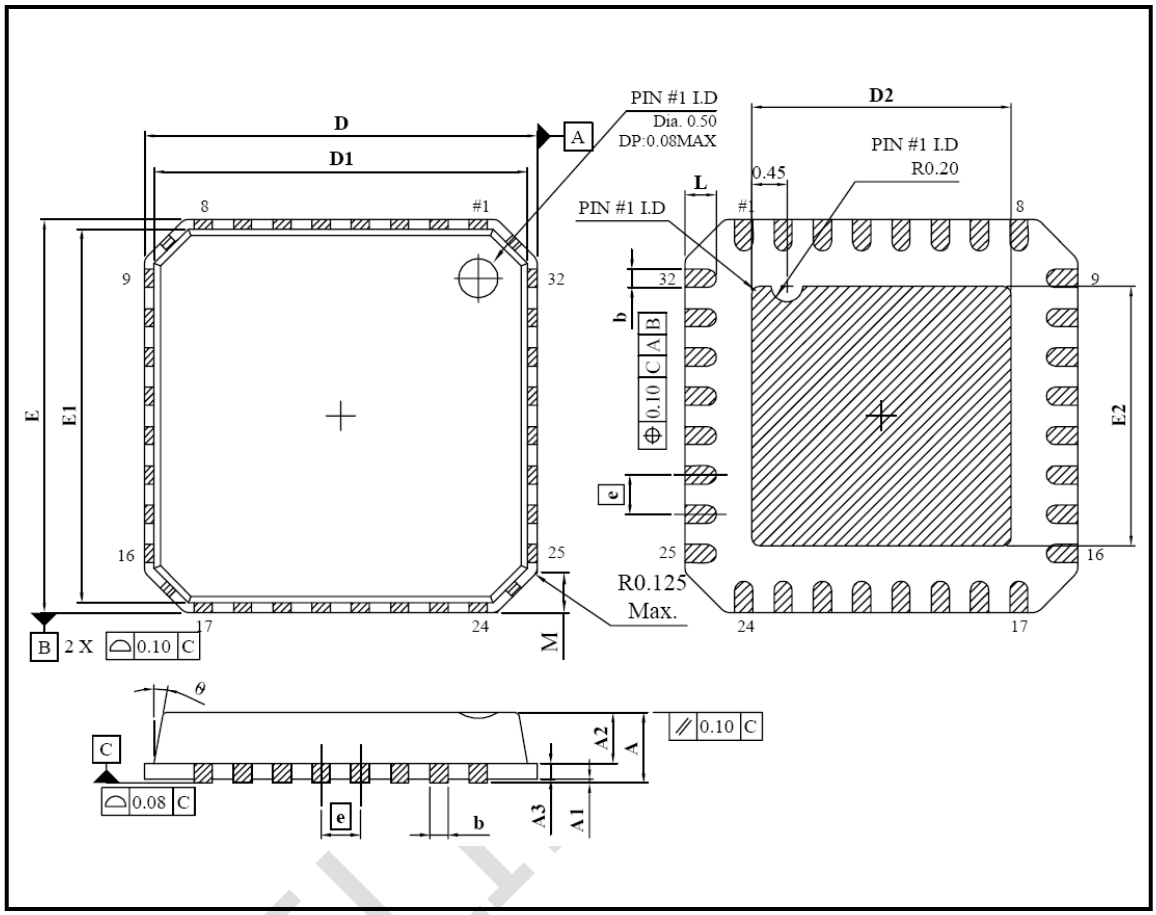


C. Split power Line (Separated 5V regulator used) – Strongly recommended



10 MECHANICAL DRAWING

10.1 Mechanical Drawing of ASRG08 (32 QFN Punched type)



DIM	MIN.	NOR.	MAX.	NOTES
A	-	0.85	0.90	
A1	0.00	0.01	0.05	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A2	-	0.65	0.70	
A3		0.20 REF.		2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
b	0.18	0.23	0.28	
D		5.00 BSC.		3.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
D1		4.75 BSC.		
D2	3.20	3.30	3.40	4.0 RADIUS ON TERMINAL IS OPTIONAL.
E		5.00 BSC.		
E1		4.75 BSC.		5.0 MATTE FINISH TOP - VDI 15~18 BOTTOM - POLISH
E2	3.20	3.30	3.40	
e		0.50 BSC.		
L	0.35	0.40	0.45	
M	0.45	0.50	0.55	
θ	9°	10°	11°	

11 MARKING DESCRIPTION

Device Code : **ASRG 0 8 QX**

- **Type of package (QD: 32QFN, QC: 28QFN)**
- **Channel Number**
- **Touch Switch Group**

Weekly Code : **YY WW**

- **Manufacturing Week**
- **Manufacturing Year**

NOTES:

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