CD40109B Types

CMOS Quad Low-to-High Voltage Level Shifter

High-Voltage Types (20-Volt Rating)

■ CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}.

The CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between V_{SS} and at least 0.7 V_{CC}; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC} and V_{DD}. When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

The CD40109B-Series types are supplied in 16-lead ceramic dual-in-line packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

■ High-or-low level-shifting with three-state outputs for unidirectional or bidirectional bussing
■ Isolation of logic subsystems using separate power supplies from supply sequencing, supply loss and supply regulation considerations

Features:

■ Independence of power supply sequence considerations—V_{CC} can exceed V_{DD}, input signals can exceed both V_{CC} and V_{DD}
■ Up and down level-shifting capability
■ Three-state outputs with separate enable controls
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range)
= 1 V at V_{CC} = 5 V, V_{DD} = 10 V
= 2 V at V_{CC} = 10 V, V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

FUNCTIONAL DIAGRAM
(1 of 4 units)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute–Maximum Values:*

DC SUPPLY–VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V
OUTPUT VOLTAGE RANGE, ALL OUTPUTS .... −0.5 V to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE–TEMPERATURE RANGE (All Package Types).............. 100mW
OPERATING–TEMPERATURE RANGE (T_A) .... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

TRUTH TABLE

INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

LOGIC 0 = LOW(V_{SS})   X = DON'T CARE   Z = HIGH IMPEDANCE
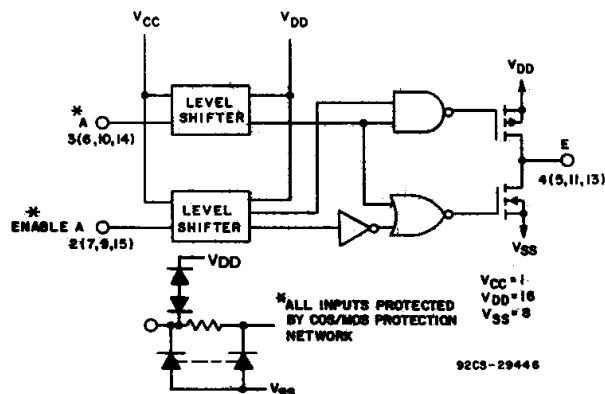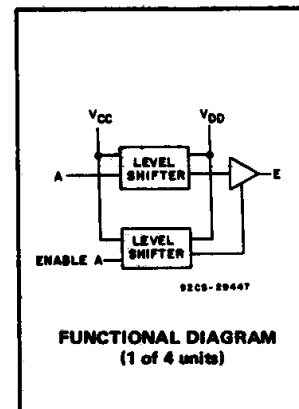LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS

Fig. 1 — CD40109B logic diagram (1 of 4 units).

COMMERCIAL CMOS HIGH VOLTAGE ICs
3

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				+25			UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1	–	
	2.5	0,5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2	–	
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	
	13.5	0,15	15	–4.2	–4	–2.8	–2.4	–3.4	–6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA
3-State Output Leakage Current I_{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	µA
	V_O (V)	V_{CC} (V)	V_{DD} (V)								
Input Low Voltage, V_{IL} Max.	1,9	5	10	1.5				–	–	1.5	V
	1.5, 13.5	10	15	3				–	–	3	
Input High Voltage, V_{IH} Min.	1,9	5	10	3.5				3.5	–	–	
	1.5,13.5	10	15	7				7	–	–	
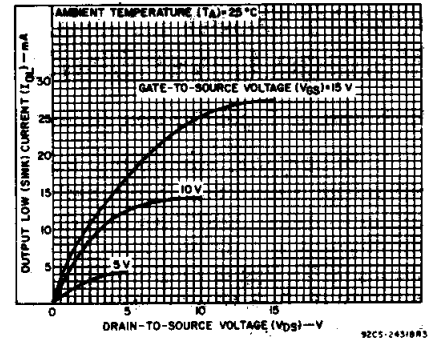
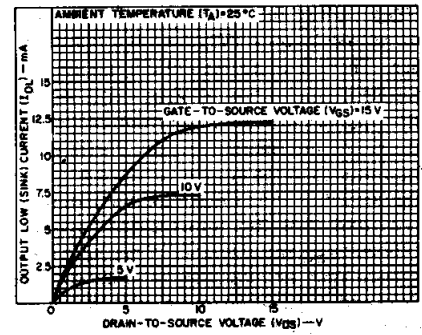Fig.2 – Typical output low (sink) current characteristics.

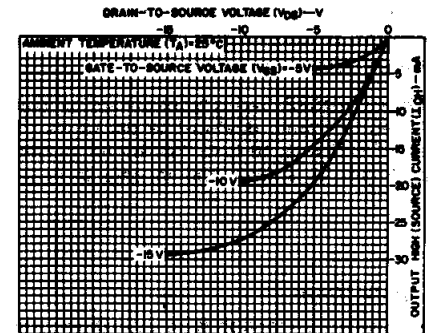Fig.3 – Minimum output low (sink) current characteristics.
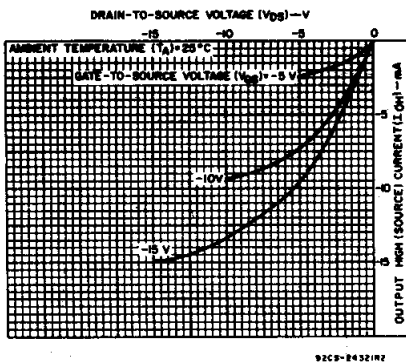

Fig.4 – Typical output high (source).

Fig.5 – Minimum output high (source) current characteristics.
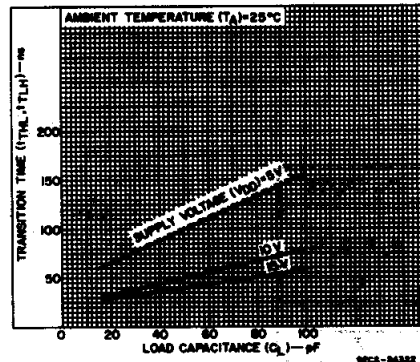

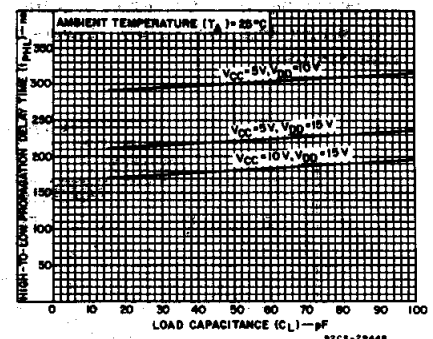Fig.6 – Typical transition time as a function of load capacitance.

Fig.7 – Typical high-to-low propagation delay time as a function of load capacitance.

CD40109B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ unless otherwise specified

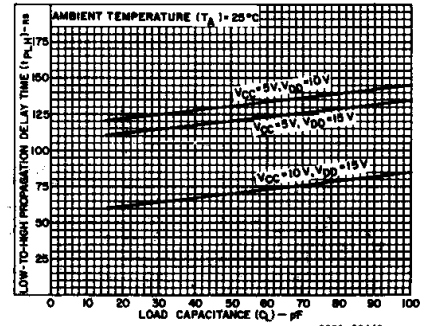| CHARACTERISTIC	SHIFTING MODE	V_{CC} (V)	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay — Data Input to Output:	L-H	5	10	300	600	
		5	15	220	440	
High-to-Low Level, t_{PHL}		10	15	180	360	
	H-L	10	5	250	500	ns
		15	5	250	500	
		15	10	120	240	
	L-H	5	10	130	260	
		5	15	120	240	
Low-to-High Level, t_{PLH}		10	15	70	140	ns
	H-L	10	5	230	460	
		15	5	230	460	
		15	10	80	160	
3-State Disable Delay: R_L = 1 kΩ	L-H	5	10	60	120	
		5	15	75	150	
Output High to High Impedance, t_{PHZ}		10	15	35	70	ns
	H-L	10	5	200	400	
		15	5	200	400	
		15	10	40	80	
	L-H	5	10	370	740	
Output Low to High Impedance, t_{PLZ}		5	15	300	600	
		10	15	250	500	ns
	H-L	10	5	250	500	
		15	5	250	500	
		15	10	130	260	
	L-H	5	10	320	640	
High Impedance to Output High, t_{PZH}		5	15	230	460	
		10	15	180	360	ns
	H-L	10	5	300	600	
		15	5	300	600	
		15	10	130	260	
	L-H	5	10	100	200	
High Impedance to Output Low, t_{PZL}		5	15	80	160	
		10	15	40	80	ns
	H-L	10	5	200	400	
		15	5	200	400	
		15	10	40	80	
	L-H	5	10	50	100	
		5	15	40	80	
Transition Time, t_{THL}, t_{TLH}		10	15	40	80	ns
	H-L	10	5	100	200	
		15	5	100	200	
		15	10	50	100	
Input Capacitance, C_I		Any Input		5	7.5	pF

Fig.8 — Typical low-to-high propagation delay time as a function of load capacitance.
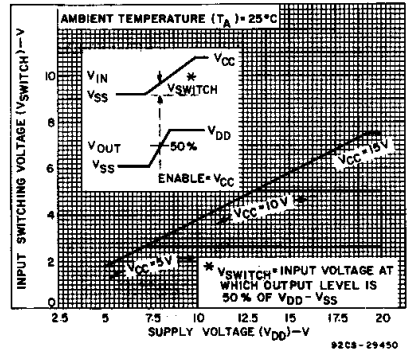

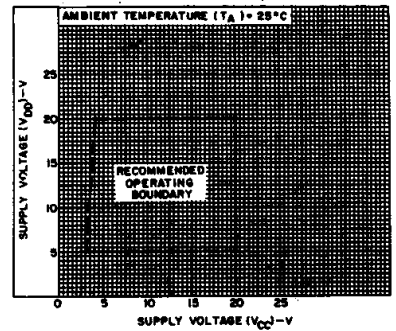Fig.9 — Typical input switching as a function of high-level supply voltage.

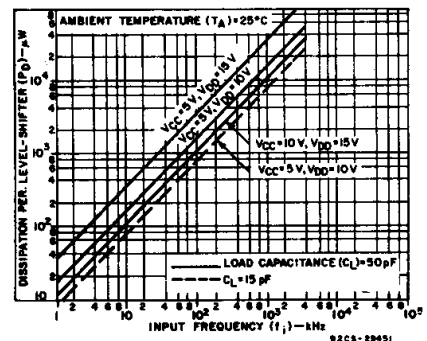Fig.10 — High-level supply voltage vs. low-level supply voltage.

Fig.11 — Typical dynamic power dissipation as a function of input frequency.

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

TEST CIRCUITS

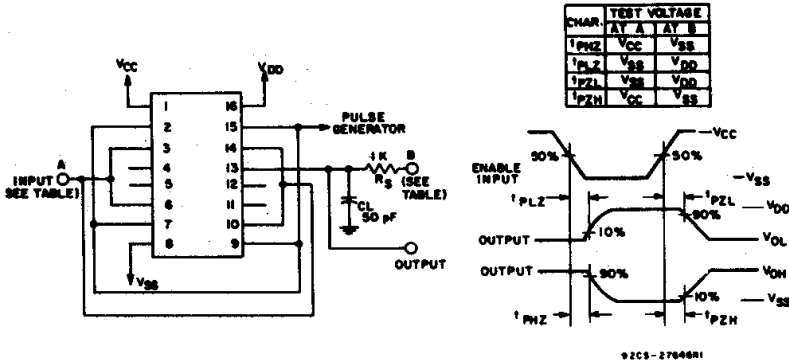| CHAR.	TEST VOLTAGE AT A	TEST VOLTAGE AT B
t_{PHZ}	V_{CC}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{CC}	V_{SS}

Fig. 12 — Output enable delay times test circuit and waveforms.
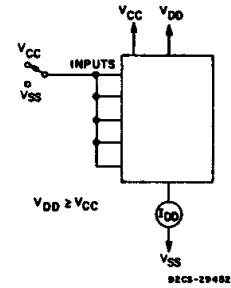
Fig. 13 — Quiescent device current.

Fig. 14 — Input voltage.

NOTE:
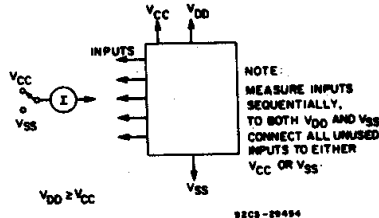TEST ANY COMBINATION OF INPUTS

Fig. 15 — input current.

NOTE:
MEASURE INPUTS SEQUENTIALLY.
TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{CC} OR V_{SS}.
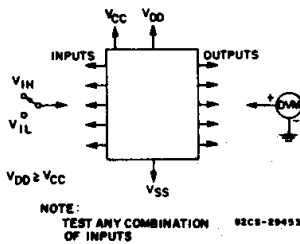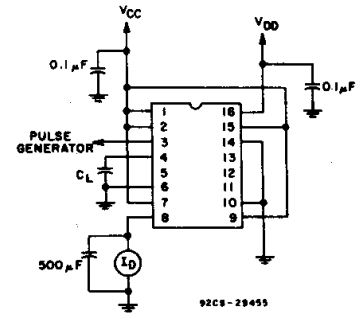
Fig. 16 — Dynamic power dissipation test circuit.

V_{CC}	1	16	V_{DD}
ENABLE A	2	15	ENABLE D
A	3	14	D
E	4	13	H
F	5	12	NC
B	6	11	G
ENABLE B	7	10	C
V_{SS}	8	9	ENABLE C

TOP VIEW

92CS-29456
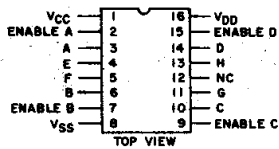
CD40109B
TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

71-79
(1.803-2.007)

4-10
(0.102-0.254)

97-105
(2.464-2.667)

92CS-36897
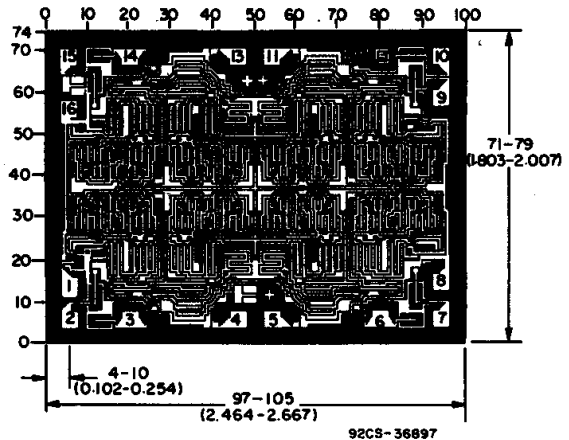
Dimensions and pad layout for CD40109BH.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40109BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40109BE	Samples
CD40109BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40109BF	Samples
CD40109BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40109BF3A	Samples
CD40109BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40109B	Samples
CD40109BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40109B	Samples
CD40109BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40109B, CD40109B-MIL :

● Catalog: CD40109B

● Automotive: CD40109B-Q1, CD40109B-Q1

● Military: CD40109B-MIL

NOTE: Qualified Version Definitions:

   ● Catalog - TI's standard catalog product

   ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

   ● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40109BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40109BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

2X
4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

⊕ 0.1Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

TEXAS
INSTRUMENTS
www.ti.com

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

1   7

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
⚠C MS−001 VARIATION	AA	BB	AC	AD

A

16   9

$\frac{0.260}{0.240}$ (6,60) / (6,10)

1   8

$\frac{0.070 \ (1,78)}{0.045 \ (1,14)}$ ⚠D

$\frac{0.045 \ (1,14)}{0.030 \ (0,76)}$ ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$\frac{0.021 \ (0,53)}{0.015 \ (0,38)}$

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

$\frac{0.325 \ (8,26)}{0.300 \ (7,62)}$

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         ⚠C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         ⚠D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com