

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM TMM2015BP-90, TMM2015BP-12
 SILICON MONOLITHIC
 N-CHANNEL SILICON GATE MOS PROCESS TMM2015BP-10, TMM2015BP-15

DESCRIPTION

The TMM2015BP is a 16, 384 bits high speed and low power static random access memory organized as 2, 048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When \overline{CS} is a logical high, the device

is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2015BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability

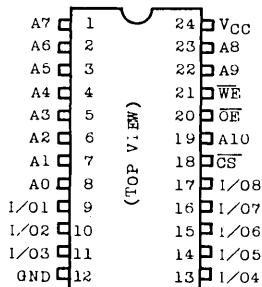
FEATURES

- Access Time and Current

Part Number	Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015BP-90		90ns	50mA	5mA
TMM2015BP-10		100ns	50mA	5mA
TMM2015BP-12		120ns	50mA	5mA
TMM2015BP-15		150ns	50mA	5mA

- High Density Assembly Capability
 0.3 inch width package (24pin plastic DIP)

PIN CONNECTION

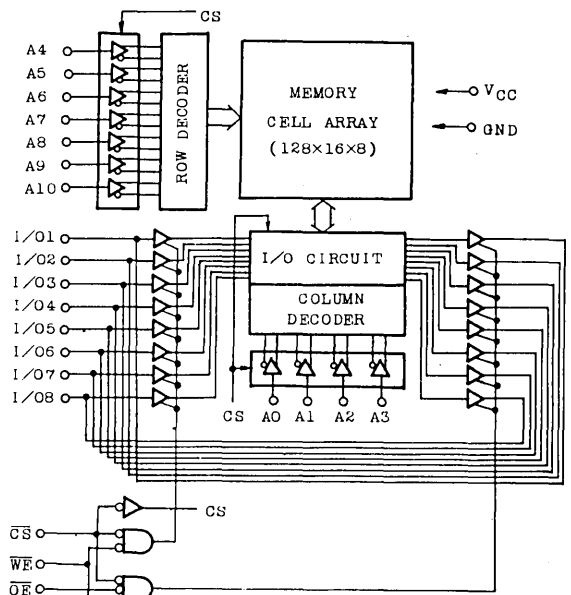


PIN NAMES

A ₀ ~A ₃	Column Address Inputs
A ₄ ~A ₁₀	Row Address Inputs
\overline{CS}	Chip Select Input
\overline{WE}	Write Enable Input
I/O ₁ ~I/O ₈	Data Input/Output
\overline{OE}	Output Enable Input
V _{CC}	Power (5V)
GND	Ground

- Single 5V power Supply
- Fully Static Operation
- Power Down Feature: \overline{CS}
- Output Buffer Control: \overline{OE}
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

BLOCK DIAGRAM



TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	Power Supply Voltage	-0.5~7.0	V
V _{IN} , V _{OUT}	Input/Output Voltage	-0.5*~7.0	V
T _{OPR}	Operating Temperature	0~70	°C
T _{STG}	Storage Temperature	-55~150	°C
T _{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P _D	Power Dissipation(T _a =70°C)	0.7	W

* -3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.0	—	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.5**	—	0.8	V
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V

** -3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} =0V~5.5V	-10	—	10	μA
V _{OH}	Output High Voltage	I _{OUT} =-1.0mA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OUT} =4.0mA	—	—	0.4	V
I _{LO}	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, V _{OUT} =0V~5.5V	-10	—	10	μA
I _{SBP}	Peak Power-on Current	$\overline{CS}=V_{CC}$, I _{OUT} =0mA	—	—	10	mA
I _{SB}	Standby Current	$\overline{CS}=V_{IH}$, I _{OUT} =0mA	—	—	5	mA
I _{CC}	Operating Current	$\overline{CS}=V_{IL}$, I _{OUT} =0mA	—	—	50	mA

CAPACITANCE*** (T_a=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} =0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

TMM2015AP-90, TMM2015AP-12 TMM2015AP-10, TMM2015AP-15

A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t _{ACC}	Address Access Time	—	90	—	100	—	120	—	150	
t _{CO}	Chip Select Access Time	—	90	—	100	—	120	—	150	
t _{OE}	Output Enable Time	—	35	—	35	—	50	—	55	
t _{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t _{CLZ}	\overline{CS} to Output in Low-Z	15	—	15	—	15	—	15	—	
t _{CHZ}	\overline{CS} to Output in High-Z	—	40	—	40	—	40	—	55	
t _{OLZ}	\overline{OE} to Output in Low-Z	5	—	5	—	5	—	5	—	
t _{OHZ}	\overline{OE} to Output in High-Z	—	35	—	35	—	35	—	50	
t _{PU}	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t _{PD}	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

Write Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t _{EW}	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t _{AS}	Address Set Up Time	20	—	20	—	20	—	20	—	
t _{WP}	Write Pulse Width	55	—	65	—	80	—	100	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t _{DS}	Data Set Up Time	30	—	35	—	45	—	50	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t _{WLZ}	\overline{WE} to Output in Low-Z	5	—	5	—	5	—	5	—	
t _{WHZ}	\overline{WE} to Output in High-Z	—	25	—	30	—	35	—	50	

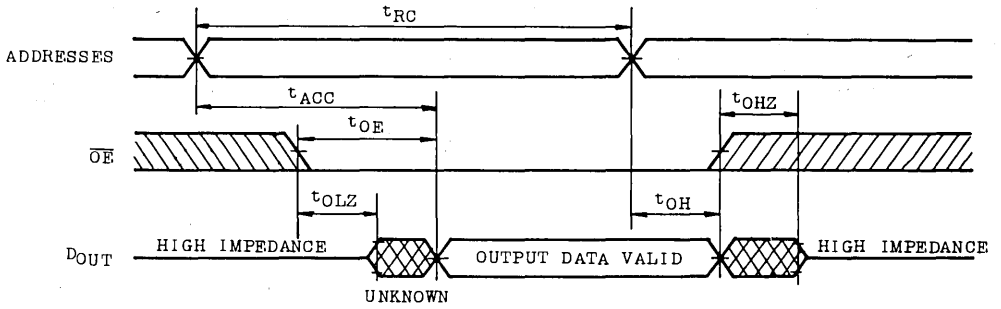
A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C _L =100pF

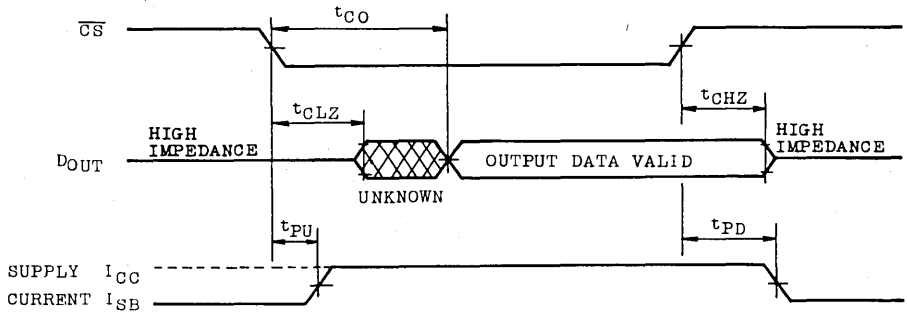
TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

TIMING WAVEFORMS

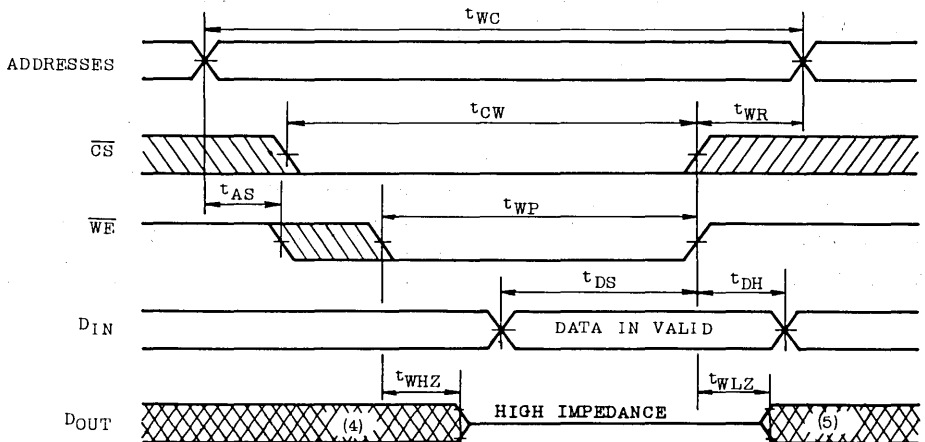
• (A) READ CYCLE (1) (1)



• (B) READ CYCLE (2) (1), (2)

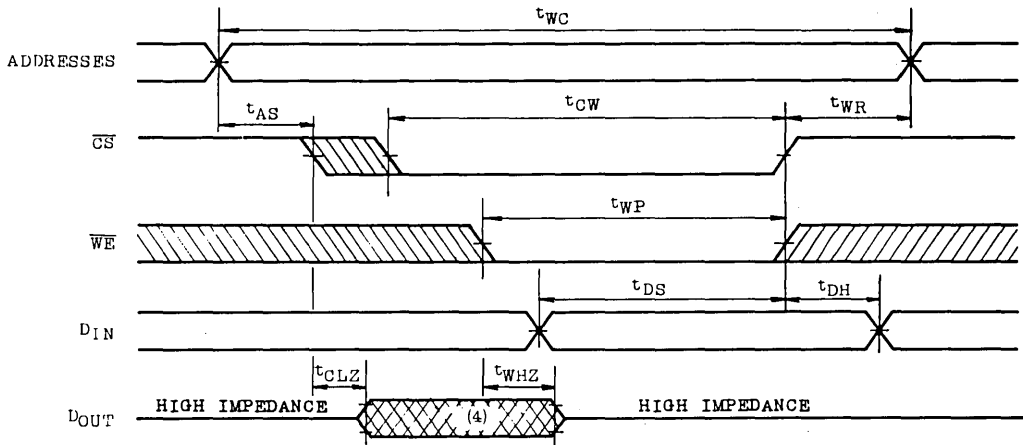


• (C) WRITE CYCLE (1) (3)



TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

• (D) WRITE CYCLE (2) (3)



NOTES:

- (1) The \overline{WE} is high for read cycle.
Device is continuously selected, $\overline{CS} = V_{IL}$ in read cycle (1)
- (2) All addresses are valid prior to or simultaneously with \overline{CS} transitions.
- (3) A write occurs during the overlap of low CS and low WE.
The t_{cw} is specified as the time from the chip selection to end of write in write cycle, and the t_{wp} is specified as the overlap time of low CS and low WE.
 \overline{OE} is allowed to be low or high level in write cycle.
If the \overline{OE} is high, the output buffers remain in a high impedance state in this period.
- (4) If the \overline{CS} low transition occurs simultaneously with or latter to the \overline{WE} low transition, the output buffers remain in a high impedance state in this period.
- (5) If the \overline{CS} high transition occurs simultaneously with \overline{WE} high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) $t_{CLZ}, t_{OLZ}, t_{WLZ}$ Output Enable Time

(B) $t_{CHZ}, t_{OHZ}, t_{WHZ}$ Output Disable Time

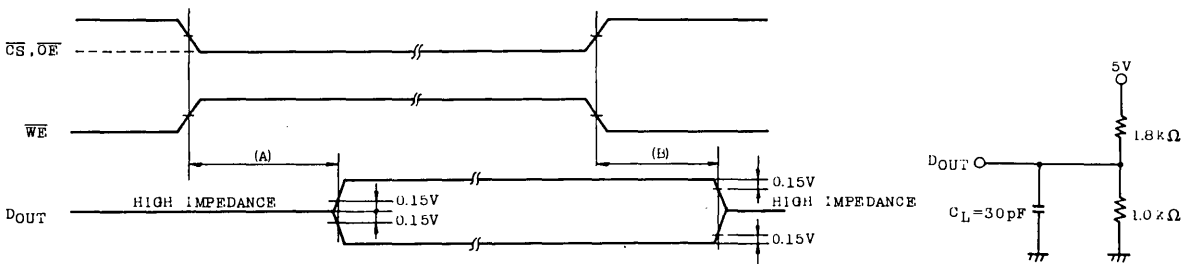
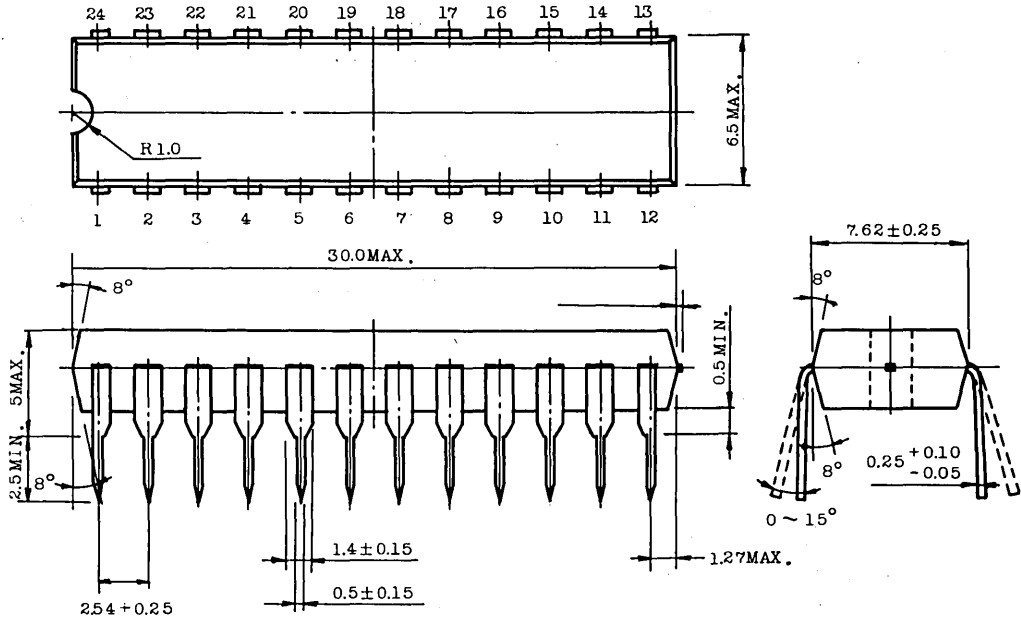


Fig. 1 Output load condition for enable disable time measurement.

TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

©Aug., 1985 Toshiba Corporation