

## Data Sheet

# BIT3107

## High Efficiency ZVS CCFL Controller

Version : 1.0

*Notice*

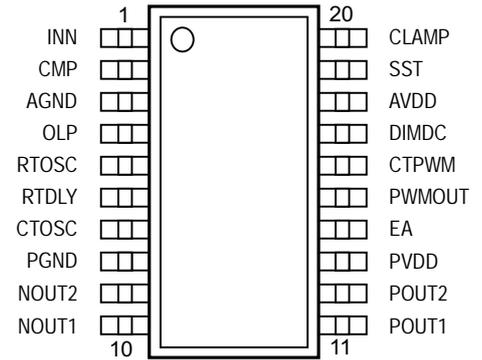
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**Features:**

- 2.7V ~ 5.5V Operation Voltage
- Full Bridge Fixed Frequency or Resonance ZVS Control
- 85 % High Efficiency
- Built-in PWM Dimming
- Programmable Striking Voltage
- Latched Open Lamp Protection
- ON/OFF Control with zero Standby Current
- Rail-to-Rail Totem Pole Output
- Low Power CMOS Process
- Winding/Piezoelectric Transformer driving Algorithm

**Pin Layout:**



**Applications:**

- Cold Cathode Fluorescent Lamps system
- Personal Digital Assistants
- Digital Camera
- Tablet PC
- Navigation Devices (GPS Equipment)
- Notebook Computer
- LCD Monitor
- Video Phone/ Door Phone

**Recommended Operating Condition:**

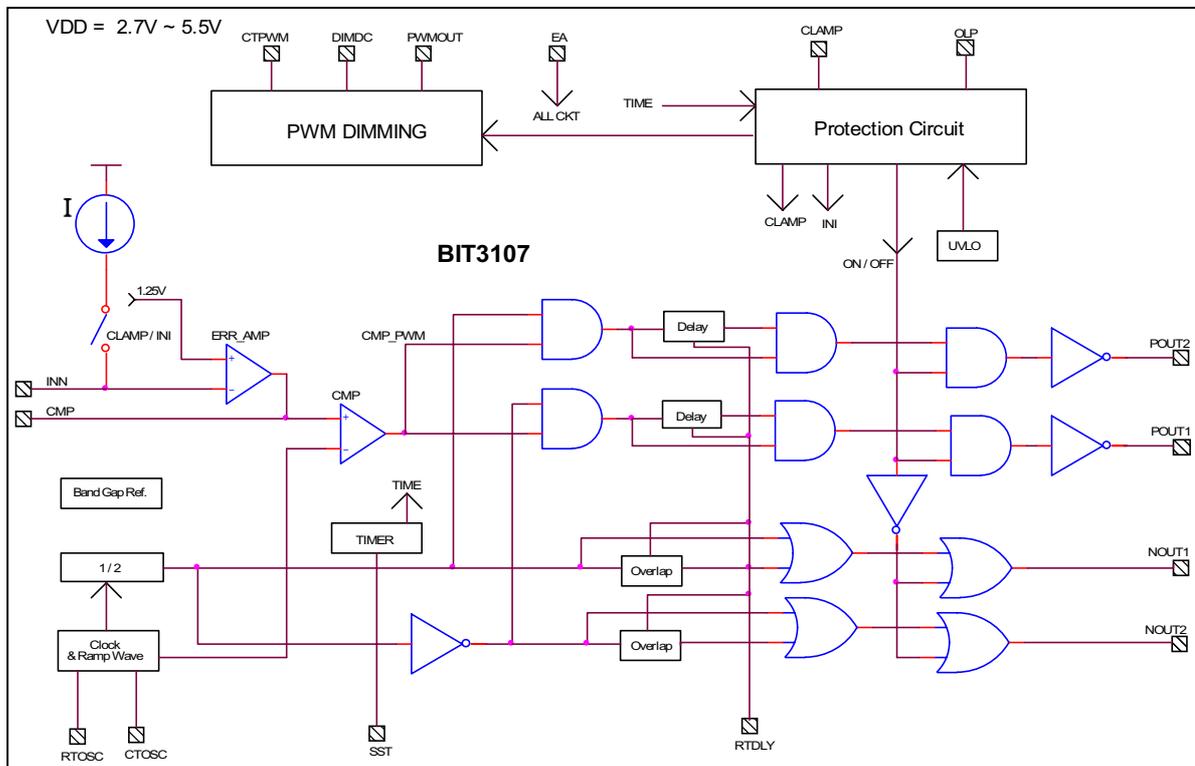
Supply Voltage.....2.7 ~ 5.5 V  
 Operating Ambient Temperature.....0 ~ 70 °C  
 Operating Frequency.....50K ~ 400K Hz

**General Description:**

BIT3107 integrated circuit provides the essential features for CCFL control in a small 20-pin SSOP package. New developed full bridge ZVS configuration provides a symmetry AC output and more than 85% efficiency to make it especially suitable for LCD backlight applications. BIT3107 senses the lamp current directly to enable the built-in PWM dimming. If no current flow into the lamp, BIT3107 provides a continuous AC output to ensure the successful ignition. PWM dimming is started immediately while the lamp is ignited. BIT3107 includes a clamped striking voltage control loop to protect the transformer while ignition and the lamp current monitor provides the most reliable latched open lamp protection.

Patent pending.

**Functional Block Diagram:**



**Functional Description:**

**UVLO:** The under-voltage-lookout circuit turns the output driver off when supply voltage drops too low. System is shut down with all outputs turned to logic high level.

**Band Gap Reference:** An internal trimmed band-gap reference provides a high accuracy, supply and temperature insensitive voltage reference. By amplifying or dividing this voltage can generate the other required references.

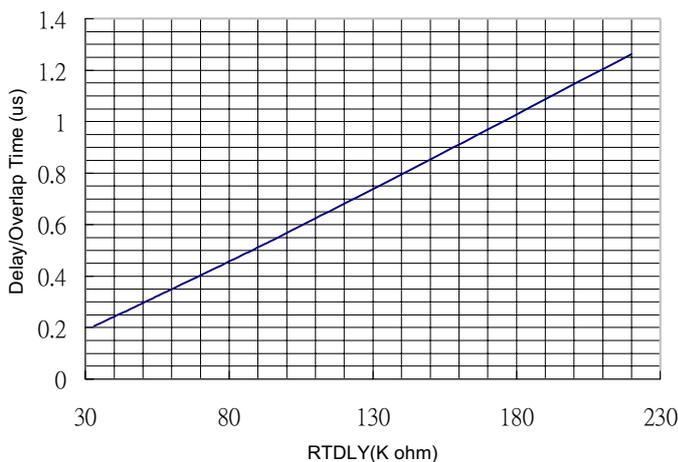
**Over Voltage Clamping:** while a > 1.5V is sensed by CLAMP pin, an internal ~ 80uA current will flow into the pin INN, the inverting input of the error amplifier, to reduce the output.

**On/Off Function:** The EA pin provides the function to turn on and off the output without shut down the supply voltage. An internal 80K ohm pulled low resistor is connected here. All of the outputs are forced to logic high when the chip is turned off.

**Set the Delay/Overlap Time for ZVS Operation:** The period of the internal delay generation circuitry dependent on the resistance of  $R_{RTDLY}$ . The CCFL control requires timing circuitry, the required period of ignition, PWM dimming PWM frequency and the delay/overlap for ZVS switching. The resistor  $R_{RTDLY}$  connected to pin RTDLY and the internal 1.25V determines a reference current  $I_{REF1}$  with

The Delay/Overlap time  $T_{Delay}$  and  $T_{Overlap}$  in typical case; 5V, 25°C operation, can be found from bellow:

RTDLY vs. Delay/Overlap Time



**Set the Lamp Operation Frequency:** Another resistor  $R_{RTOSC}$  connected to pin RTOSC determines the reference current  $I_{REF2}$  as equation (2)

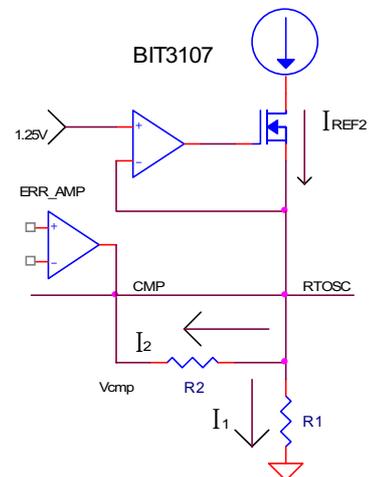
$$I_{REF2} = \frac{1.25V}{R_{RTOSC}} \dots\dots\dots(2)$$

The lamp frequency is:

$$F_{LAMP} = \frac{1.6 \times I_{REF2}}{C_{CTOSC}} \dots\dots\dots(3)$$

For a 55KHz operation CCFL if a 100K ohm resistor is used as the  $R_{RTOSC}$  resistor. A 350pF capacitor is required to connect to pin CTOSC.

**Voltage Controlled Lamp Frequency:** BIT3107 provides the variable lamp frequency control scheme for resonance application. The bellowing diagram shows an example of such operation:



The reference current  $I_{REF2}$ , which determines the lamp frequency, can be controlled as:

$$I_{REF2} = \frac{1.25V - V_{cmp}}{R2} + \frac{1.25V}{R1} \dots\dots\dots(4)$$

The lamp frequency is then varied with the output of the error amplifier.

**The Power On Initialization and Open Lamp Protection:**

A current mirror provides current with value  $\sim 0.05 \times I_{REF1}$  to charge the SST pin. The slope of  $\Delta V/\Delta T$  can be determined by

$$\frac{\Delta V}{\Delta T} = \frac{0.0625}{R_{RTDLY} \times C_{SST}} \dots\dots\dots(5)$$

A  $\sim 180\mu A$  current flow in to the inverting input of the error amplifier to force the output of PWM controller to be zero as the initial condition while the voltage of pin SST < 0.5V. Open lamp protection is triggered while pin SST > 1.5V. The ignition operates while the voltage of SST located between 0.5V and 1.5V, and it

can be calculated as equation (6)

$$T_{\text{STRIKE}} = 16 \times R_{\text{RTDLY}} \times C_{\text{SST}} \dots\dots\dots(6)$$

In the case of  $R_{\text{RTDLY}} = 82\text{K ohm}$ .

A 1.0 uF capacitor connected on the pin SST can set an ~ 1 Sec period for striking the lamp. If the voltage of OLP pin less than 300mV after this period, the latched protection function will latch the output drivers to PVDD high level. The latched situation can be released while the system is re-started.

**PWM Dimming:** To compare the input of pin DIMDC and the 0.5V ~ 1.5V ramp wave makes the PWM pulses for PWM dimming. The ramp wave generator generates

a ramp wave with peak =1.5V and valley =0.5V. Its frequency can be set as equation (7)

$$F_{\text{PWM}} = \frac{0.625}{R_{\text{RTDLY}} \times C_{\text{SST}}} \dots\dots\dots(7)$$

The output of pin PWMOUT is pulled to VDD to make the dark portion of the CCFL output bursts and the floating state to make the bright portion. A less than 0.5V input on pin DIMDC will make the PWMOUT to be floating to obtain 100% brightness. BIT3107 provides the continuous high voltage to strike the lamp. It sends the PWM pulses and turns off the controller while the voltage of OLP pin > 300mV.

**Pin Description:**

Pin	Names	I/O	Description
1	INN	I	The inverting input of the error amplifier.
2	CMP	O	Output of the error amplifier.
3	AGND	I/O	The ground pin of analog control circuitry.
4	OLP	I	Lamp current detection pin, the open lamp situation is detected if a less than 300mV input is sensed.
5	RTOSC	I/O	An external resistor connected here makes a reference current which determines the clock timing of the output drivers.
6	RTDLY	I/O	An external resistor connected here makes a reference current which determines the delay and overlap timing of the output drivers. With this reference current and different capacitors can set the period of ignition, the frequency of PWM dimming.
7	CTOSC	I/O	With the RTOSC pin made reference current and an external capacitor connected here can set the lamp operation frequency.
8	PGND	I/O	The ground pin of the output drivers.
9	NOUT2	O	The number 2 output driver of driving the NMOSFET switch.
10	NOUT1	O	The number 1 output driver of driving the NMOSFET switch.
11	POUT1	O	The number 1 output driver of driving the PMOSFET switch.
12	POUT2	O	The number 2 output driver of driving the PMOSFET switch.
13	PVDD	I	The power supplies input of output drivers.
14	EA	I	ON/OFF control pin, 1.2V threshold with an internal 80K ± 15% ohm pull low resistor.
15	PWMOUT	O	The output of PWM dimming. An ~ 200ohm pull to AVDD switch can be used to turn off the lamp with low frequency.
16	CTPWM	I/O	With the RTDLY pin made reference current and an external capacitor connected here can set the PWM dimming operation frequency and a 0.5V ~ 1.5V triangle wave output is generated for PWM input
17	DIMDC	I	PWM dimming control input. A PWM output comes out by comparing this DC input and the triangle wave that is generated by CTPWM.
18	AVDD	I	The power supply of analog voltage control circuitry.
19	SST	O	With the RTDLY pin made reference current and an external capacitor connected here can set the required period of ignition and the timing of initialization. The controller is forced to reset mode while SST <0.5V. During reset mode, a ~ 180uA current will flow into the INN pin to disable the output of the error amplifier CMP to turn off the controller. The open lamp protection function will be enabled after this node is charged to > 1.5V.
20	CLAMP	I	Over voltage clamping. If a > 1.5 V voltage is detected. A ~ 80uA current will flow into the INN pin to reduce the output of the error amplifier CMP to clamp the output voltage.

**Absolute Ratings:** (if  $T_a=25^{\circ}\text{C}$ )

Parameter	Symbol	Ratings	Unit	Remarks
Control Supply Voltage	AVDD	-0.3~+ 8	V	Ta=25°C
Analog Ground	AGND	±0.3	V	
Driver Supply Voltage	PVDD	-0.3~+ 8	V	
Driver Ground	PGND	±0.3	V	
Input Voltage		-0.3~ VDD+0.3	V	
Power Dissipation		800	mW	
Operating Ambient Temperature	Ta	0~ +70	°C	
Operating Junction Temperature		+150	°C	
Storage Temperature		-55~+150	°C	

**DC/AC Characteristics:**

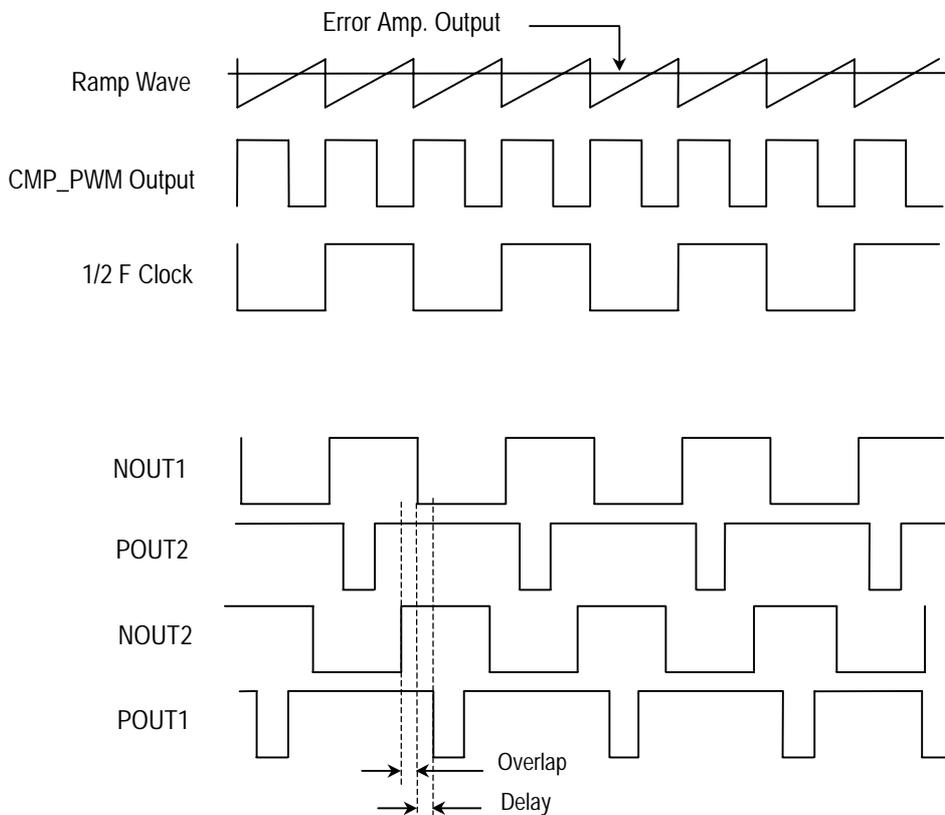
Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Supply Voltages</b>					
AVDD (note1)		2.7		5.5	V
PVDD (note1)		2.7		5.5	V
Chip Consumed Current	5V Supply Voltage Ta=25°C		1.5		mA
<b>Reference Voltage</b>					
Output voltage	Measure INN	1.2125	1.25	1.2875	V
Line regulation	VDD=2.7~5.5 V		2	20	mV
<b>Under Voltage Look Out</b>					
Positive Going Threshold	Ta=25°C	2.4	2.5	2.6	V
Hysteresis	Note4	0.01	0.1	0.2	V
<b>Ramp Wave Generator and Lamp Frequency</b>					
Operating Frequency		50		400	KHz
Output peak	Note2		1.5		V
Output valley			0.25		V
<b>Error Amplifier</b>					
Input voltage		0.1		3	V
Open loop gain	Note3	60	80		dB
Unit gain band width		1	1.5		MHz
<b>SST Power On Initialization and Open Lamp Enable</b>					
Output current			25/R <sub>RTDLY</sub>		mA
Power On Reset	VDD=5V, Ta=25°C		0.5		V
Open Lamp Detection Enable			1.5		V
<b>Open Lamp Protection</b>					
OLP pin Open lamp detection lower threshold	VDD=5V, Ta=25°C		300		mV
Hysteresis	Note 4		20		mV
<b>Over Voltage Clamping</b>					
CLAMP pin detection lower threshold	VDD=5V, Ta=25°C		1.5		V
Hysteresis			20		mV
INN pin driving current			180		uA
<b>On/Off Function</b>					
The threshold of EA pin	VDD=5V, Ta=25°C		1.2		V
Internal pulled low resistance			80K		Ω
<b>PWM dimming</b>					

Ramp Wave Peak		1.5	V
Ramp Wave Valley		0.5	V
PWM Frequency		10	100K Hz
100 % Brightness Dimming Voltage on pin DIMDC	VDD=5V, Ta=25°C		0.5 V
0 % Brightness Dimming Voltage on pin DIMDC		1.5	V
Pulled high resistance of Pin PWMOUT output for making the dark burst		200	Ω
Pin PWMOUT output for making the bright burst		Floating	
<b>Output</b>			
CMOS output impedance	(Note3, Note4)	50	Ω
Rising Time	VDD=5V, 1000pF(Note3, Note4)	110	ns
Falling Time		100	ns

- Note 1. AVDD and PVDD must be set to an equal supply voltage VDD in typical application.
- Note 2. The lamp operation frequency is the half of the ramp wave frequency.
- Note 3. Only verified by simulation. Not 100% tested.
- Note 4. The voltages of the output drivers are VDD in each off states.

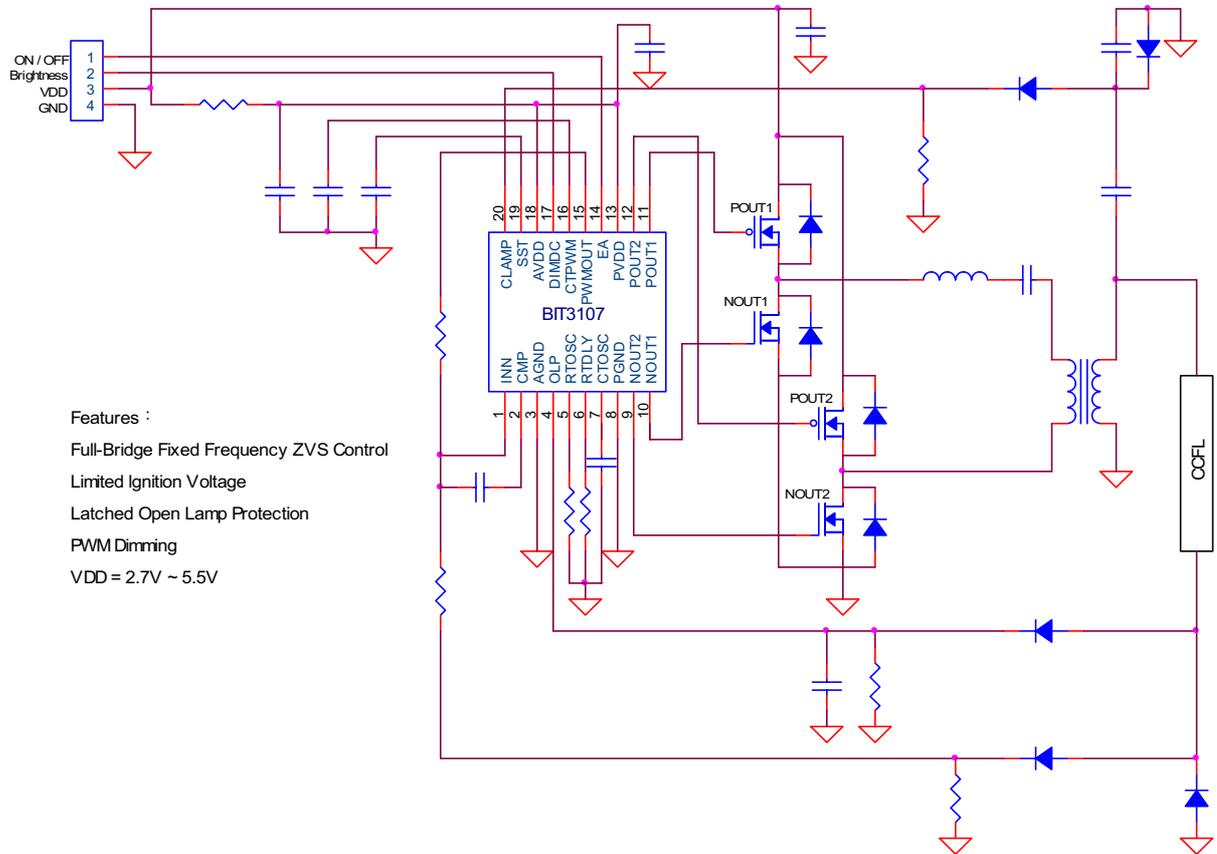
**Timing Diagram**

BIT3107 uses new developed fixed frequency full bridge driving methodology to drive CCFL. The lower side switches, NMOSFET, are driven by fixed frequency and fixed > 50% duty cycle signals. The upper side switches, PMOSFET, are driven by fixed frequency PWM controlled signals. The detail timing relationship is shown as below:



If the lamp operation frequency is set to higher than resonant frequency of the LC tank, symmetry ZVS switching operation can be performed. A well-controlled delay and overlap timing relationship play the key role of this control scheme. It can be set through using proper resistor connected on RTDLY pin. (*Patent pending*)

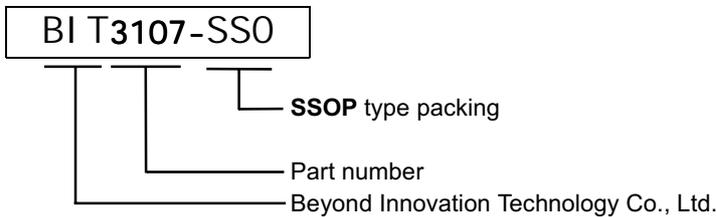
**Application Information:**



- Features :
- Full-Bridge Fixed Frequency ZVS Control
  - Limited Ignition Voltage
  - Latched Open Lamp Protection
  - PWM Dimming
  - VDD = 2.7V ~ 5.5V

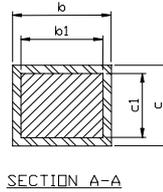
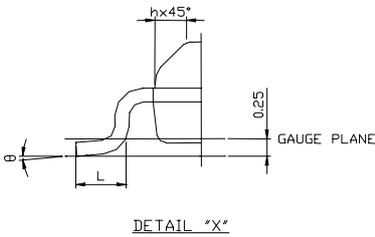
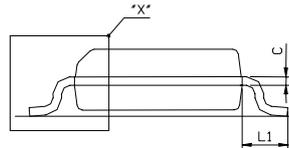
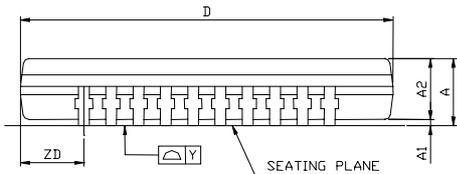
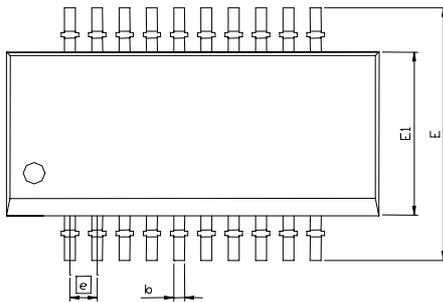
A Typical application of BIT3107

**Order Information:**



**Package Information :**

SSOP type :



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20	0.254	0.30	8	10	12
b1	0.20	0.254	0.28	8	10	11
c	0.18	0.203	0.25	7	8	10
c1	0.18	0.203	0.23	7	8	9
D	8.56	8.66	8.74	337	341	344
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	1.50 REF			58 REF		
Y			0.10			4
$\theta$	0°		8°	0°		8°

NOTE:

1. REFER TO JEDEC STD MO-137 AD
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6 MIL) PER SIDE. PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6 MIL) PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. CONTROLLING DIMENSION: MILLIMETER