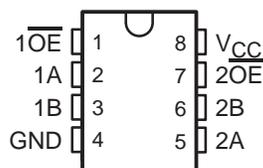


SN74CBTD3306C DUAL FET BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION AND LEVEL SHIFTING

SCDS128 – SEPTEMBER 2003

- Undershoot Protection on A and B Ports Down to -2 V
- Designed to Be Used in Level-Shifting Applications
 - 5-V Input to 3.3-V Output Level Shift
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 3 \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{iO(OFF)} = 5 \text{ pF}$ Typical)
- V_{CC} Operating Range From 4.5 V to 5.5 V
- I_{off} Supports Partial-Power-Down Mode Operation
- TTL-Compatible Control Inputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTD3306C dual FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (\overline{OE}) input is high. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V input to 3.3-V output levels.

The Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3306C provides protection for undershoot down to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper state.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube	SN74CBTD3306CD	CC306C
		Tape and reel	SN74CBTD3306CDR	
	TSSOP – PW	Tape and reel	SN74CBTD3306CPWR	CC306C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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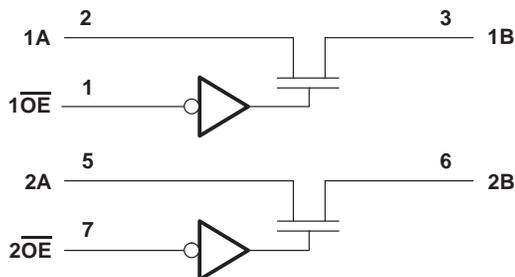
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FUNCTION TABLE
(each bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 3 and 4)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	-40	85	°C

- NOTES: 3. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.8	V
V_{IKU}	Data inputs	$V_{CC} = 5\text{ V}$,	$0\text{ mA} > I_I \geq -50\text{ mA}$, $\overline{OE} = V_{CC}$			-2	V
V_{OH}		See Figure 4					
I_{IN}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_{IN} = V_{CC}$ or GND			± 1	μA
I_{OZ}^\ddagger		$V_{CC} = 5.5\text{ V}$,	$V_{I/O} = V_{CC}$ or GND, $\overline{OE} = V_{CC}$			± 10	μA
I_{off}		$V_{CC} = 0$,	$V_{I/O} = 0$ to 5.5 V			± 10	μA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_{I/O} = 0$, $\overline{OE} = V_{CC}$ or GND			1.5	mA
ΔI_{CC}^\S	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V , Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	$V_{IN} = 3\text{ V}$ or 0				3.5	pF
$C_{io(OFF)}$		$V_{I/O} = 3\text{ V}$ or 0 ,	Switch OFF, $\overline{OE} = V_{CC}$			5	pF
$C_{io(ON)}$		$V_{I/O} = 3\text{ V}$ or 0 ,	Switch ON, $\overline{OE} = \text{GND}$			12.5	pF
r_{on}^\parallel		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_O = 64\text{ mA}$	3	6	Ω
				$I_O = 30\text{ mA}$	3	6	
			$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$	9	20	

V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^\#$	A or B	B or A		0.15	ns
t_{en}	\overline{OE}	A or B	1.5	4.7	ns
t_{dis}	\overline{OE}	A or B	1.5	4.7	ns

The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	$V_{OH}-0.3$		V

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

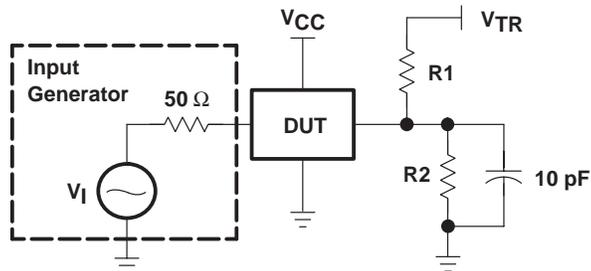


Figure 1. Device Test Setup

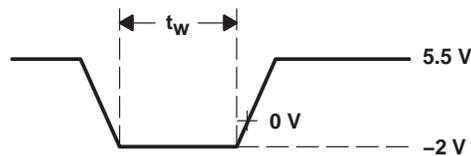


Figure 2. Transient Input Voltage Waveform (Open Socket)

Table 1. Device Test Conditions

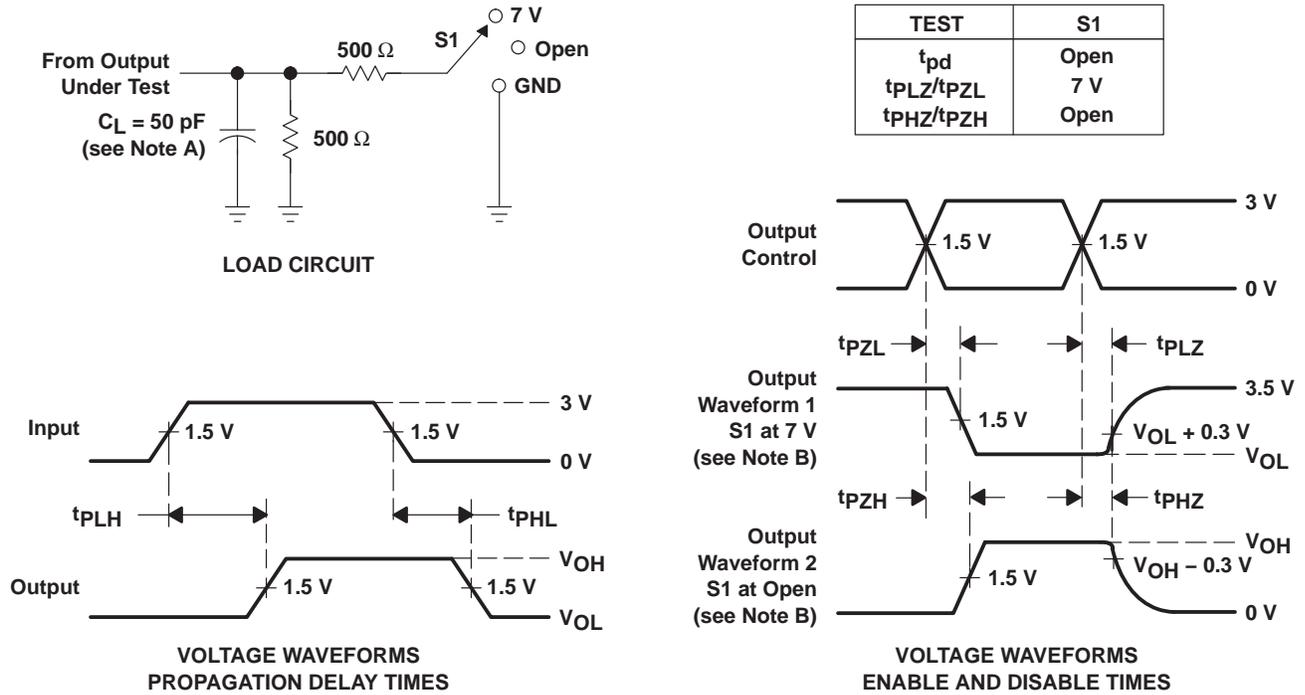
PARAMETER	VALUE	UNIT
B port under test‡	See Figure 1	
V_I	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
$R1 = R2$	100	$k\Omega$
V_{TR}	11	V
V_{CC}	5.5	V

‡ B-port outputs are open (switch is OFF).

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

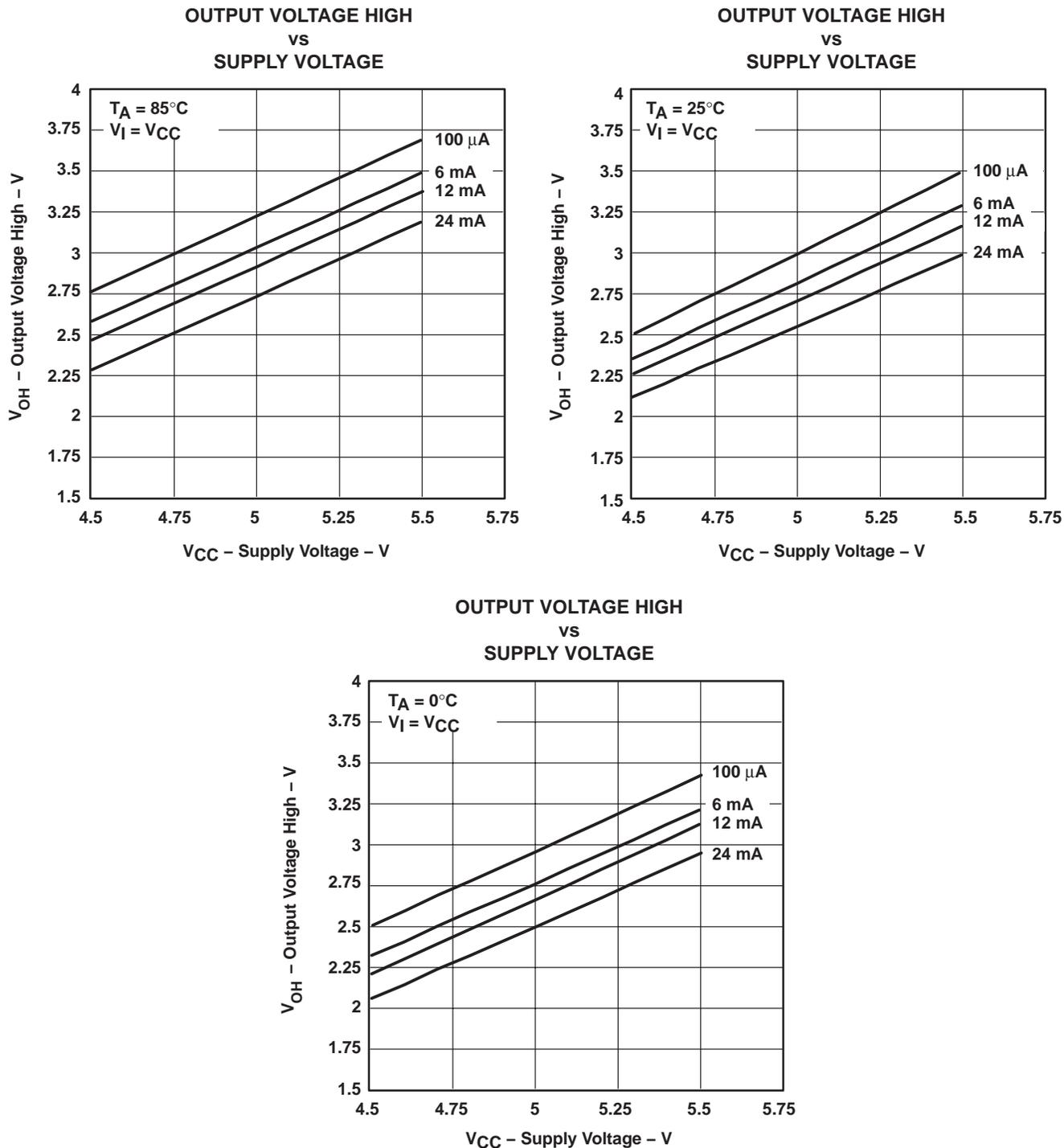


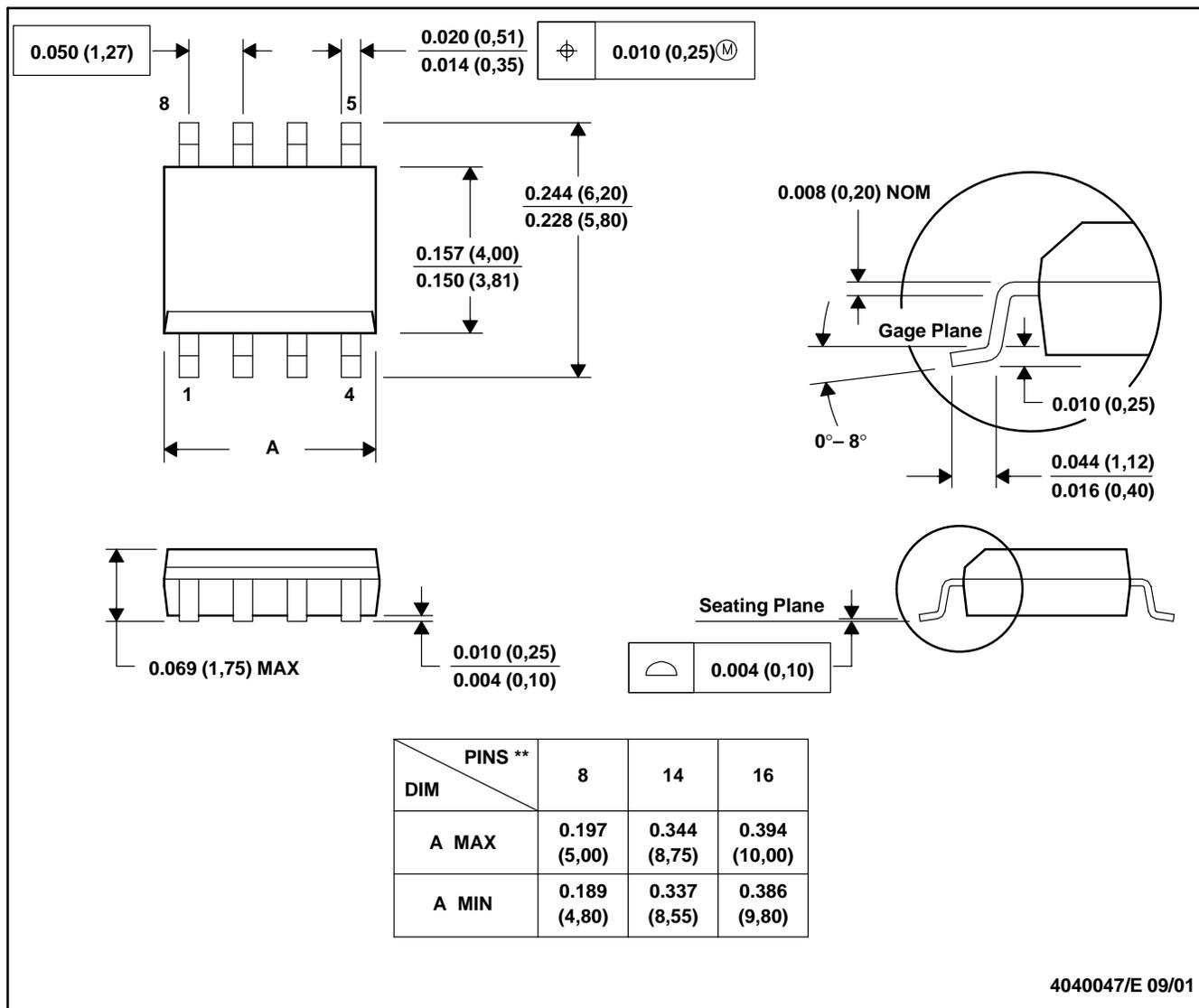
Figure 4. V_{OH} Values



D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

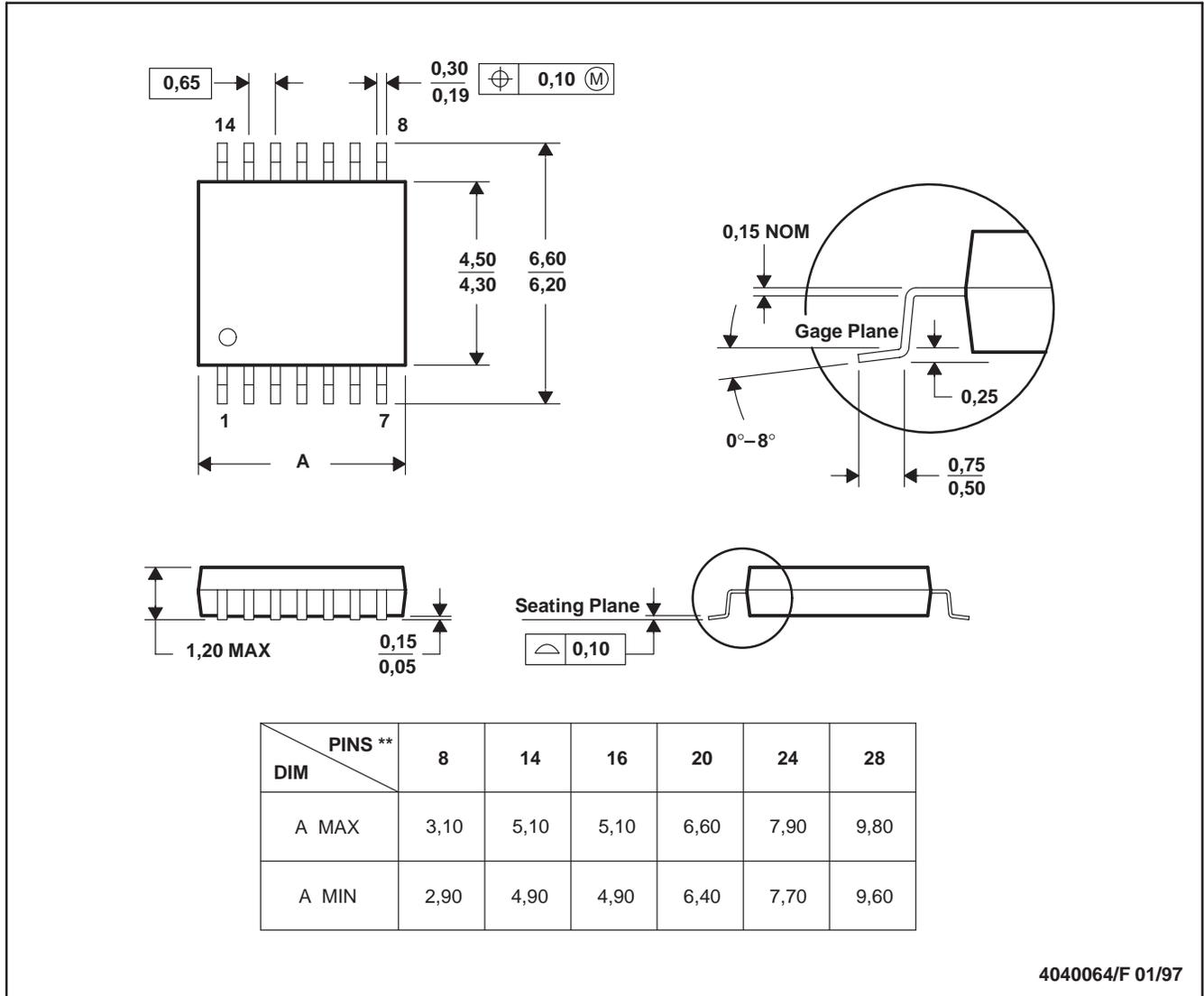


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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