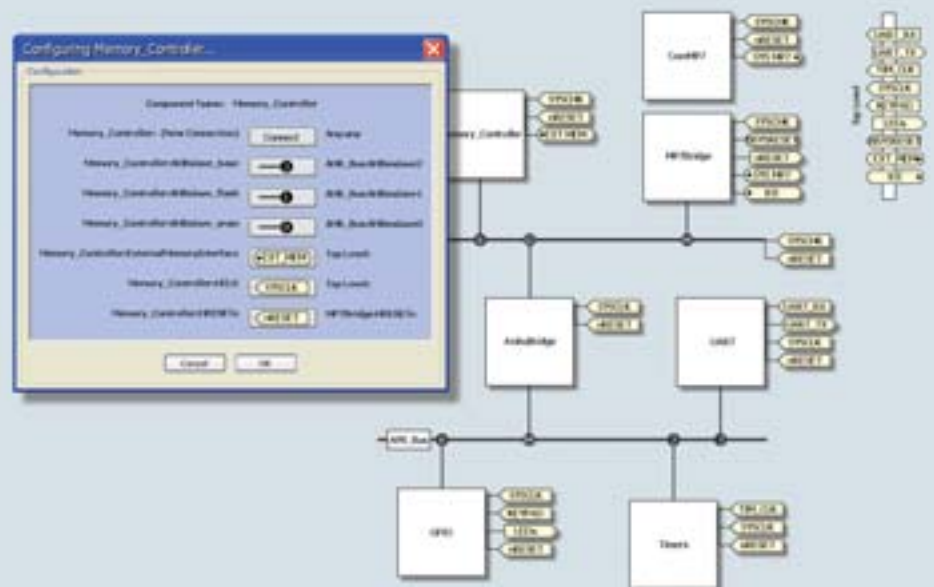# Actel®

CoreConsole

IP DEPLOYMENT PLATFORM SIMPLIFIES DEVELOPMENT OF SYSTEM-LEVEL DESIGNS IN ACTEL FPGAs

The CoreConsole IP Deployment Platform (IDP) and block stitcher has been developed to enable designers to quickly assemble system-level designs and to simplify the construction of the subsystem and assembly of IP blocks within the design. The CoreConsole IDP is a front-end design entry tool that enables IP blocks, designed around the CoreMP7 soft IP ARM7™ family microprocessor, to be stitched together into synthesizable and simulatable RTL that can be exported into the Actel Libero® Integrated Design Environment (IDE). Additionally, the tool delivers all relevant software drivers for the IP to be used with ARM7 software program development tools. The CoreConsole IDP enables users to focus on the system rather than individual components, allowing them to perform efficient system-level evaluation early in the design process and reduce overall development time.
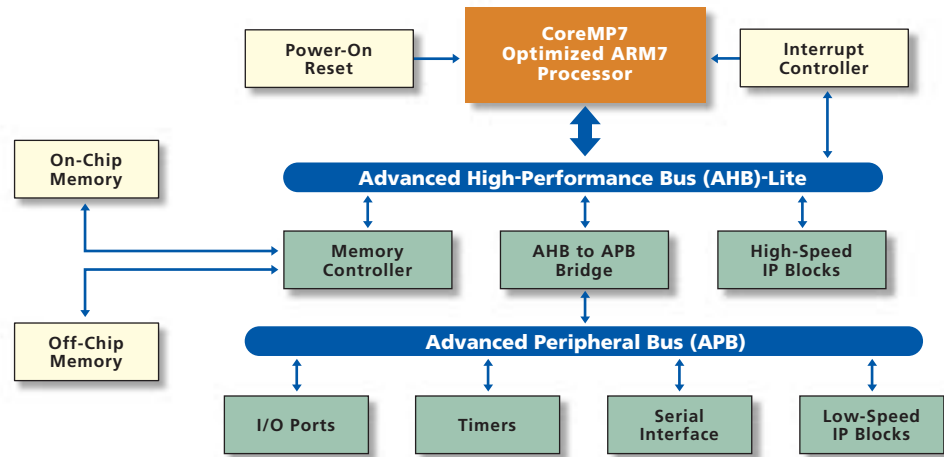
Key Features

— **Enables Rapid Assembly of System-Level Designs**

— **IP Deployment Platform with Secure IP Vault**

— **Supports IP Block Stitching and Configuration**

— **Intuitive, Easy to Use Graphical User Interface (GUI)**

— **Users Can Add Their Own IP Cores**

— **Automatic System Testbench Generation**

— **Includes Configurable Processor Subsystem Blocks for Use with CoreMP7**

CoreConsole GUI and Configuration Interface

CoreConsole Features

CoreConsole is a bus-centric tool implemented at a level of abstraction above the RTL. This makes it independent of the processor, subsystem, and IP blocks, allowing it to be used with a broad range of IP. The tool has an intuitive and easy to use graphical user interface that facilitates rapid assembly of system applications with the Actel CoreMP7. CoreConsole consists of two components: the CoreConsole IDP tool and an IP Vault. The CoreConsole IDP tool supports the integration and configuration of processor subsystem functions (timers, UARTs, etc.) and DirectCores delivered in the IP Vault as well as integration of CompanionCore IP blocks. The tool also supports the instantiation of user IP and canned IP blocks. CoreConsole enables users to reduce system development time and perform system-level evaluation, and allows them to focus on the system rather than components.

CoreMP7 Subsystem in CoreConsole

CoreConsole is used at the entry phase of the design process and works with RTL. It integrates easily into Libero IDE and other tools and enables users to configure the IP blocks for use in their application. CoreConsole also generates a system interconnect testbench that can be used to debug and validate the connection of the user's application within the FPGA fabric, and outputs to the software development tool flow to enable the rapid development of the software program that will run on CoreMP7.

Other CoreMP7 Development Tools

Actel offers several other tools that are used in conjunction with CoreConsole to aid users in the development of system-level applications with CoreMP7 in M7 ProASIC3 or Fusion devices.

Libero IDE The files generated by CoreConsole fully support the CoreMP7 and the M7 devices within the Actel Libero IDE and Designer software. Libero IDE is a comprehensive FPGA design and development tool that provides start-to-finish design flow guidance and control for novice and experienced users. Libero IDE provides all necessary design tools to create your Actel FPGA design, including simulation, synthesis, and place-and-route.

By combining the Actel internally developed tools with EDA tools from industry leaders such as Magma Design Automation,™ Mentor Graphics,® Synplicity,® and SynaptiCAD™ into a single package, Libero IDE provides a "one-stop shopping" approach. Libero IDE ensures complete tool interoperability, a streamlined design flow, management of all source, design, run, and log files, and seamless passing of all design data between tools from schematic/HDL entry through synthesis, simulation, place-and-route, and device programming.
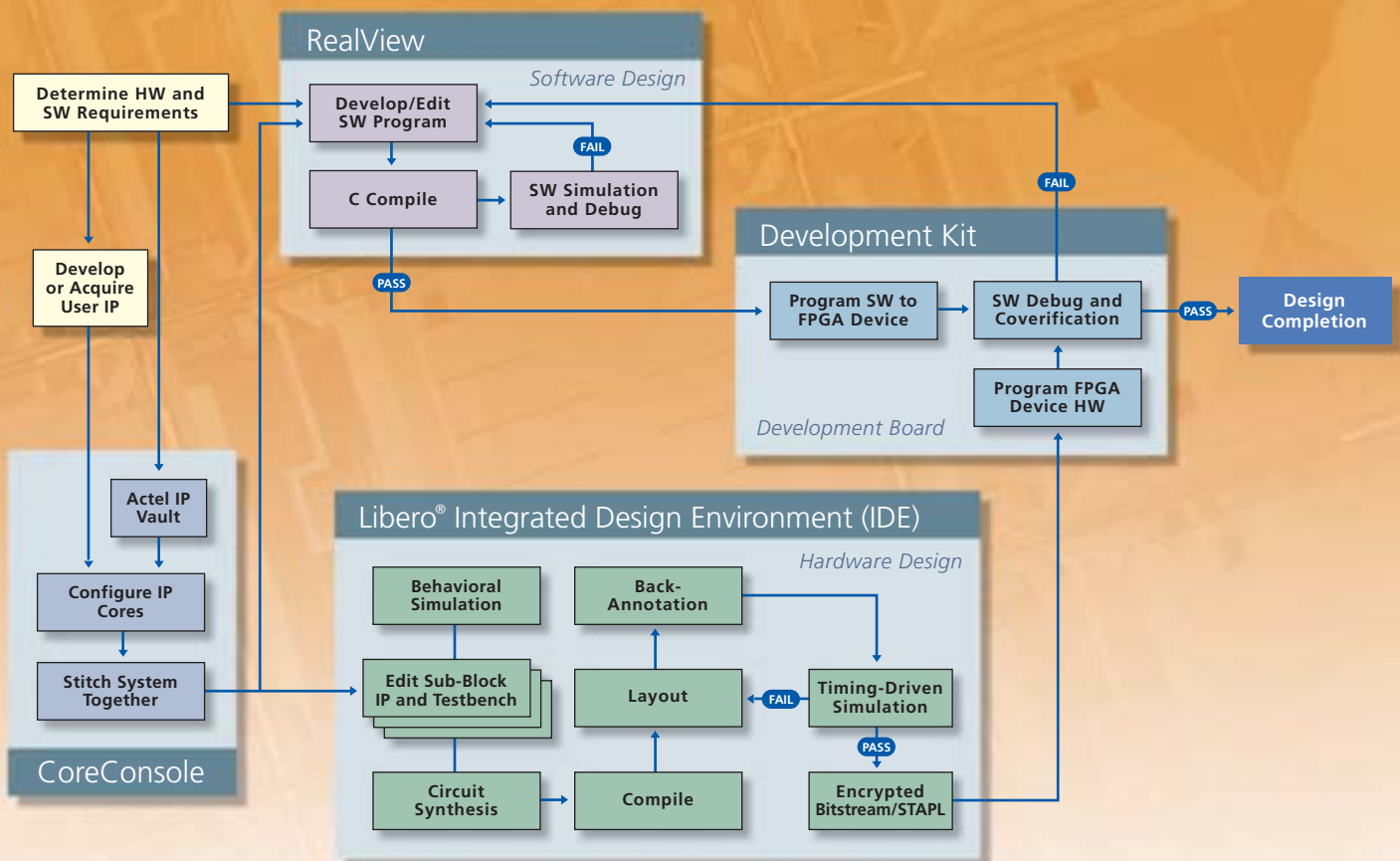
RealView® ARM® has developed an Actel RealView Developer Kit (RVDK) for CoreMP7 that uses the output from CoreConsole and provides tools for building, debugging, and managing software development projects that run on the processor. The toolkit contains an optimized C compiler, debugger, assembler, and instruction set simulator and is available from Actel. Designers can use the RVDK to develop, build, and debug C, C++, and assembly language programs for CoreMP7.

FlashPro3 The FPGA fabric on M7 ProASIC3 and Fusion devices can be programmed and debugged with a FlashPro3 programmer. M7 devices support in-system programming (ISP). To program a device mounted on a system board, a programmer connects to the ISP header. The configuration data is supplied through a standard JTAG interface from a microprocessor, Silicon Sculptor II, or FlashPro3. The FlashPro3 programmer, with its small

size, ease of portability, and USB programming port connections, is ideal for prototyping and development. FlashPro3 allows high-speed programming, and even the largest M7 ProASIC3 and Fusion parts can be programmed in less than two minutes.

Development Kit The CoreMP7 Development Kit is a complete package consisting of a board with an M7 device, Actel Libero IDE Gold, CoreConsole, C program development tools, the FlashPro3 programmer with a USB cable, a power supply, tutorials, and support documentation. Designers can develop their application or explore the various benefits of CoreMP7 in nonvolatile M7 ProASIC3 devices, including ISP, device serialization, and FlashLock® on-chip system security. Additionally, this kit enables designers to quickly and efficiently evaluate the performance and functionality of potential designs for cost-sensitive, ASIC-alternative applications.

CoreConsole and CoreMP7 Development Tools

Actel   **CoreConsole**

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For more information regarding the **Actel CoreConsole IP Development Platform**, please visit the **Actel** website at **www.actel.com** or contact or your local sales representative.

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