

GENERAL DESCRIPTION

The FDC37C65C+ is a CMOS device which interfaces a host microprocessor to up to four floppy disk drives. It integrates the Formatter/Controller, Data Separator, Write Precompensation generator, Data Rate Selector, Clock Generator, and FIFO in one package. The FDC37C65C+ provides a complete microprocessor interface, a microsequencer, and a disk drive interface.

Toshiba vertical (perpendicular) recording is supported as well as conventional longitudinal format recording. This is required for the new 2.88MB floppy disk drives.

The microprocessor interface of the FDC37C65C+ supports a 12 MHz microprocessor bus without the use of wait states. For PC and PC/AT applications, the device provides qualification of interrupt and DMA requests.

The disk drive interface of the FDC37C65C+ directly connects to up to four drives. All drive-related outputs can sink 48 mA; all host related-outputs can sink 24 mA. All host- and drive-related inputs except for the data bus and crystal have internal Schmitt triggers.

The FDC37C65C+ uses two clock inputs which provide the necessary signals for internal timing. A 9600, 16/32 MHz oscillator handles the data rates of 1 Mbit, 500, 250, and 125 Kbits/sec. Internal crystal oscillator circuits may be used with the 44-pin PLCC package. The 40-pin DIP requires TTL clock inputs.

The FDC37C65C+ may be used in applications using two speed disk drives, such as AT compatible systems.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
HOST PROCESSOR INTERFACE				
7-14	7-14	Data 0-7	D0-D7	Input/Output. The data bus connection used by the host microprocessor to transmit and receive data to and from the FDC37C65C+. These pins are in a high-impedance state when not in output mode.
1	1	$\overline{\text{Read}}$	$\overline{\text{RD}}$	Input. This active low signal is issued by the host microprocessor to indicate a read operation. A low level on this input when the FDC37C65C+ is selected enables data from the Buffer or Status Register onto the data bus for reading by the host.

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2	2	$\overline{\text{Write}}$	$\overline{\text{WR}}$	Input. This active low signal is issued by the host microprocessor to indicate a write operation. A low level on this input when the FDC37C65C+ is selected enables data from the data bus to be written into the FDC37C65C+, latching the data on the rising edge.
3	3	$\overline{\text{Chip Select}}$	$\overline{\text{CS}}$	Input. This active low signal issued by the host microprocessor allows data transfers to occur.
4	4	Address 0	A0	Input. This host processor signal determines whether data or status information will appear on the Data Bus. A low level selects the status level; a high level selects the data register.
15	15	Direct Memory Access Request	DMA	Output. This active high signal is a DMA request for byte transfers of data. This signal is cleared when the host responds with the $\overline{\text{DACK}}$ signal going low. This signal is normally driven in the Base Mode. When the FDC37C65C+ is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN signal from the Digital Output Register.
5	5	$\overline{\text{DMA Acknowledge}}$	$\overline{\text{DACK}}$	Input. A low level on this pin indicates a response by the host to a DMA request. It is used by the DMA controller to transfer data to or from the FDC37C65C+. Logical equivalent to $\overline{\text{CS}}$ and A0 = logic "1". In Special or PC/AT mode, this signal is qualified by DMAEN from the Digital Output Register.

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6	6	Terminal Count	TC	Input. This active high signal indicates to the FDC37C65C+ that data transfers are complete. In Base Mode, TC will be qualified by \overline{DACK} only in DMA operations. In non-DMA (Programmed I/O) operations, \overline{CS} and the \overline{RD} and \overline{WR} signals are used as a gating function. In Special or PC/AT mode, TC will always be qualified by \overline{DACK} (whether in DMA or non-DMA operation), but will only be qualified by \overline{DACK} if DMAEN from the Digital Output Register is a logic "1". If the FIFO is not enabled, all operations will terminate successfully with the use of TC qualified as described above. In non-DMA operations where TC is not used, the operations will terminate successfully but report termination errors on the completion of the command. If the FIFO is enabled, all DMA operations will terminate successfully.
16	16	Interrupt	IRQ	Output. This interrupt indicates the completion of command execution and in non-DMA operation also indicates data transfer requests. This signal is normally driven in the Base mode. When the FDC37C65C+ is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN signal from the Digital Output Register.
18	17	$\overline{\text{Load Digital Output Register}}$	\overline{LDOR}	Input. Active low Digital Output Register load enable. When \overline{LDOR} and \overline{WR} are low, the Data Bus is enabled into the Digital Output Register, latching on the rising edge of \overline{LDOR} and \overline{WR} . When \overline{LDOR} , \overline{LDCR} and \overline{WR} are low, the Format Control Register is selected.

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19	18	$\overline{\text{Load Data Rate Selection Register}}$	$\overline{\text{LDCR}}$	Input. This active low signal allows access to the Data Rate Selection Register and Format Control Register. When $\overline{\text{LDCR}}$ and $\overline{\text{WR}}$ are low, DB0, DB1 and DB3 of the Data Bus are enabled into this register, latching on the rising edge of $\overline{\text{LDOR}}$ or $\overline{\text{WR}}$. When $\overline{\text{LDCR}}$, $\overline{\text{RD}}$, and $\overline{\text{DCHGEN}}$ are low, the $\overline{\text{DCHG}}$ input status is carried on bit D7 of the Data Bus, while bits D0-D6 remain in the high impedance state. When $\overline{\text{LDOR}}$, $\overline{\text{LDCR}}$ and $\overline{\text{WR}}$ are low, the Format Control Register is selected.
20	19	Reset	RST	Input. This active high signal resets the FDC37C65C+. When RST occurs, the FDC37C65C+ defaults to Base Mode and the data rate is defaulted to 250K MFM (or 125K FM, code dependent, CLK1 = 16 MHz). When RST is active, the high current driver outputs to the disk drive are disabled.
DRIVE INTERFACE				
21	20	$\overline{\text{Read Disk Data}}$	$\overline{\text{RDD}}$	Input. Raw serial bit stream from the disk drive. Each falling edge represents a flux transition of the encoded data.
29	26	$\overline{\text{Write Enable}}$	$\overline{\text{WE}}$	Output. This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
30	27	$\overline{\text{Write Data}}$	$\overline{\text{WD}}$	Output. This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media. This output is enabled only when $\overline{\text{Write Enable}}$ is low.
28	25	$\overline{\text{Head Select}}$	$\overline{\text{HS}}$	Output. This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.

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31	28	$\overline{\text{Direction Control}}$	$\overline{\text{DIRC}}$	Output. This high current output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
32	29	$\overline{\text{Step Pulse}}$	$\overline{\text{STEP}}$	Output. This active low high current driver issues a low pulse for each track-to-track movement of the head.
40	N/A	$\overline{\text{Disk Change}}$	$\overline{\text{DCHG}}$	Input. This active low input senses from the disk drive that the drive door is open or that the diskette has possibly been changed since the last drive selection.
17	N/A	$\overline{\text{Disk Change Enable}}$	$\overline{\text{DCHGEN}}$	Input. This active low input enables the $\overline{\text{DCHG}}$ input status onto D7 during a read of the Digital Input Register. This signal is connected to an internal pull-up resistor.
33	30	$\overline{\text{Drive Select 1}}$	$\overline{\text{DS1}}$	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT/EISA Mode, a logic "0" on DSEL and a logic "1" on MOEN1 from the Digital Output Register will cause $\overline{\text{DS1}}$ to enable the Drive 1 interface. When the FDC37C65C+ is in the Base Mode or the Special Mode, $\overline{\text{DS1}}$ is number 1 of the four decoded Unit Selects, as specified in the device command, and the Digital Output Register has no effect.
35	32	$\overline{\text{Drive Select 2}}$	$\overline{\text{DS2}}$	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT Mode, a logic "1" on DSEL and a logic "1" on MOEN2 from the Digital Output Register will cause $\overline{\text{DS2}}$ to enable the Drive 2 interface. When the FDC37C65C+ is in the Base Mode or the Special Mode, this output is number 2 of the four decoded Unit Selects, as specified in the device command, and the Digital Output register has no effect.

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36	33	<u>Motor</u> <u>On 1/Drive</u> <u>Select 3</u>	<u>MO1/DS3</u>	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT Mode, a logic "1" on MOEN1 from the Digital Output Register will cause this output to go low, thereby acting as the Motor-On Enable for Drive 1. When the FDC37C65C+ is in the Base Mode or the Special Mode, this output is number 3 of the four decoded Unit Selects, as specified in the device command, thereby acting as drive select 3, and the Digital Output Register has no effect.
37	34	<u>Motor</u> <u>On 2/Drive</u> <u>Select 4</u>	<u>MO2/DS4</u>	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT Mode, a logic "1" on MOEN2 from the Digital Output Register will cause this output to go low, thereby acting as the Motor-On Enable for Drive 2. When the FDC37C65C+ is in the Base Mode or the Special Mode, this output is number 4 of the four decoded Unit Selects, as specified in the device command, thereby acting as drive select 4, and the Digital Output Register has no effect.
38	35	<u>Head</u> <u>Loaded</u>	<u>HDL</u>	Output. This active low high current driving signal causes the head to be loaded against the media in the selected drive.
39	36	<u>Reduced</u> <u>Write</u> <u>Current/</u> <u>Revolutions</u> <u>Per Minute</u>	<u>RWC/RPM</u>	Output. This active low signal occurs when tracks greater than 43 are being accessed, and the inner track location has caused increased bit density. This signal, valid in the Base Mode and the Special Mode, indicates that write precompensation is necessary. In the PC/AT mode, this signal may be used to select a 300 RPM spindle rate on two speed drives when 250 Kbps MFM is selected.
41	37	<u>Write</u> <u>Protected</u>	<u>WP</u>	Input. This active low Schmitt Trigger input senses from the disk drive that a disk is write protected.
42	38	<u>Track 00</u>	<u>TR00</u>	Input. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.

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43	39	$\overline{\text{Index}}$	$\overline{\text{IDX}}$	Input. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
27	24	Precompensation Value	PCVAL	Input. The level on this pin determines the amount of write precompensation to be used on the inner tracks of the diskette. When precompensation is disabled, this pin has no effect. This input has an internal pull up resistor.
24	22	Drive Type	DRV	Input. This input is used to indicate the drive type being used. A logic "0" on this input indicates a two speed spindle motor, in which case the second clock input should be grounded. This signal is connected to an internal pull-up resistor.
MISCELLANEOUS				
N/A	23	CLOCK 1	CLK1	16 or 32 MHz TTL level clock input for all standard data rates. The frequency should be accurate to within 0.1% and may have a 40% to 60% duty cycle.
N/A	21	CLOCK 2	CLK2	TTL level clock input for non-standard data rates. The frequency is selected from the Data Rate Selection Register in Table 1.
25,26	N/A	$\overline{\text{Crystal 1}}$, Crystal 1	$\overline{\text{XTAL1}}$, XTAL1	An external 16 MHz or 32 MHz parallel resonant crystal should be connected to these pins for all standard data rates. If an external 16 MHz or 32 MHz TTL clock is used instead, it should be connected to XTAL1 and $\overline{\text{XTAL1}}$ should be left floating.
22,23	N/A	$\overline{\text{Crystal 2}}$, Crystal 2	$\overline{\text{XTAL2}}$, XTAL2	An external parallel resonant crystal should be connected to these pins for all non-standard data rates. If an external TTL clock is used instead, it should be connected to XTAL2 and $\overline{\text{XTAL2}}$ should be left floating.
44	40	Power	V _{cc}	+ 5 Volt supply pin.
34	31	Ground	GND	Ground pin. (Refer to note in DC Electrical Characteristics)

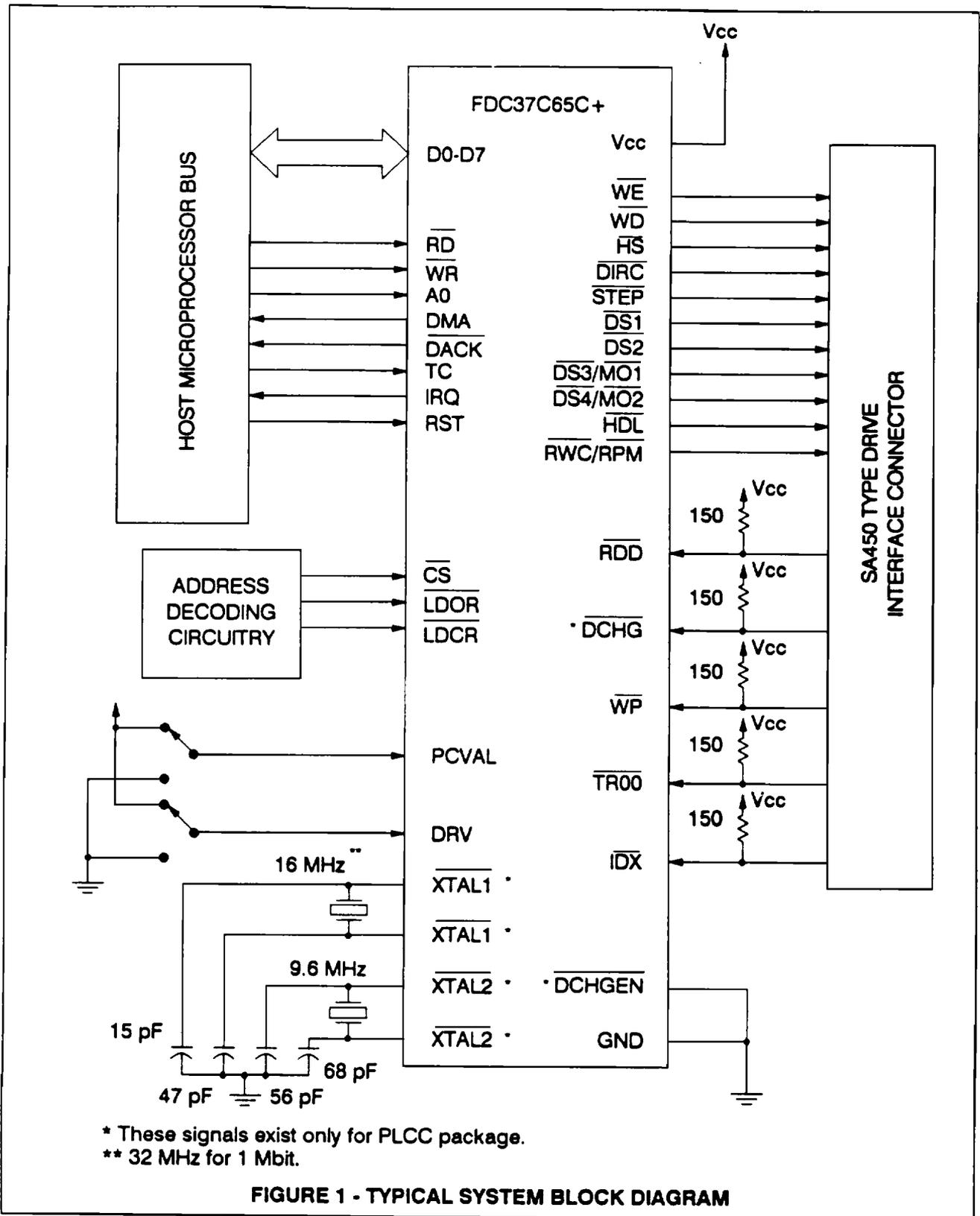
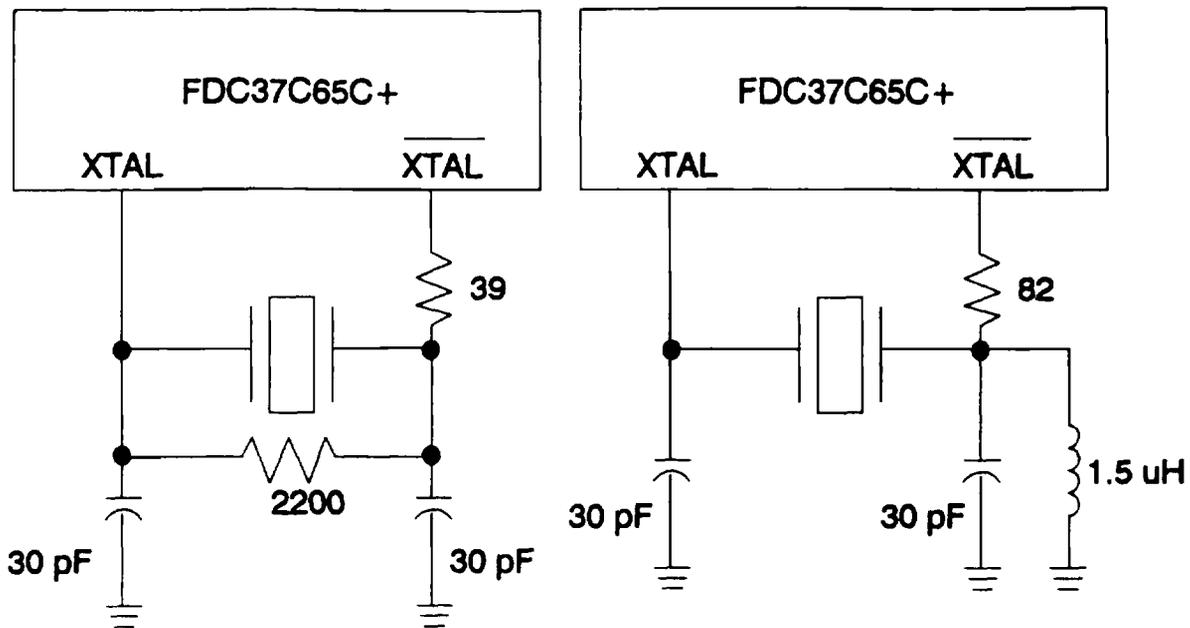
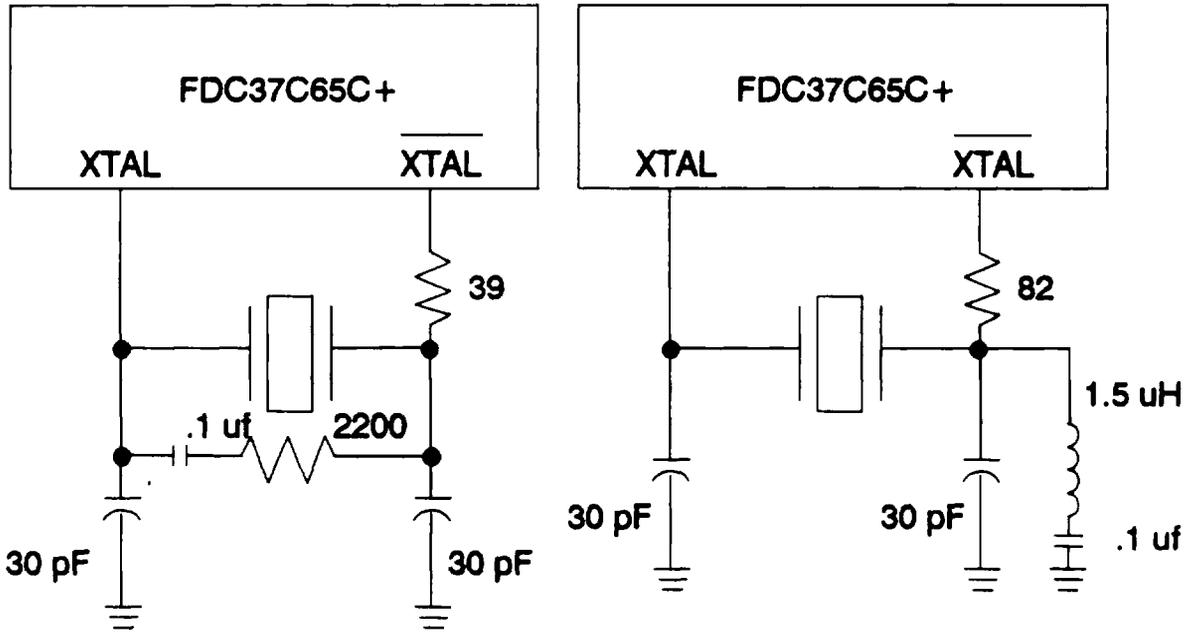


FIGURE 1 - TYPICAL SYSTEM BLOCK DIAGRAM



Crystal: 32 MHz, Parallel Resonant, Third Overtone
 Source: Ecliptek Part No. EC 320-32 00 MHz or equivalent

FIGURE 2 - SUGGESTED OSCILLATOR CIRCUITS



Crystal: 32 MHz, Parallel Resonant, Third Overtone
 Source: Ecliptek Part No. EC 320-32 00 MHz or equivalent

FIGURE 2A - SUGGESTED LOW POWER OSCILLATOR CIRCUITS

