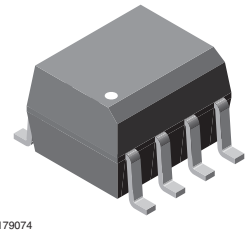
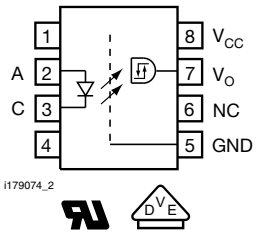
High Speed Optocoupler, Single, 5 MBd, in SOIC-8 Package





FEATURES

- Data rate 5 MBits/s (2.5 MBit/s over temperature)
- Buffer
- Isolation test voltage, 4000 V_{RMS}
- TTL, LSTTL and CMOS compatible
- Internal shield for very high common mode transient immunity
- Wide supply voltage range (4.5 V to 15 V)
- Low input current (1.6 mA to 5 mA)
- Parameters specified from 0 °C to 85 °C
- T_{amb} from -40 °C to 100 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e3

RoHS COMPLIANT

DESCRIPTION

The single channel 5 Mb/s SFH6720 and SFH6721 high speed optocoupler consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector. The detector incorporates a Schmitt-trigger stage for improved noise immunity. A Faraday shield provides a common mode transient immunity of 1000 V/µs at V_{CM} = 50 V for SFH6720 and 2500 V/µs at V_{CM} = 400 V for SFH6721.

AGENCY APPROVALS

- UL1577, file no. E52744 system code Y
- DIN EN 60747-5-5 (VDE 0884) available with option 1

APPLICATIONS

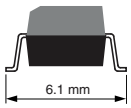
- Industrial control
- Replace pulse transformers
- Routine logic interfacing
- Motion / power control
- High speed line receiver
- Microprocessor system interfaces
- Computer peripheral interfaces

ORDERING INFORMATION

S	F	H	6	7	2	#	T

PART NUMBER

TAPE AND REEL



AGENCY CERTIFIED/PACKAGE	CMR (kV/µs)	CMR (kV/µs)
UL	**1**	**2.5**
SOIC-8	SFH6720T	SFH6721T
VDE, UL	**1**	**2.5**
SOIC-8	SFH6720-X001T	-

TRUTH TABLE (positive logic)

PART	IR DIODE	OUTPUT
SFH6720	On	H
	Off	L
SFH6721	On	H
	Off	L

ABSOLUTE MAXIMUM RATINGS (1) (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
INPUT				
Reverse voltage		V_R	3	V
DC forward current		I_F	10	mA
Surge forward	$t_p \leq 1$ µs, 300 pulses/s	I_{FSM}	1	mA
Power dissipation		P_{diss}	20	mW
OUTPUT				
Supply voltage		V_{CC}	-0.5 to +15	V
Output voltage		V_O	-0.5 to +15	V
Average output current		I_O	25	mA
Power dissipation		P_{diss}	100	mW
COUPLER				
Storage temperature range		T_{stg}	-55 to +125	°C
Ambient temperature range		T_{amb}	+ 85	°C
Lead soldering temperature	t = 10 s	T_{sld}	260	°C

Note

(1) Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability

RECOMMENDED OPERATING CONDITIONS (1)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Supply voltage		V_{CC}	4.5		15	V
Forward input current		I_{Fon}	1.6 (2)		5	mA
		I_{Foff}			0.1	mA
Operating temperature		T_A	-40		85	°C

Notes

(1) A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used

(2) We recommended using a 2.2 mA if to permit at least 20 % CTR degradation guard band

ELECTRICAL CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
INPUT						
Forward voltage	I_F = 5 mA, 25 °C	V_F		1.6	1.75	V
		V_F			1.9	V
Input current hysteresis	V_{CC} = 5 V, $I_{HYS} = I_{Fon} - I_{Foff}$	I_{HYS}	0.1			V
Reverse current	V_R = 3 V	I_R		0.5	10	µA
Capacitance	V_R = 0 V, f = 1 MHz	C_O		60		pF
Thermal resistance		R_{thja}		700		K/W

ELECTRICAL CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
OUTPUT						
Logic low output voltage	I_{OL} = 6.4 mA	V_{OL}			0.5	V
Logic high output voltage	I_{OH} = - 2.6 mA, V_{OH} = V_{CC} - 1.8 V	V_{OH}	2.4			V
Output leakage current (V_{OUT} > V_{CC})	V_O = 5.5 V, V_{CC} = 4.5 V, I_F = 5 mA	I_{OHH}		0.5	100	µA
	V_O = 15 V, V_{CC} = 4.5 V, I_F = 5 mA	I_{OHH}		1	500	µA
Logic low supply current	V_{CC} = 5.5 V, I_F = 0	I_{CCL}		3.7	6	mA
	V_{CC} = 15 V, I_F = 0	I_{CCL}		4.1	6.5	mA
Logic high supply current	V_{CC} = 5.5 V, I_F = 5 mA	I_{CCH}		3.4	4	mA
	V_{CC} = 15 V, I_F = 5 mA	I_{CCH}		3.7	5	mA
Logic low short circuit output current (output short circuit time ≤ 10 ms)	V_O = V_{CC} = 5.5 V, I_F = 0	I_{OSL}	25			mA
	V_O = V_{CC} = 15 V, I_F = 0	I_{OSL}	40			mA
Logic high short circuit output current (output short circuit time ≤ 10 ms)	V_{CC} = 5.5 V, V_O = 0 V, I_F = 5 mA	I_{OSH}			- 10	mA
	V_{CC} = 15 V, V_O = 0 V, I_F = 5 mA	I_{OSH}			-25	mA
Thermal resistance		R_{thja}		300		K/W
COUPLER						
Capacitance (input to output)	f = 1 MHz, pins 1 to 4 and 5 to 8 shorted together	C_{IO}		0.6		pF

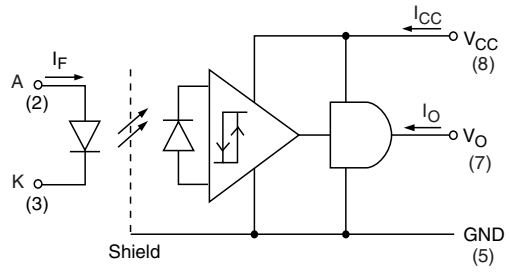
Note

(1) - 40 ° C ≤ T_{amb} ≤ 85 °C; 4.5 V ≤ V_{CC} ≤ 15 V; 1.6 mA ≤ I_{Fon} ≤ 5 mA; 2 ≤ V_{EH} ≤ 15 V; 0 ≤ V_{EL} ≤ 0.8 V; 0 mA ≤ I_{Foff} ≤ 0.1 mA.
Typical values: T_{amb} = 25 °C; V_{CC} = 5 V; I_{Fon} = 3 mA unless otherwise specified.
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements

SWITCHING CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Propagation delay time to logic low output level	Without peaking capacitor	t_{PHL}		120		ns
	With peaking capacitor	t_{PHL}		115	300	ns
Propagation delay time to logic high output level	Without peaking capacitor	t_{PLH}		125		ns
	With peaking capacitor	t_{PLH}		90	300	ns
Output rise time	10 % to 90 %	t_r		40		ns
Output fall time	90 % to 10 %	t_f		10		ns

Note

(1) 0 °C ≤ T_{amb} ≤ 85 °C; 4.5 V ≤ V_{CC} ≤ 15 V; 1.6 mA ≤ I_{Fon} ≤ 5 mA; 0 mA ≤ I_{Foff} ≤ 0.1 mA
Typical values: T_{amb} = 25 ° C; V_{CC} = 5 V; I_{Fon} = 3 mA unless otherwise specified. A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used



COMMON MODE TRANSIENT IMMUNITY (1)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic high common mode transient immunity (2)	$\|V_{CM}\|$ = 50 V, I_F = 1.6 mA	SFH6720	$\|CM_H\|$	1000			V/µs
	$\|V_{CM}\|$ = 300 V, I_F = 1.6 mA	SFH6721	$\|CM_H\|$	5000			V/µs
Logic low common mode transient immunity (2)	$\|V_{CM}\|$ = 50 V, I_F = 0 mA	SFH6720	$\|CM_L\|$	1000			V/µs
	$\|V_{CM}\|$ = 1000 V, I_F = 0 mA	SFH6721	$\|CM_L\|$	10 000			V/µs

Note

(1) T_{amb} = 25 °C, V_{CC} = 5 V (2)

(2) CM_H is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level (V_O > 2 V). CM_L is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic low level (V_O < 0.8 V)

SAFETY AND INSULATION RATINGS				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		55/100/21	
Pollution degree	According to DIN VDE 0109		2	
Comparative tracking index	Insulation group IIIa	CTI	175	
Maximum rated withstanding isolation voltage	According to UL1577, t = 1 min	V_{ISO}	3333	V_{RMS}
Tested withstanding isolation voltage	According to UL1577, t = 1 s	V_{ISO}	4000	V_{RMS}
Maximum transient isolation voltage	According to DIN EN 60747-5-5	V_{IOTM}	6000	V_{peak}
Maximum repetitive peak isolation voltage	According to DIN EN 60747-5-5	V_{IORM}	560	V_{peak}
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	≥ 10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	≥ 10^{11}	Ω
Output safety power		P_{SO}	350	mW
Input safety current		I_{SI}	150	mA
Input safety temperature		T_S	165	°C
Creepage distance	SOIC-8		≥ 4	mm
Clearance distance	SOIC-8		≥ 4	mm
Insulation thickness		DTI	≥ 0.2	mm

Note

- As per IEC 60747-5-5, § 7.4.3.8.2, this optocoupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

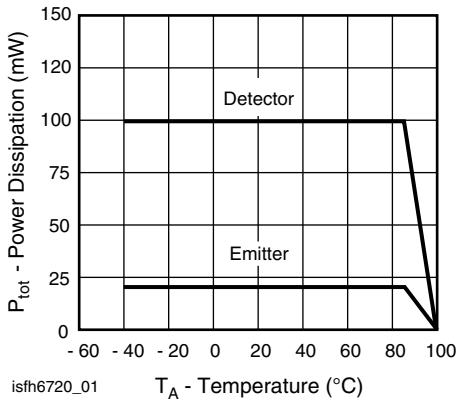


Fig. 1 - Permissible Total Power Dissipation vs. Temperature

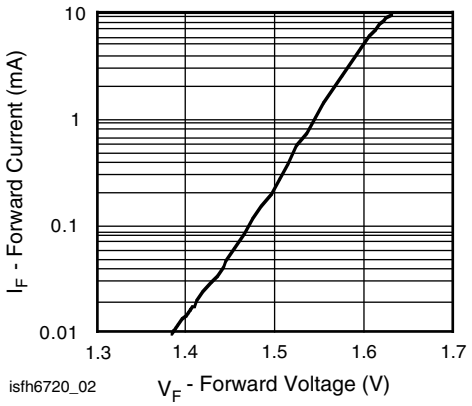


Fig. 2 - Typical Input Diode Forward Current vs. Forward Voltage

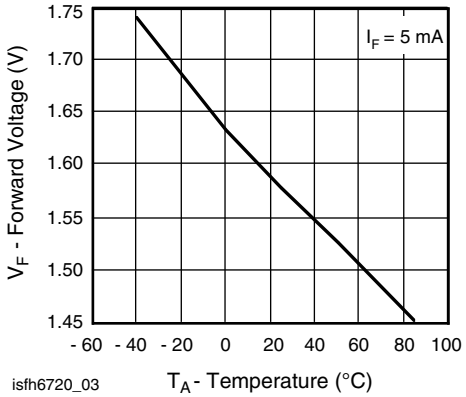


Fig. 3 - Typical Forward Input Voltage vs. Temperature

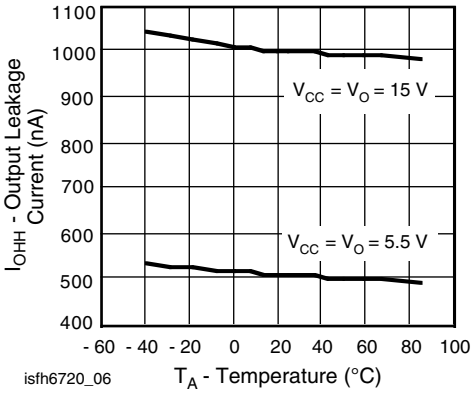


Fig. 6 - Typical Output Leakage Current vs. Temperature

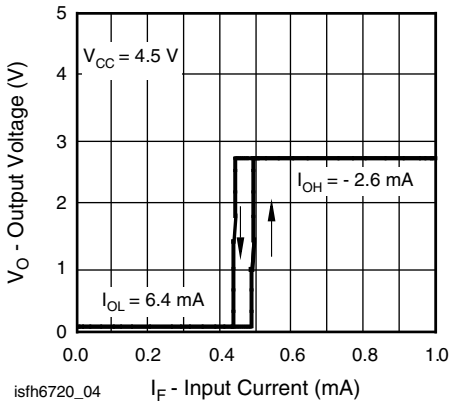


Fig. 4 - Typical Output Voltage vs. Forward Input Current

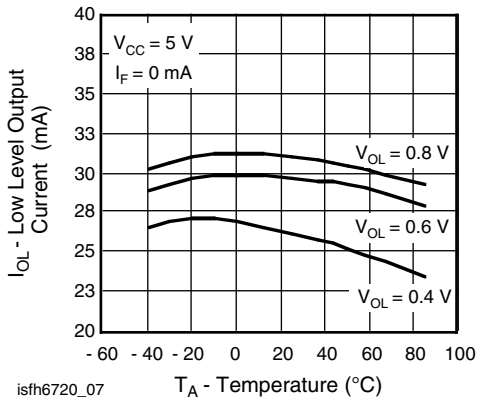


Fig. 7 - Typical Low Level Output Current vs. Temperature

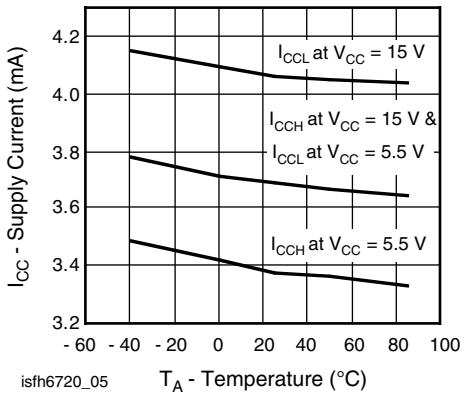


Fig. 5 - Typical Supply Current vs. Temperature

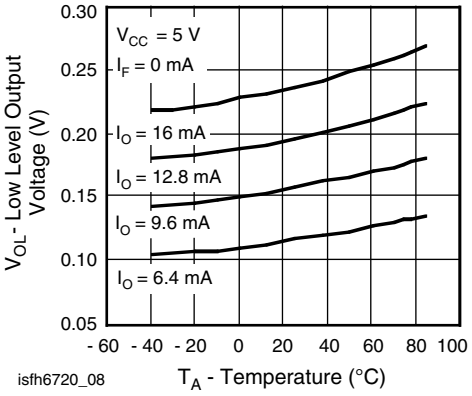


Fig. 8 - Typical Low Level Output Voltage vs. Temperature

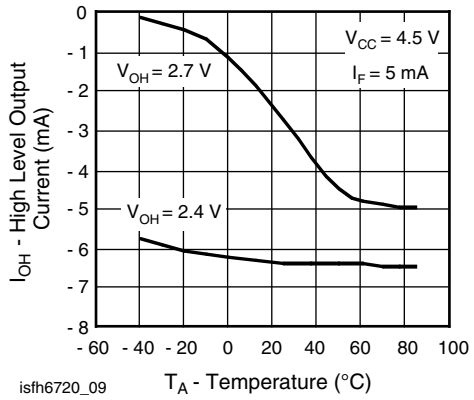


Fig. 9 - Typical High Level Output Current vs. Temperature

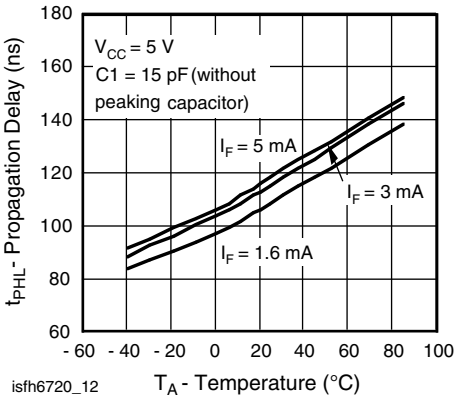


Fig. 12 - Typical Propagation Delays to Logic Low vs. Temperature

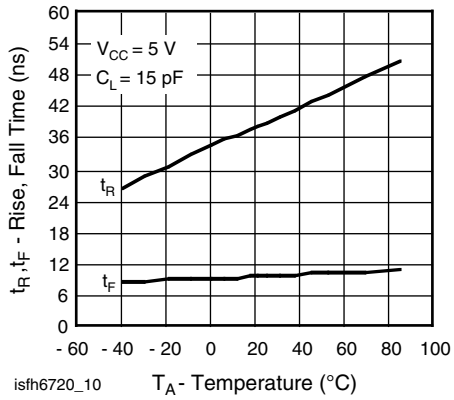


Fig. 10 - Rise and Fall Time vs. Ambient Temperature

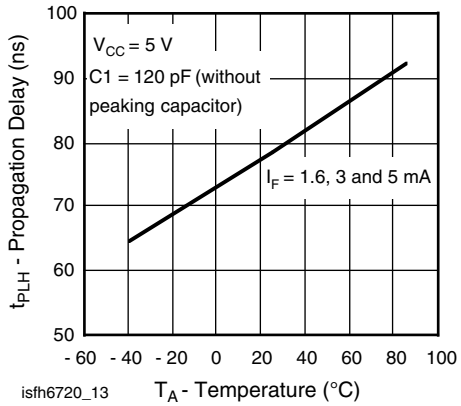


Fig. 13 - Typical Propagation Delays to Logic High vs. Temperature

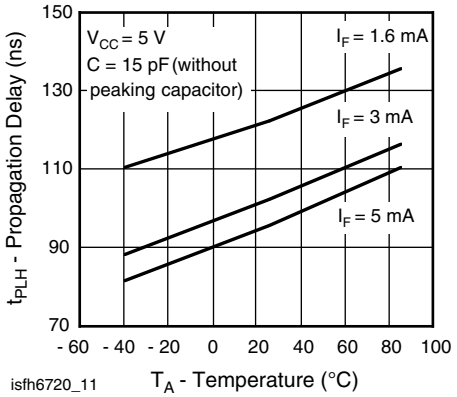


Fig. 11 - Typical Propagation Delays to Logic High vs. Temperature

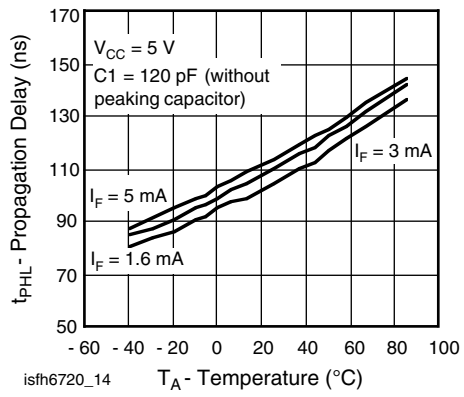


Fig. 14 - Typical Propagation Delays to Logic Low vs. Temperature

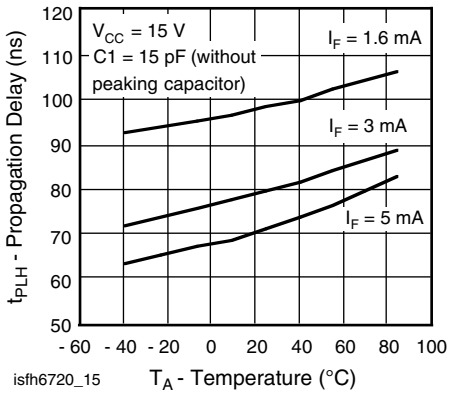


Fig. 15 - Typical Propagation Delays to Logic High vs. Temperature

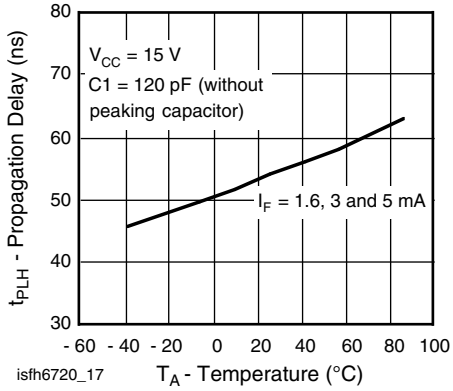


Fig. 17 - Typical Propagation Delays to Logic High vs. Temperature

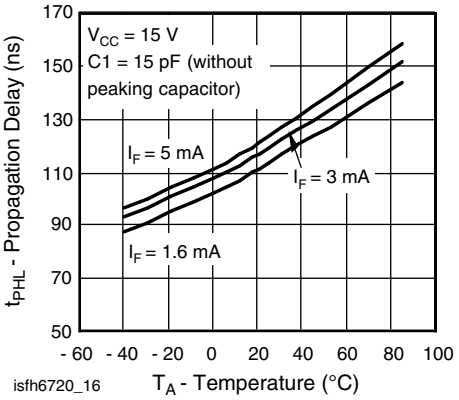


Fig. 16 - Typical Propagation Delays to Logic Low vs. Temperature

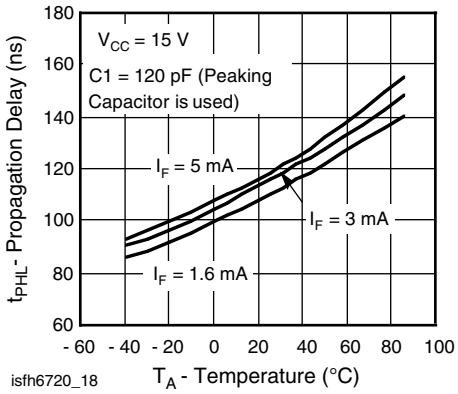
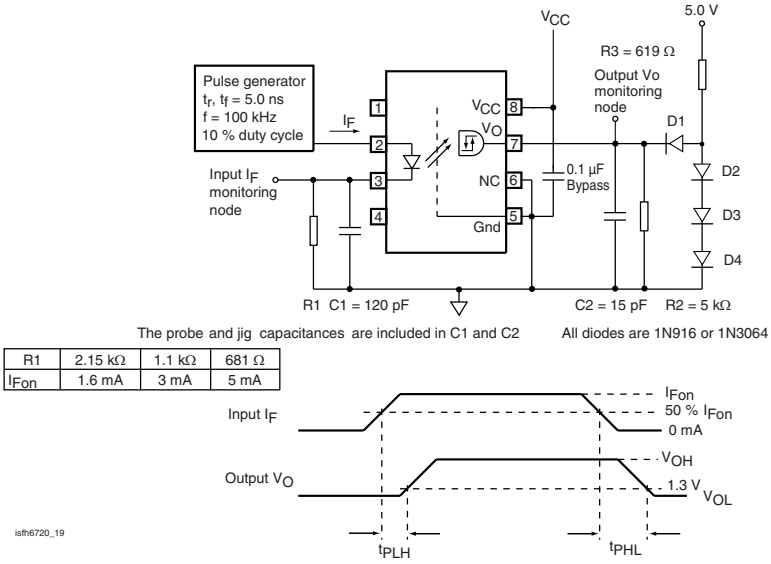


Fig. 18 - Typical Propagation Delays to Logic Low vs. Temperature



R1	2.15 kΩ	1.1 kΩ	681 Ω
I_{Fon}	1.6 mA	3 mA	5 mA

Fig. 19 - Test Circuit for t_{PLH}, t_{PHL}, t_R and t_f

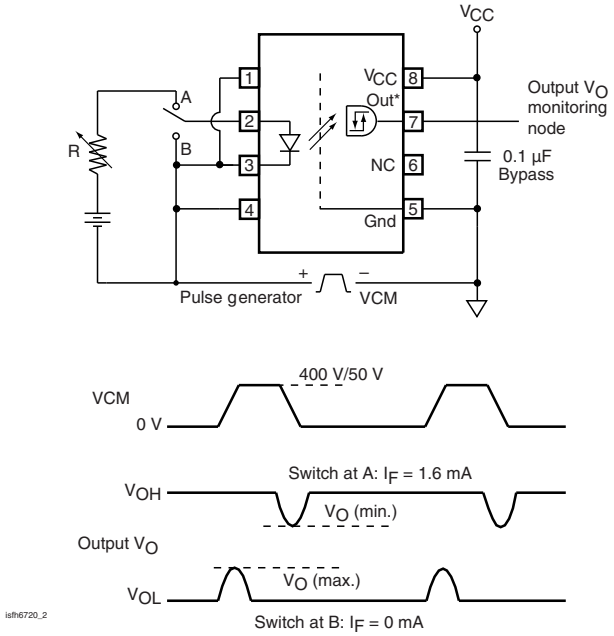


Fig. 20 - Test Circuit for Common Mode Transient Immunity and Typical Waveforms

PACKAGE DIMENSIONS (in millimeters)

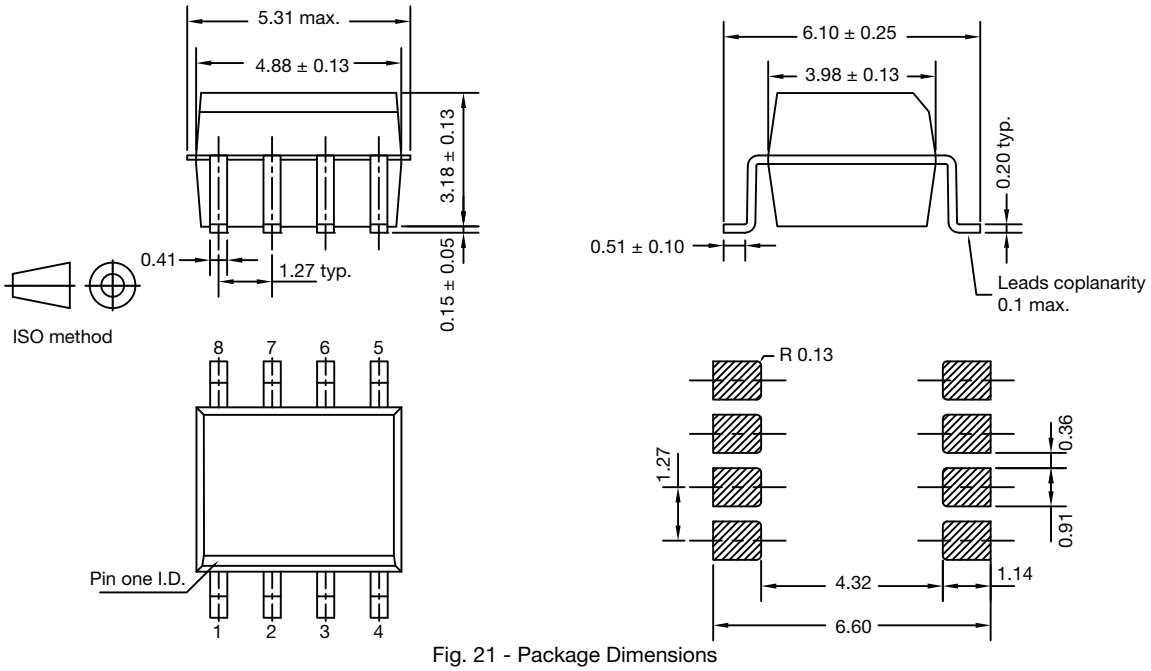


Fig. 21 - Package Dimensions

PACKAGE MARKING

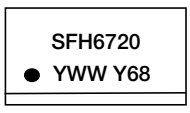


Fig. 22 - SFH6720

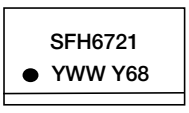


Fig. 23 - SFH6721

Note

- Tape and reel suffix (T) is not part of the package marking

PACKAGE INFORMATION (in millimeters)

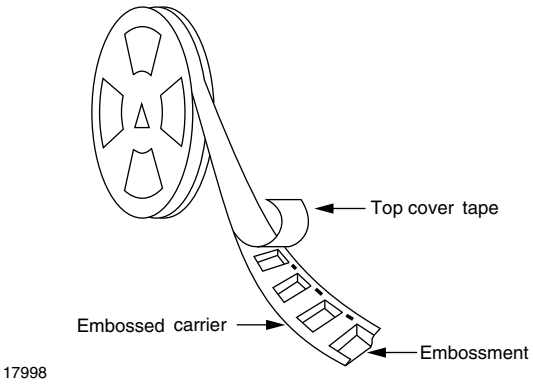


Fig. 24 - Tape and Reel Shipping Medium

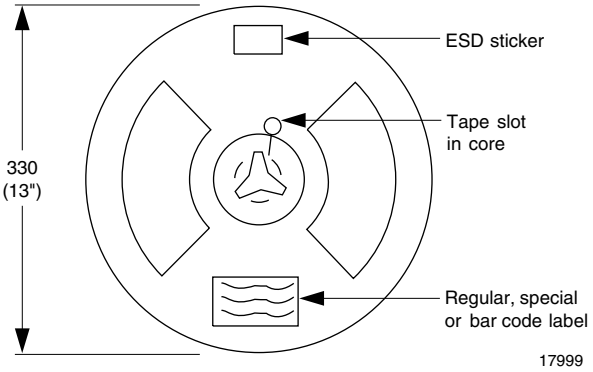


Fig. 25 - Tape and Reel Shipping Medium

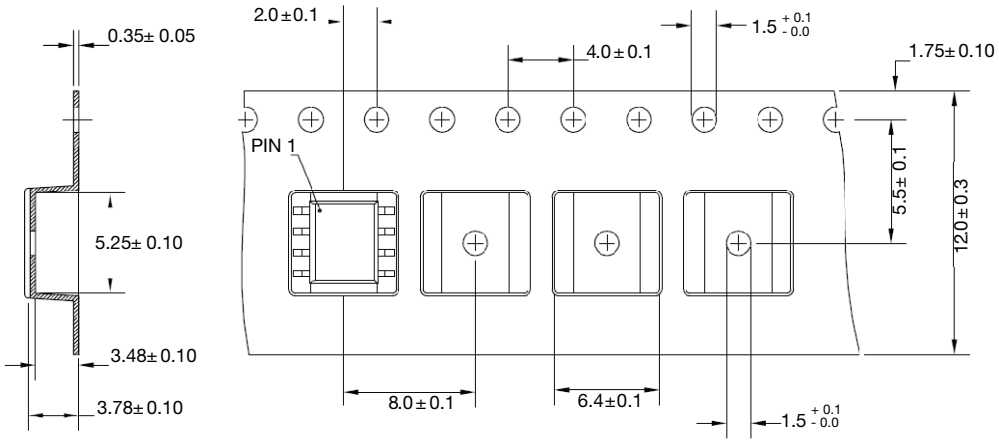


Fig. 26 - Tape and Reel Packing for SOIC (2000 pieces on reel)

SOLDER PROFILES

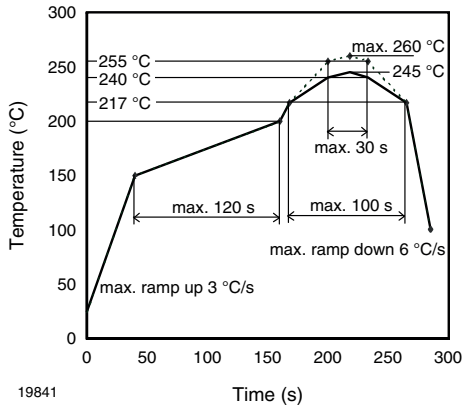


Fig. 27 - Lead (Pb)-free Reflow Solder Profile According to J-STD-020 for SMD Devices

HANDLING AND STORAGE CONDITIONS

ESD level: HBM class 2

Floor life: unlimited

Conditions: T_{amb} < 30 °C, RH < 85 %

Moisture sensitivity level 1, according to J-STD-020

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