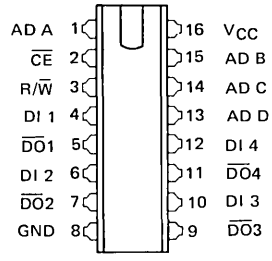
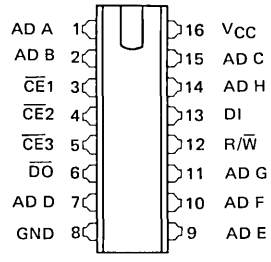
SERIES 54S/74S
RANDOM-ACCESS READ/WRITE MEMORIES

BULLETIN NO. DL-S 7512257, MAY 1975

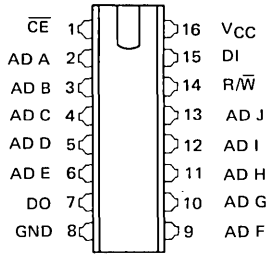
64 BITS (16 WORDS BY 4 BITS)
'S189, 'S289



256 BITS (256 WORDS BY 1 BIT)
'S201, 'S301



1024 BITS (1024 WORDS BY 1 BIT)
SN74S209, SN74S309



Pin assignments for all of these memories are the same for all packages.

- Schottky-Clamped for High Performance
- Full On-Chip Decoding and Fast Chip-Enable Simplify System Decoding
- P-N-P Inputs Reduce Loading on System Buffers/Drivers
- Choice of 3-State or Open-Collector Outputs

4

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES		WRITE CYCLE TIME	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATIONS)	CHIP-SELECT	ADDRESS	SN54S'	SN74S'
SN54S189(J, W)	SN74S189(J, N)	3-State	64 Bits (16 W x 4 B)	12 ns	25 ns	25 ns	25 ns
SN54S289(J, W)	SN74S289(J, N)	Open-Collector					
SN54S201(J, W)	SN74S201(J, N)	3-State	256 Bits (256 W x 1 B)	13 ns	42 ns	100 ns	65 ns
SN54S301(J, W)	SN74S301(J, N)	Open-Collector					
	SN74S209(J, N)	3-State	1024 Bits (1024 W x 1 B)	20 ns	70 ns		150 ns
	SN74S309(J, N)	Open-Collector					

description

These monolithic TTL memories feature Schottky clamping for high performance, a fast chip-select access time to enhance decoding at the system level, and the 'S201 and 'S209 RAMs utilize inverted-cell memory elements to achieve high densities. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor.

A three-state-output version and an open-collector-output version are offered for each of the three organizations. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

write cycle

Information to be stored in the memory is written into the selected address (AD) location when the chip-enable ($\overline{CE}$) and the read/write (R/$\overline{W}$) inputs are low. While the read/write input is low, the memory output(s) is(are) off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the output(s) when the read/write input is high and the chip-enable input(s) is(are) low. When one(or more) chip-enable input is(are) high, the output(s) will be off.

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FUNCTION TABLE

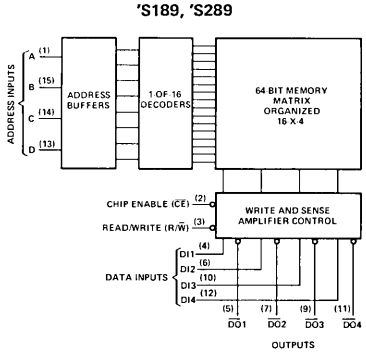
FUNCTION	INPUTS		OUTPUTS			
	CHIP ENABLE†	READ/ WRITE	'S189 'S201	'S289 'S301	SN74S209	SN74S309
Write	L	L	High Impedance	H	High Impedance	H
Read	L	H	Complement of Data Entered	Complement of Data Entered	Data Entered	Data Entered
Inhibit	H	X	High Impedance	H	High Impedance	H

H = high level, L = low level, X = irrelevant

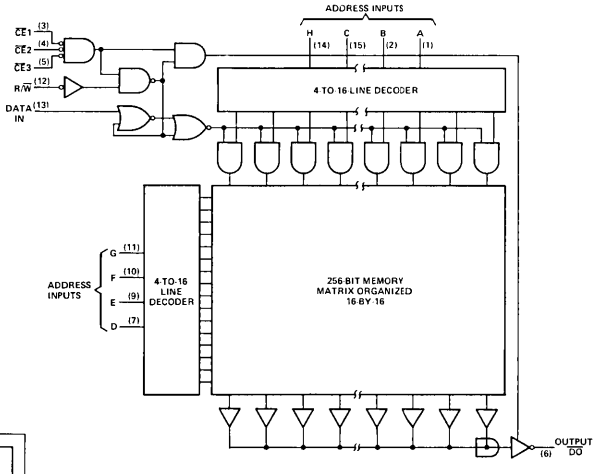
†For chip-enable of 'S201 and 'S301: L = all $\overline{CE}$ inputs low, H = one or more $\overline{CE}$ inputs high.

functional block diagrams

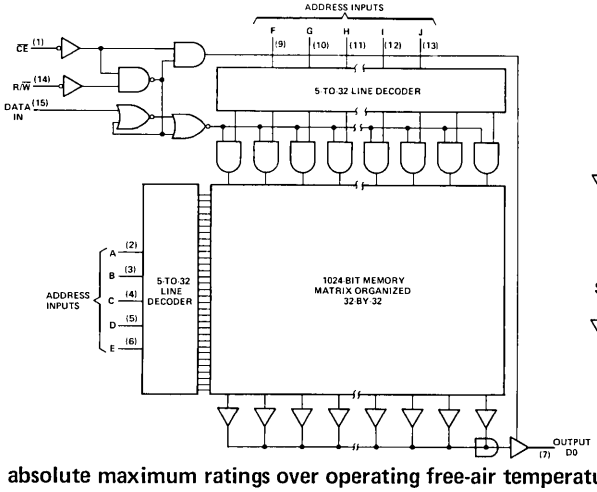
'S189, 'S289



'S201

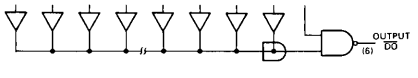


SN74S209



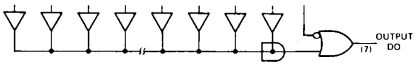
'S301

Same as 'S201 except output is as shown below.



SN74S309

Same as SN74S209 except output is as shown below.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S189			SN74S189			SN54S201			SN74S201			SN74S209			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−6.5			−2			−10.3			−10.3	mA
Low-level output current, I_{OL}				16			16			16			16			16	mA
Width of write pulse, $t_{w(wr)}$ (see Figure 1)		25			25			100			65			130			ns
Setup time (see Figure 1)	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			10↓			ns
	Chip enable before write pulse, $t_{su(\overline{CE})}$	0↓			0↓			0↓			0↓			10↓			
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			100↑			65↑			140↑			
Hold time (see Figure 1)	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			10↑			ns
	Chip enable after write pulse, $t_{h(\overline{CE})}$	0↑			0↑			0↑			0↑			10↑			
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			10↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition of the read/write input used for reference: ↑for the low-to-high-transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S189			'S201			SN74S209			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = ♦					−1.2			−1.2			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		Series 54S'	2.4	3.4		2.4	3.3					V
				Series 74S'	2.4	3.2		2.4	2.9		2.4	2.9		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		Series 54S'		0.35	0.5		0.38	0.5				V
				Series 74S'		0.35	0.45		0.38	0.45		0.38	0.45	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 2.4 V					50			40			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 0.4 V					−50			−40			−100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100	−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Series 54S'	T_A = MAX			110			115				mA
				T_A = 25°C		75	110		100	140				
				T_A = MIN			110			155				
			Series 74S'	Full range		75	110		100	140		110	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
♦I_I = −18 mA for 'S189 and 'S201, −12 mA for 'S209.
NOTE 2: For the 'S189 I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.
For the 'S201 and SN74S209 I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

recommended operating conditions

		SN54S289			SN74S289			SN54S301			SN74S301			SN74S309			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			16			16			16			16	mA
Width of write pulse, $t_{w(wr)}$ (see Figure 1)		25			25			100			65			130			ns
Setup time (see Figure 2)	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			10↓			ns
	Chip enable before write pulse, $t_{su(\overline{CE})}$	0↓			0↓			0↓			0↓			10↓			
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			100↑			65↑			140↑			
Hold time (see Figure 2)	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			10↑			ns
	Chip enable after write pulse, $t_{h(\overline{CE})}$	0↑			0↑			0↑			0↑			10↑			
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			10↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition of the read/write input used for reference: ↑for the low-to-high-transition, ↓for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			'S289			'S301			SN74S309			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = ♦					−1.2			−1.2			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		V_O = 2.4 V			40			40			100	μA
				V_O = 5.5 V			100			100			250	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,		Series 54S'			0.5		0.38	0.5				V
		V_{IL} = 0.8 V, I_{OL} = 16 mA		Series 74S'			0.45		0.38	0.45		0.38	0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	Series 54S'	T_A = MAX			105			110				mA
				T_A = 25°C		75	105		100	140				
				T_A = MIN			105			155				
			Series 74S'	Full range		75	105		100	140		110	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦I_I = −18 mA for 'S289 and 'S301, −12 mA for 'S309.
NOTE 3: For the 'S289 I_{CC} is measured with the read/write and chip-enable inputs grounded, all other inputs at 4.5 V, and the outputs open.
For the 'S301 and SN74S309 I_{CC} is measured with all chip-enable inputs grounded, all other inputs at 4.5 V, and the output open.

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switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

random-access memories with three-state outputs

PARAMETER			TEST CONDITIONS	SN54S189		SN74S189		SN54S201		SN74S201		SN74S209		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{w(wr,min)}$	Minimum width of write pulse		C_L = 30 pF, R_L = 300 Ω, See Figure 1	15	25	15	25	40	100	40	65	65	85	ns
$t_{a(ad)}$	Access time from address			25	50	25	35	42	85	42	65	70	100	ns
$t_{a(\overline{CE})}$	Access time from chip enable (enable time)			12	25	12	17	13	40	13	30	20	40	ns
t_{SR}	Sense recovery time			22	40	22	35	20	50	20	40	20	40	ns
t_{PXZ}	Disable time from high or low level	from $\overline{CE}$	C_L = 5 pF, R_{L1} = 300 Ω, See Figure 1	12	25	12	17	9	30	9	20	15	30	ns
		from R/$\overline{W}$		12		12		13	45	13	35	25	40	

random-access memories with open-collector outputs

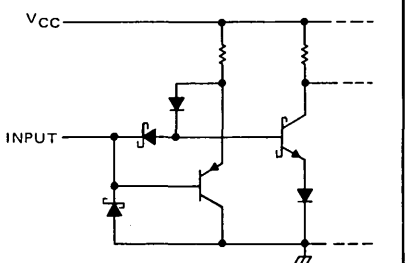
PARAMETER			TEST CONDITIONS	SN54S289		SN74S289		SN54S301		SN74S301		SN74S309		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{w(wr,min)}$	Minimum width of write pulse		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 2	15	25	15	25	40	100	40	65	65	85	ns
$t_{a(ad)}$	Access time from address			25	50	25	35	42	85	42	65	70	100	ns
$t_{a(\overline{CE})}$	Access time from chip enable (enable time)			12	25	12	17	13	40	13	30	20	40	ns
t_{SR}	Sense recovery time			22	40	22	35	20	50	20	40	20	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{CE}$		12	25	12	17	8	30	8	20	15	30	ns
		from R/$\overline{W}$		12		12		15	45	15	35	25	40	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics of inputs and outputs

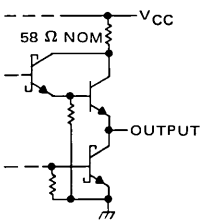
'S189, 'S201, SN74S209, 'S289, 'S301, SN74S309

EQUIVALENT OF EACH INPUT



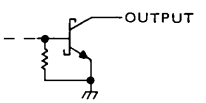
'S189, 'S201, SN74S209

OUTPUT

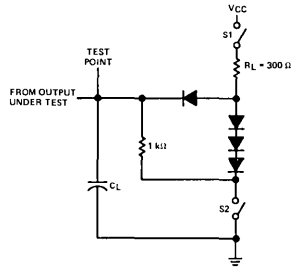


'S289, 'S301, SN74S309

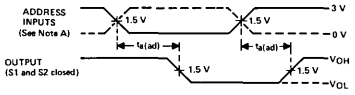
OUTPUT



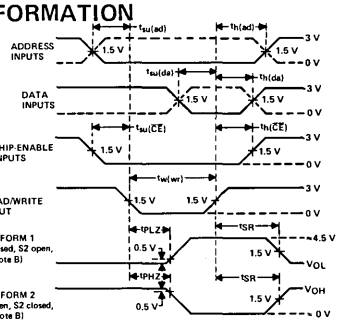
PARAMETER MEASUREMENT INFORMATION



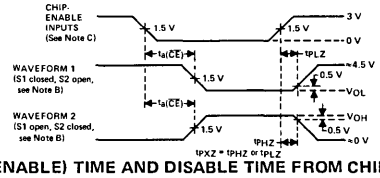
LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



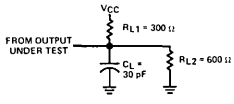
WRITE CYCLE VOLTAGE WAVEFORMS



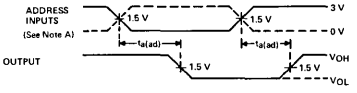
ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip enable input(s) is(are) low and the read/write is high.
B. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
C. When measuring access and disable times from chip enable input(s), the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

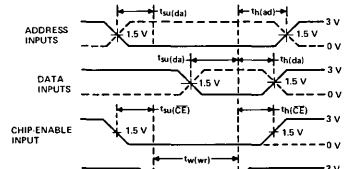
FIGURE 1—TESTING RAM's WITH 3-STATE OUTPUTS



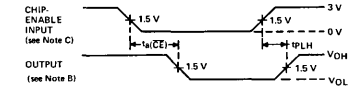
LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



WRITE CYCLE VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-enable input(s) is(are) low and the read/write input is high.
B. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
C. When measuring access and disable times from chip-enable input(s), the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 2—TESTING RAM's WITH OPEN-COLLECTOR OUTPUTS

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