# DATA SHEET

| Part No. | AN49239A |
|---|---|
| Package Code No. | SSOP024-P-0300E |

## Contents

# AN49239A

## Current monitor IC for 3-phase motor

### ■ Overview

AN49239A monitors the current of 3-wire of 3-phase AC power applied to 3-phase motor respectively, using external detection resistors. Then AN49239A amplifies the current, and outputs analog.

Moreover, when the current more than setup value is applied, the detection signal which shows an oversupply is output.

### ■ Features

- High precision current detection function (3 systems)
- Detected value is set by an external resistor (3 systems common)
- Detection signal output (3 systems common)
- The detection values of 3 systems is output by analog individually.
- Analog output gain variable (4 steps)

### ■ Applications

- 3-phase motor for washing machine, air conditioner, etc.

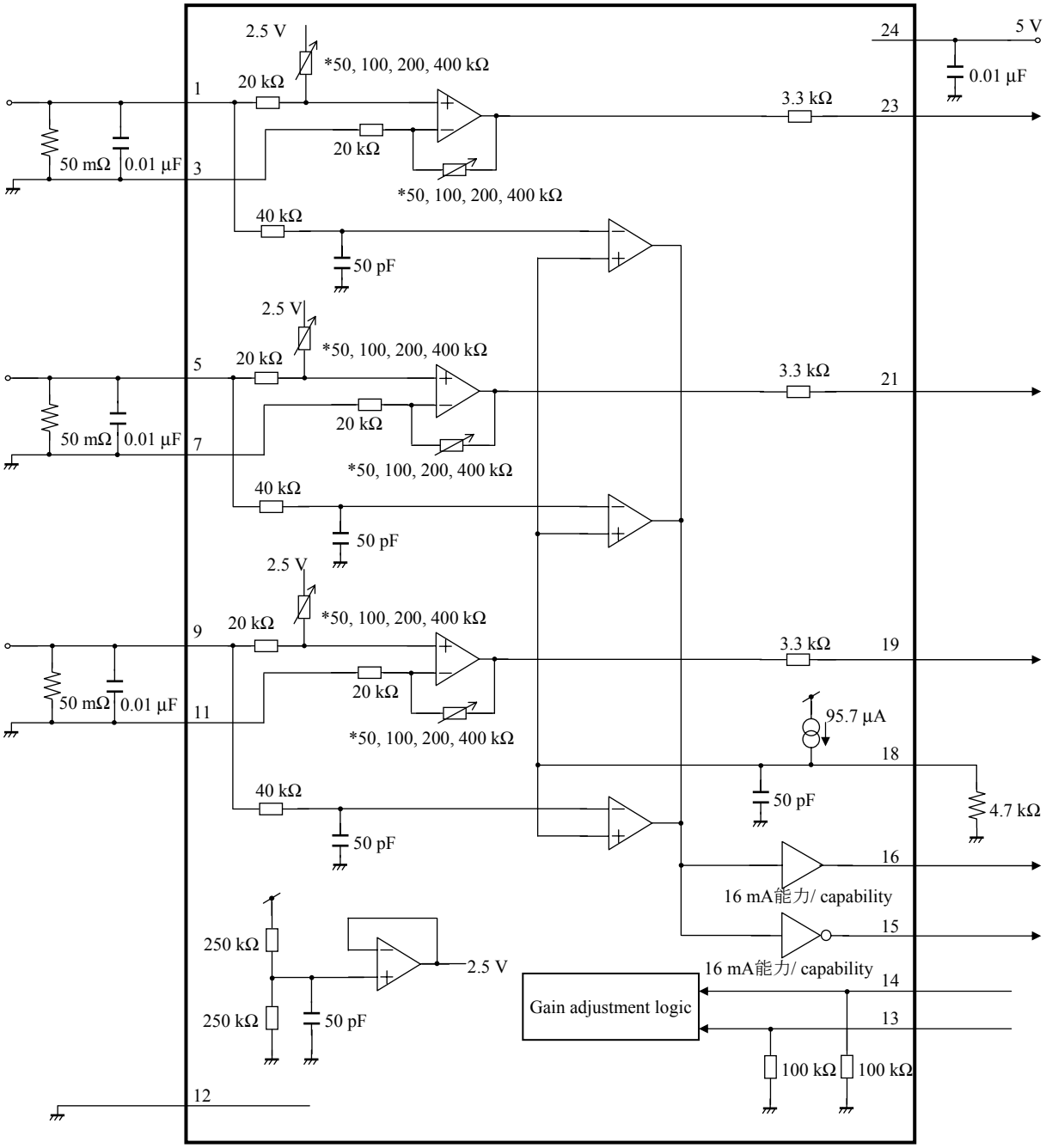
### ■ Package

- 24 pin Plastic Shrink Small Outline Package (SSOP Type)

### ■ Type

- Bi-CMOSIC

■ Application Circuit Example (Block Diagram)




Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

• Use a resistor with an accuracy of ±1% as an external resistor of Pin 18.

• This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

| Pin No. | Pin name | Type | Description |
|---|---|---|---|
| 1 | IU | Input | U-phase input (motor side) |
| 2 | NC | — | No connection |
| 3 | GU | Input | U-phase input (Ground side) |
| 4 | NC | — | No connection |
| 5 | IV | Input | V-phase input (motor side) |
| 6 | NC | — | No connection |
| 7 | GV | Input | V-phase input (Ground side) |
| 8 | NC | — | No connection |
| 9 | IW | Input | W-phase input (motor side) |
| 10 | NC | — | No connection |
| 11 | GW | Input | W-phase input (Ground side) |
| 12 | GND | Ground | Ground pin |
| 13 | VGAIN2 | Input | Analog output gain setting 2 |
| 14 | VGAIN1 | Input | Analog output gain setting 1 |
| 15 | INT | Output | Detection output (positive logic) |
| 16 | NINT | Output | Detection output (negative logic) |
| 17 | NC | — | No connection |
| 18 | VR | Input | Detected value setting |
| 19 | ADIW | Output | W-phase analog output |
| 20 | NC | — | No connection |
| 21 | ADIV | Output | V-phase analog output |
| 22 | NC | — | No connection |
| 23 | ADIU | Output | U-phase analog output |
| 24 | VDD | Power supply | Power supply pin |

## ■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

| A No. | Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|---|
| 1 | Supply voltage | $V_{DD}$ | 6.0 | V | *1 |
| 2 | Supply current | $I_{DD}$ | — | mA | — |
| 3 | Power dissipation | $P_D$ | 156 | mW | *2 |
| 4 | Operating ambient temperature | $T_{opr}$ | –30 to +85 | °C | *3 |
| 5 | Storage temperature | $T_{stg}$ | –55 to +125 | °C | *3 |

Notes) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at $T_a$ = 75°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the $P_D$-$T_a$ diagram in the ■ Technical Data standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $T_a$ = 25°C.

## ■ Operating Supply Voltage Range

| Parameter | Symbol | Range | Unit | Notes |
|---|---|---|---|---|
| Supply voltage range | $V_{DD}$ | 4.5 to 5.5 | V | *1 |

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

## ■ Allowable Current and Voltage Range

Notes) • Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
• Voltage values, unless otherwise specified, are with respect to GND.
• $V_{DD}$ is voltage for VDD.
• Do not apply external currents or voltages to any pin not specifically mentioned.

| Pin No. | Pin name | Rating | Unit | Notes |
|---|---|---|---|---|
| 1 | IU | −1.0 to ($V_{DD}$ + 0.3) | V | *1 |
| 3 | GU | − 0.3 to ($V_{DD}$ + 0.3) | V | *1 |
| 5 | IV | −1.0 to ($V_{DD}$ + 0.3) | V | *1 |
| 7 | GV | − 0.3 to ($V_{DD}$ + 0.3) | V | *1 |
| 9 | IW | −1.0 to ($V_{DD}$ + 0.3) | V | *1 |
| 11 | GW | − 0.3 to ($V_{DD}$ + 0.3) | V | *1 |
| 13 | VGAIN2 | − 0.3 to ($V_{DD}$ + 0.3) | V | *1 |
| 14 | VGAIN1 | − 0.3 to ($V_{DD}$ + 0.3) | V | *1 |
| 18 | VR | − 0.3 to ($V_{DD}$ + 0.3) | V | *1,2 |

Notes) *1: ($V_{DD}$ + 0.3) V must not be exceeded 5.8 V.
*2: Rating when used for input. External voltage or current must not be applied when used for output.

■ Electrical Characteristics at $V_{DD}$ = 5.0 V, GU = 0 V, GV = 0 V, GW = 0 V, VR = 4.7 kΩ

Note) $T_a$ = 25°C±2°C unless otherwise specified.

| B No. | Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| ADIU | | | | | | | | |
| 1 | Output voltage (0 A)<br>5 times gain setting | Vou1 | IU = 0 V,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ – 0.2 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.2 | V | — |
| 2 | Output voltage (3 A)<br>5 times gain setting | Vou2 | IU = 150 mV,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ + 0.55 | 0.5 × $V_{DD}$ + 0.75 | 0.5 × $V_{DD}$ + 0.95 | V | — |
| 3 | Output gain<br>5 times gain setting | DVou1 | DVou1 = (Vou2 – Vou1) / 0.15 | 4.9 | 5.0 | 5.1 | Times | — |
| 4 | Output voltage (0 A)<br>10 times gain setting | Vou3 | IU = 0 V,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ – 0.4 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.4 | V | — |
| 5 | Output voltage (3.52 A)<br>10 times gain setting | Vou4 | IU = 176 mV,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 5 V | $V_{DD}$ – 1.14 | $V_{DD}$ – 0.74 | $V_{DD}$ – 0.34 | V | — |
| 6 | Output gain<br>10 times gain setting | DVou2 | DVou2 = (Vou4 – Vou3) / 0.176 | 9.9 | 10.0 | 10.1 | Times | — |
| 7 | Output voltage (0 A)<br>2.5 times gain setting | Vou5 | IU = 0 V,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ – 0.2 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.2 | V | — |
| 8 | Output voltage (–15.68 A)<br>2.5 times gain setting | Vou6 | IU = –784 mV,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 0 V | 0.34 | 0.54 | 0.74 | V | — |
| 9 | Output gain<br>2.5 times gain setting | DVou3 | DVou3 = (Vou5 – Vou6) / 0.784 | 2.4 | 2.5 | 2.6 | Times | — |
| 10 | Output voltage (0 A)<br>20 times gain setting | Vou7 | IU = 0 V,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ – 0.8 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.8 | V | — |
| 11 | Output voltage (1 A)<br>20 times gain setting | Vou8 | IU = 50 mV,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ + 0.2 | 0.5 × $V_{DD}$ + 1.0 | 0.5 × $V_{DD}$ + 1.8 | V | — |
| 12 | Output gain<br>20 times gain setting | DVou4 | DVou4 = (Vou8 – Vou7) / 0.05 | 19.8 | 20.0 | 20.2 | Times | — |

■ Electrical Characteristics (continued) at $V_{DD}$ = 5.0 V, GU = 0 V, GV = 0 V, GW = 0 V, VR = 4.7 kΩ

Note) $T_a$ = 25°C±2°C unless otherwise specified.

| B No. | Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| ADIV | | | | | | | | |
| 13 | Output voltage (0 A)<br>5 times gain setting | Vov1 | IV = 0 V,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ – 0.2 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.2 | V | — |
| 14 | Output voltage (3 A)<br>5 times gain setting | Vov2 | IV = 150 mV,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ + 0.55 | 0.5 × $V_{DD}$ + 0.75 | 0.5 × $V_{DD}$ + 0.95 | V | — |
| 15 | Output gain<br>5 times gain setting | DVov1 | DVov1 = (Vov2 – Vov1) / 0.15 | 4.9 | 5.0 | 5.1 | Times | — |
| 16 | Output voltage (0 A)<br>10 times gain setting | Vov3 | IV = 0 V,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ – 0.4 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.4 | V | — |
| 17 | Output voltage (3.52 A)<br>10 times gain setting | Vov4 | IV = 176 mV,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 5 V | $V_{DD}$ – 1.14 | $V_{DD}$ – 0.74 | $V_{DD}$ – 0.34 | V | — |
| 18 | Output gain<br>10 times gain setting | DVov2 | DVov2 = (Vov4 – Vov3) / 0.176 | 9.9 | 10.0 | 10.1 | Times | — |
| 19 | Output voltage (0 A)<br>2.5 times gain setting | Vov5 | IV = 0 V,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ – 0.2 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.2 | V | — |
| 20 | Output voltage (–15.68 A)<br>2.5 times gain setting | Vov6 | IV = –784 mV,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 0 V | 0.34 | 0.54 | 0.74 | V | — |
| 21 | Output gain<br>2.5 times gain setting | DVov3 | DVov3 = (Vov5 – Vov6) / 0.784 | 2.4 | 2.5 | 2.6 | Times | — |
| 22 | Output voltage (0 A)<br>20 times gain setting | Vov7 | IV = 0 V,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ – 0.8 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.8 | V | — |
| 23 | Output voltage (1 A)<br>20 times gain setting | Vov8 | IV = 50 mV,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ + 0.2 | 0.5 × $V_{DD}$ + 1.0 | 0.5 × $V_{DD}$ + 1.8 | V | — |
| 24 | Output gain<br>20 times gain setting | DVov4 | DVov4 = (Vov8 – Vov7) / 0.05 | 19.8 | 20.0 | 20.2 | Times | — |

■ Electrical Characteristics (continued) at $V_{DD}$ = 5.0 V, GU = 0 V, GV = 0 V, GW = 0 V, VR = 4.7 kΩ

Note) $T_a$ = 25°C±2°C unless otherwise specified.

| B No. | Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| ADIW | | | | | | | | |
| 25 | Output voltage (0 A)<br>5 times gain setting | Vow1 | IW = 0 V,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ – 0.2 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.2 | V | — |
| 26 | Output voltage (3 A)<br>5 times gain setting | Vow2 | IW = 150 mV,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ + 0.55 | 0.5 × $V_{DD}$ + 0.75 | 0.5 × $V_{DD}$ + 0.95 | V | — |
| 27 | Output gain<br>5 times gain setting | DVow1 | DVow1 = (Vow2 – Vow1) / 0.15 | 4.9 | 5.0 | 5.1 | Times | — |
| 28 | Output voltage (0 A)<br>10 times gain setting | Vow3 | IW = 0 V,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ – 0.4 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.4 | V | — |
| 29 | Output voltage (3.52 A)<br>10 times gain setting | Vow4 | IW = 176 mV,<br>$V_{GAIN1}$ = 0 V, $V_{GAIN2}$ = 5 V | $V_{DD}$ – 1.14 | $V_{DD}$ – 0.74 | $V_{DD}$ – 0.34 | V | — |
| 30 | Output gain<br>10 times gain setting | DVow2 | DVow2 = (Vow4 – Vow3) / 0.176 | 9.9 | 10.0 | 10.1 | Times | — |
| 31 | Output voltage (0 A)<br>2.5 times gain setting | Vow5 | IW = 0 V,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 0 V | 0.5 × $V_{DD}$ – 0.2 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.2 | V | — |
| 32 | Output voltage (–15.68 A)<br>2.5 times gain setting | Vow6 | IW = –784 mV,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 0 V | 0.34 | 0.54 | 0.74 | V | — |
| 33 | Output gain<br>2.5 times gain setting | DVow3 | DVow3 = (Vow5 – Vow6) / 0.784 | 2.4 | 2.5 | 2.6 | Times | — |
| 34 | Output voltage (0 A)<br>20 times gain setting | Vow7 | IW = 0 V,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ – 0.8 | 0.5 × $V_{DD}$ | 0.5 × $V_{DD}$ + 0.8 | V | — |
| 35 | Output voltage (1 A)<br>20 times gain setting | Vow8 | IW = 50 mV,<br>$V_{GAIN1}$ = 5 V, $V_{GAIN2}$ = 5 V | 0.5 × $V_{DD}$ + 0.2 | 0.5 × $V_{DD}$ + 1.0 | 0.5 × $V_{DD}$ + 1.8 | V | — |
| 36 | Output gain<br>20 times gain setting | DVow4 | DVow4 = (Vow8 – Vow7) / 0.05 | 19.8 | 20.0 | 20.2 | Times | — |

■ Electrical Characteristics (continued) at $V_{DD}$ = 5.0 V, GU = 0 V, GV = 0 V, GW = 0 V, VR = 4.7 kΩ

Note) $T_a$ = 25°C±2°C unless otherwise specified.

| B No. | Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| IU | | | | | | | | |
| 37 | Over-current detection voltage: U-phase | IRQU | NINT = High → Low | 430 | 450 | 470 | mV | — |
| 38 | Over-current detection output time: U-phase | TRQU | IIN = 0 V → $V_{DD}$, $V_R$ = 1 V, Arrival time to INT = $V_{DD}$ × 0.8 V | — | — | 3 | µs | — |
| IV | | | | | | | | |
| 39 | Over-current detection voltage: V-phase | IRQV | NINT = High → Low | 430 | 450 | 470 | mV | — |
| 40 | Over-current detection output time: V-phase | TRQV | IIN = 0 V → $V_{DD}$, $V_R$ = 1 V, Arrival time to INT = $V_{DD}$ × 0.8 V | — | — | 3 | µs | — |
| IW | | | | | | | | |
| 41 | Over-current detection voltage: W-phase | IRQU | NINT = High → Low | 430 | 450 | 470 | mV | — |
| 42 | Over-current detection output time: W-phase | TRQU | IIN = 0 V → $V_{DD}$, $V_R$ = 1 V, Arrival time to INT = $V_{DD}$ × 0.8 V | — | — | 3 | µs | — |
| VR | | | | | | | | |
| 43 | Reference detection voltage | VVR | VR = 4.7 kΩ | 440 | 450 | 460 | mV | — |
| INT | | | | | | | | |
| 44 | Detection output High-level | VOH | IU > 470 mV, IIN = –16 mA | $V_{DD}$ × 0.8 | — | — | V | — |
| 45 | Detection output Low-level | VOL | IU < 430 mV, IIN = +16 mA | — | — | $V_{DD}$ × 0.2 | V | — |
| NINT | | | | | | | | |
| 46 | Detection output High-level | VOHN | IU < 430 mV, IIN = –16 mA | $V_{DD}$ × 0.8 | — | — | V | — |
| 47 | Detection output Low-level | VOLN | IU > 470 mV, IIN = +16 mA | — | — | $V_{DD}$ × 0.2 | V | — |

■ Electrical Characteristics (continued) at $V_{DD}$ = 5.0 V, GU = 0 V, GV = 0 V, GW = 0 V, VR = 4.7 kΩ

Note) $T_a$ = 25°C±2°C unless otherwise specified.

| B No. | Parameter | Symbol | Conditions | Limits | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| VGAIN1 | | | | | | | | |
| 48 | Input current | IIG1 | VIN = 5 V | 25 | 50 | 100 | µA | — |
| 49 | Input High-level | VIH1 | — | $V_{DD}$ × 0.7 | — | — | V | — |
| 50 | Input Low-level | VIL1 | — | — | — | $V_{DD}$ × 0.3 | V | — |
| VGAIN2 | | | | | | | | |
| 51 | Input current | IIG1 | VIN = 5 V | 25 | 50 | 100 | µA | — |
| 52 | Input High-level | VIH1 | — | $V_{DD}$ × 0.7 | — | — | V | — |
| 53 | Input Low-level | VIL1 | — | — | — | $V_{DD}$ × 0.3 | V | — |
| Circuit current | | | | | | | | |
| 54 | Circuit current | IDD | — | — | 1.5 | 5.0 | mA | — |

## ■ Control Pin Mode Table

Note) See parameters B No. 49, B No. 50, B No.52, B No.53 in the Electrical Characteristics for control voltage retention ranges.

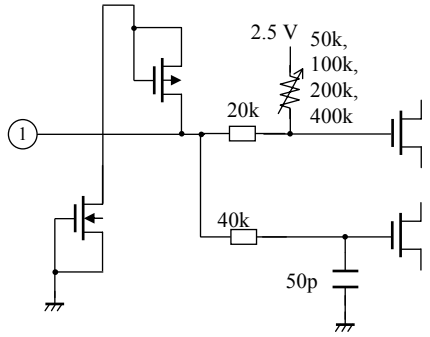
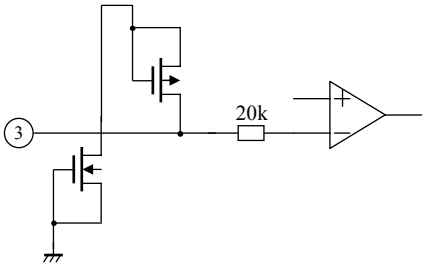
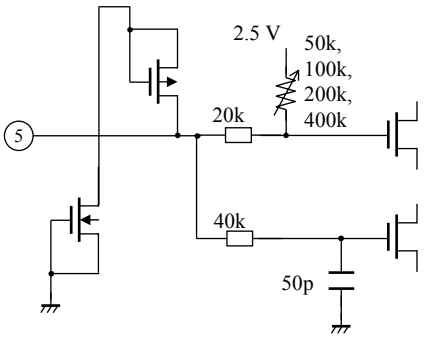
| Pin No. | Description | Pin voltage | | Remarks |
|---|---|---|---|---|
| | | Low | High | |
| 13 | VGAIN2 | GAIN Low | GAIN High | The gain levels of ADIU, ADIV and ADIW are set.<br>These gain values are set by VGAIN1. |
| 14 | VGAIN1 | Normal Gain | Extra Gain | Normal Gain is set to 5 times or 10 times by GAIN2.<br>Extra Gain is set to 2.5 times or 20 times by GAIN2. |

2.5 times gain : VGAIN1 = High, VGAIN2 = Low
5 times gain : VGAIN1 = Low, VGAIN2 = Low
10 times gain : VGAIN1 = Low, VGAIN2 = High
20 times gain : VGAIN1 = High, VGAIN2 = High

## ■ Technical Data

• I/O block circuit diagrams and pin function descriptions

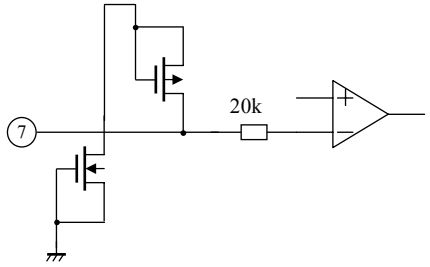
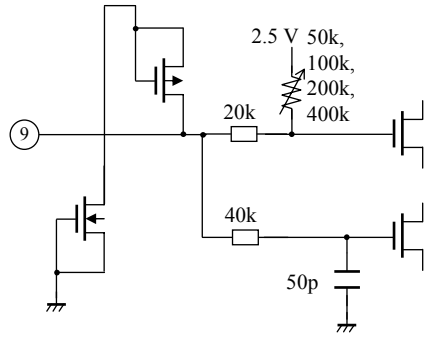
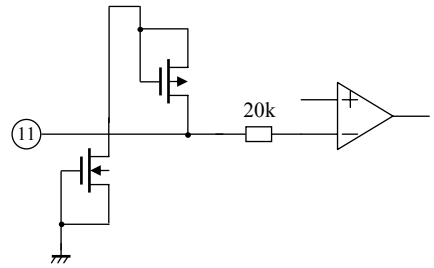
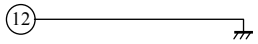
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

| Pin No. | Waveform and voltage | Internal circuit | Impedance | Description |
|---|---|---|---|---|
| 1 | AC |  | — | Pin name: IU<br>U-phase input (motor side) |
| 2 | — | — | — | Pin name: N.C.<br>No connection |
| 3 | AC |  | — | Pin name: GU<br>U-phase input (Ground side) |
| 4 | — | — | — | Pin name: N.C.<br>No connection |
| 5 | AC |  | — | Pin name: IV<br>V-phase input (motor side) |
| 6 | — | — | — | Pin name: N.C.<br>No connection |

■ Technical Data (continued)

• I/O block circuit diagrams and pin function descriptions (continued)

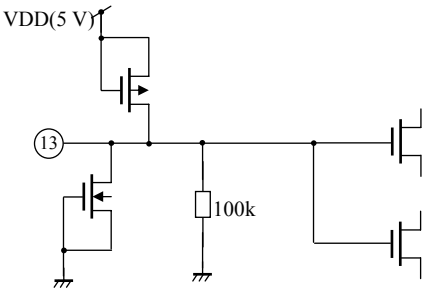
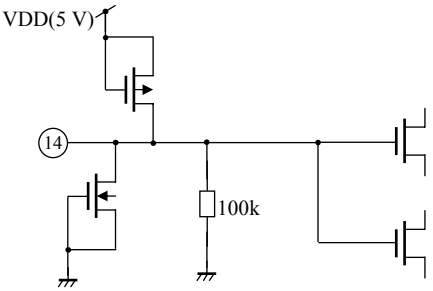
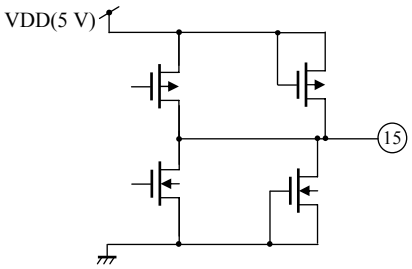
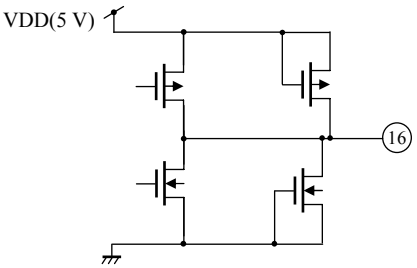
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

| Pin No. | Waveform and voltage | Internal circuit | Impedance | Description |
|---|---|---|---|---|
| 7 | AC |  | — | Pin name: GV<br>V-phase input (Ground side) |
| 8 | — | — | — | Pin name: N.C.<br>No connection |
| 9 | AC |  | — | Pin name: IW<br>W-phase input (motor side) |
| 10 | — | — | — | Pin name: N.C.<br>No connection |
| 11 | AC |  | — | Pin name : GW<br>W-phase input (Ground side) |
| 12 | DC (0 V) |  | — | Pin name: GND<br>Ground pin |

■ Technical Data (continued)

• I/O block circuit diagrams and pin function descriptions (continued)

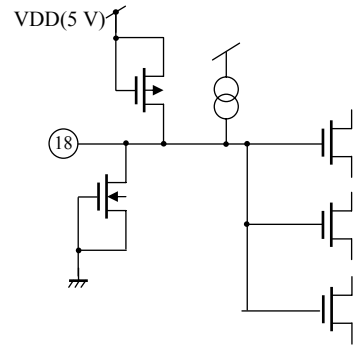
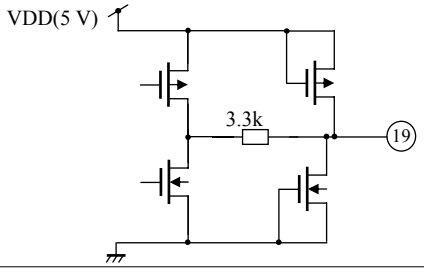
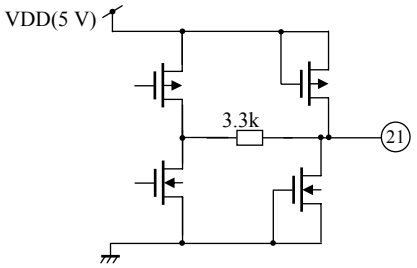
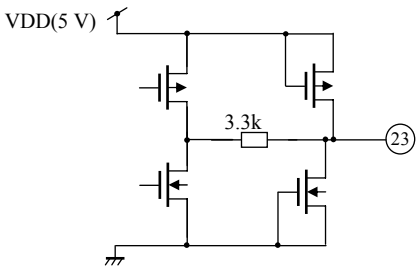
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

| Pin No. | Waveform and voltage | Internal circuit | Impedance | Description |
|---|---|---|---|---|
| 13 | DC |  | — | Pin name: VGAIN2<br>Analog output gain setting 2 |
| 14 | DC |  | — | Pin name: VGAIN1<br>Analog output gain setting 1 |
| 15 | DC |  | — | Pin name: INT<br>Detection output (positive logic) |
| 16 | DC |  | — | Pin name: NINT<br>Detection output (negative logic) |
| 17 | — | — | — | Pin name: N.C.<br>No connection |

■ Technical Data (continued)

• I/O block circuit diagrams and pin function descriptions (continued)

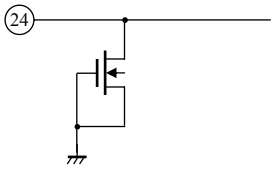
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

| Pin No. | Waveform and voltage | Internal circuit | Impedance | Description |
|---|---|---|---|---|
| 18 | DC |  | — | Pin name: VR<br>Detected value setting |
| 19 | DC |  | — | Pin name: ADIW<br>W-phase analog output |
| 20 | — | — | — | Pin name: N.C.<br>No connection |
| 21 | DC |  | — | Pin name: ADIV<br>V-phase analog output |
| 22 | — | — | — | Pin name: N.C.<br>No connection |
| 23 | DC |  | — | Pin name: ADIU<br>U-phase analog output |

■ Technical Data (continued)

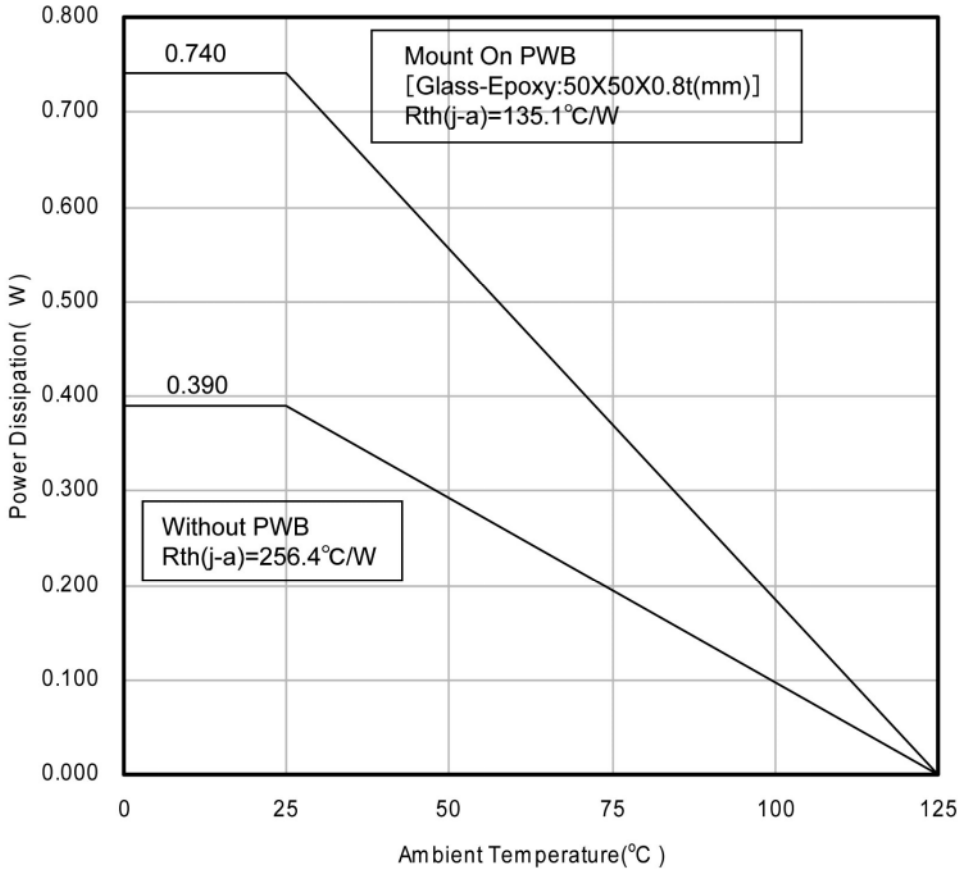
• I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

| Pin No. | Waveform and voltage | Internal circuit | Impedance | Description |
|---|---|---|---|---|
| 24 | DC (Typ. 5.0 V) |   | — | Pin name: VDD<br>Power supply pin |

■ Technical Data (continued)

• $P_D$ — $T_a$ diagram



## ■ Usage Notes

•Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [3-phase motor].
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.

   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-$V_{CC}$ short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment. Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

7. When using the LSI for new models, verify the safety including the long-term reliability for each product.

8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

## Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.



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