

EiceDRIVER^(TM)

2ED020112-F

Dual Channel IGBT Driver IC

<http://www.infineon.com/gatedriver>

Power Management & Drives



N e v e r s t o p t h i n k i n g

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2ED020112-F**Confidential****Revision History: 2006-05**

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Table of Contents		Page
1	Overview.....	5
	1.1 Coreless transformer (CLT) technology.....	5
2	Pin configuration and package outline	7
3	Block diagram.....	8
4	Functional description	9
	4.1 Power supply.....	9
	4.2 Logic inputs	9
	4.3 Gate driver.....	9
	4.4 General purpose operational amplifier.....	9
	4.5 General purpose comparator	9
	4.6 CLT.....	9
	4.7 EMI.....	9
5	Electrical parameters.....	10
	5.1 Absolute maximum ratings.....	10
	5.2 Operating range	11
	5.3 Electrical characteristics.....	11
	5.3.1 Voltage Supply.....	11
	5.3.2 Logic inputs.....	12
	5.3.3 Gate drivers	12
	5.3.4 Dynamic characteristics.....	12
	5.3.5 General purpose operational amplifier.....	13
	5.3.6 General purpose comparator.....	13
6	Diagrams	14

1 Overview

The 2ED020112-F is a high voltage, high speed power IGBT and MOSFET driver of the Infineon *EiceDRIVER*[™] family with interlocking high and low side referenced output channels. The floating high side driver may be supplied directly or by means of a bootstrap diode and capacitor. All logic inputs are compatible with 3.3 V and 5 V TTL. Additionally the 2ED020112-F is equipped with a dedicated shutdown input. The drivers feature a high pulse current buffer stage. Propagation delays are matched to simplify use in high frequency applications. Both drivers are designed to drive an n-channel power IGBT or MOSFET which operates up to 1200 V. In addition, a general purpose operational amplifier and a general purpose comparator are provided, which may be used e.g. for current measurement or over current detection.

Product Highlights

- Fully operational to ± 1200 V
- Floating high side driver
- Gate drive supply range from 13 to 18 V
- Gate drive currents of +1 A / -2 A
- Matched propagation delay for both channels
- High dV/dt immunity
- General purpose operational amplifier
- General purpose comparator

Features

- Under-voltage lockout for both channels
- 3.3 V and 5 V TTL compatible inputs
- CMOS Schmitt-triggered inputs with internal pull-down
- CMOS Schmitt-triggered shutdown with internal pull-up
- Non-inverting inputs
- Interlocking inputs
- Dedicated shutdown input with internal pull-up
- UL recognized (pending)



1.1 Coreless transformer (CLT) technology

The coreless transformer technology combines almost all advantages of optocouplers, level-shifters, and discrete transformers by avoiding at the same time almost all disadvantages of these devices by a very cost efficient way and high voltage isolation capability.

The principle function of the CLT is realized by two coils which are compounded on silicon within one integrated circuit. The isolation between these coils together with the used package dimensions makes this device suitable for 1200 V applications and provides a functional isolation. **Figure 1** shows a schematic of the internal stages of the IC.

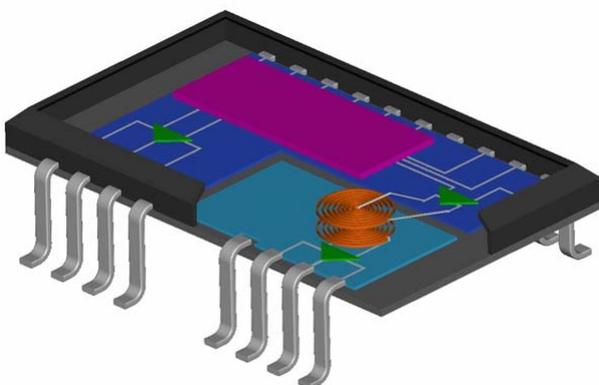
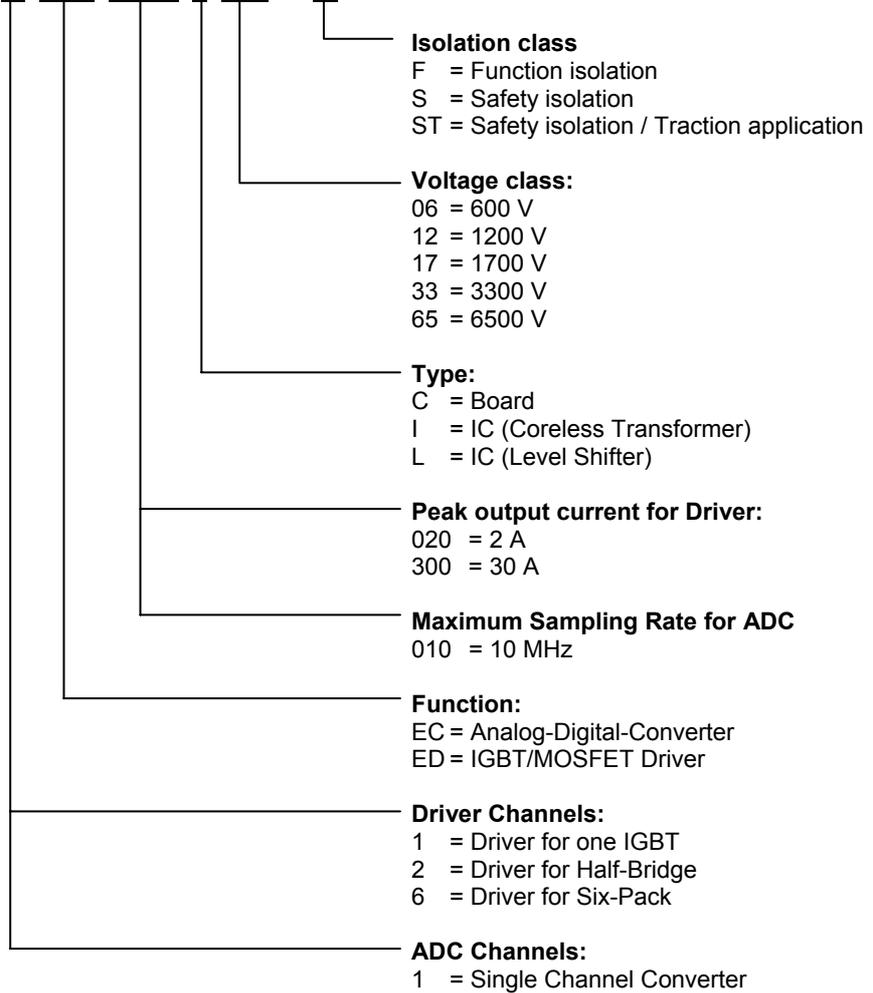


Figure 1 IC schematic

Each *EiceDRIVER*™ has a type number, which can be resolved by the following schemata:

***EiceDRIVER*™ 2 ED 020 I 12 - F**



2 Pin configuration and package outline

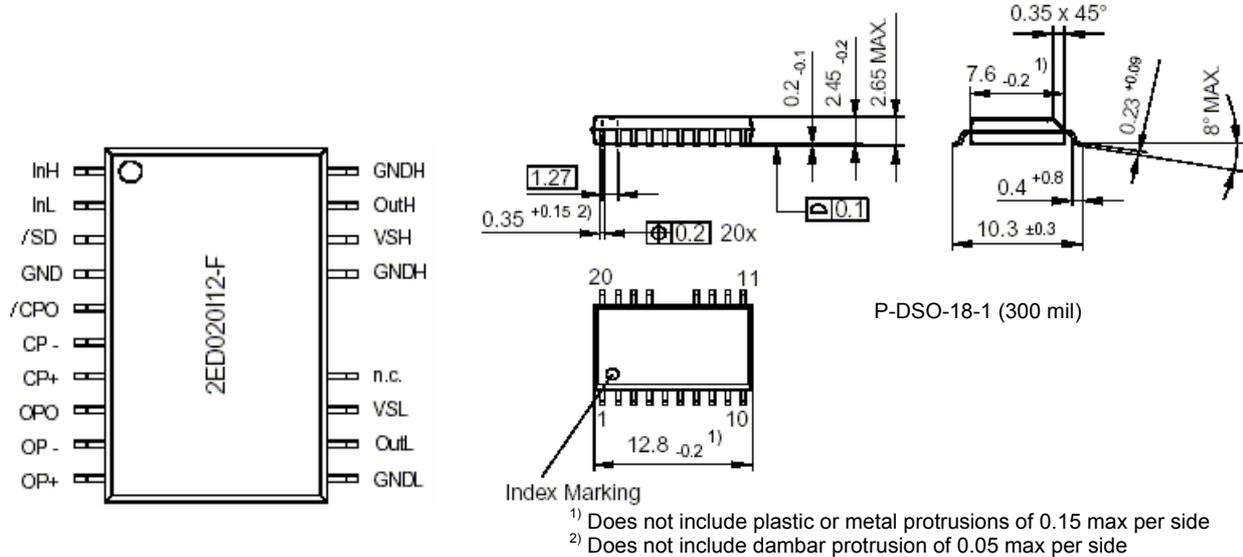


Figure 2 Pin configuration (top view)

Figure 3 Package outline (all measures in mm)

Pin	Symbol	Function
1	InH	Logic input for high side driver
2	InL	Logic input for low side driver
3	/SD	Logic input for shutdown of both drivers
4	GND	Common ground
5	/CPO	Open drain output of general purpose comparator
6	CP-	Inverting input of general purpose comparator
7	CP+	Non-inverting input of general purpose comparator
8	OPO	Output of general purpose operational amplifier
9	OP-	Inverting input of general purpose operational amplifier
10	OP+	Non-inverting input of general purpose operational amplifier
11	GNDL	Low side supply ground
12	OutL	Low side gate driver output
13	VSL	Low side supply voltage
14	n.c.	(not connected)
15	n.e.	(not existing)
16	n.e.	(not existing)
17	GNDH	High side supply ground
18	VSH	High side supply voltage
19	OutH	High side gate driver output
20	GNDH	High side supply ground

3 Block diagram

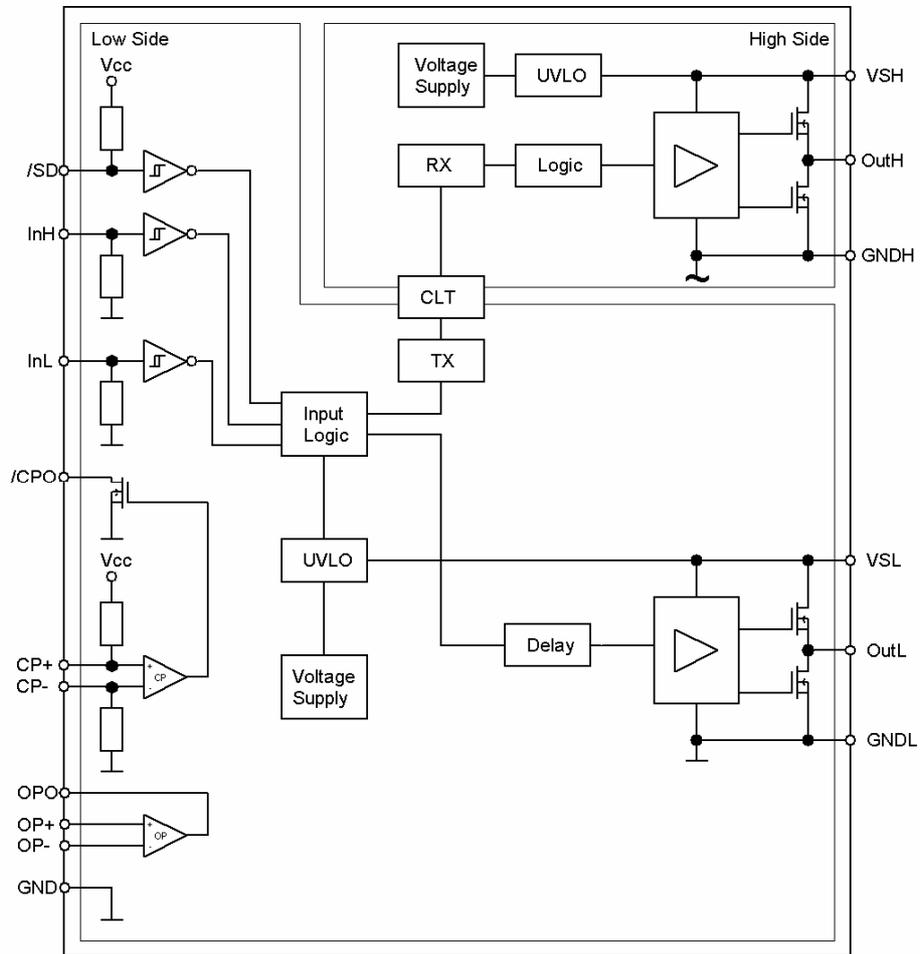


Figure 4 Block diagram

4 Functional description

4.1 Power supply

The power supply of both sides, VSL and VSH, is monitored by an under-voltage lockout block (UVLO) which enables operation of the corresponding side when the supply voltage reaches the “on” threshold of 12 V. Afterwards the internal voltage reference and the biasing circuit are enabled. When the supply voltage (VSL, VSH) drops below the “off” threshold of 11 V the circuit is disabled.

4.2 Logic inputs

The logic inputs InH, InL (non-inverting) and /SD (inverting) are fed into Schmitt-Triggers with thresholds compatible to 3.3 V and 5 V TTL. When /SD is enabled (low), inputs InH and InL are disabled. If InH is high while InL is low, OutH is enabled and vice versa. However, if both signals are high, they are internally disabled until both signals get low again. This is due to the interlocking logic of the device (see also Figure 5).

4.3 Gate driver

2ED020112-F features two hard-switching gate drivers with n-channel output stages capable to source 1 A and to sink 2 A peak current. Both drivers are equipped with active-low-clamping capability. Furthermore, they feature a large ground bounce ruggedness in order to compensate ground bounces caused by a turn-off of the driven IGBT or MOSEFT.

4.4 General purpose operational amplifier

The integrated general purpose operational amplifier can be applied for current measurement of the driven low-side IGBT or MOSFET. The OP is equipped with a -0.1 V to 2 V input stage and a rail-to-rail output stage which is capable to drive ± 5 mA and is dedicated to drive for instance an A/D converter. The OP needs for stable operation a minimum gain of 3 set by the external circuitry.

4.5 General purpose comparator

The integrated general purpose comparator can be applied for over-current detection of the low side IGBT or MOSFET. A dedicated offset as well as a pull-up and pull-down resistor have been introduced to its inputs for security reasons.

4.6 CLT

In order to enable signal transmission across the isolation barrier between low-side and high-side driver, a coreless transformer is employed. Signals, that are to be transmitted, are specially encoded by the transmitter and correspondingly reconstructed by the receiver. In this way EMI due to variations of GNDH (dV_{GNDH}/dt) or the magnetic flux density (dH/dt) can be suppressed. To compensate the additional propagation delay of transmitter, coreless transformer and receiver, a dedicated propagation delay is introduced into the low-side driver which assures a maximum difference of the propagation delay times of 10 ns.

4.7 EMI

The driver was tested according to IEC 61000-4-4 Level 3 (typical industrial environment) in an Infineon reference frequency converter.

5 Electrical parameters

5.1 Absolute maximum ratings

Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND. The pins GND and GNDL have to be connected externally through the shortest possible way.

Parameter	Symbol	Limit values		Unit	Remark
		min.	max.		
High side ground	V_{GNDH}	-1200	1200	V	
High side supply voltage	V_{VSH}	-0.3	20	V	¹⁾
High side gate driver output	V_{OutH}	-0.3	$V_{\text{VSH}} + 0.3$	V	¹⁾
Low side ground	V_{GNDL}	-0.3	5.3	V	
Low side supply voltage	V_{VSL}	-0.3	20	V	²⁾
Low side gate driver output	V_{OutL}	-0.3	$V_{\text{VSL}} + 0.3$	V	³⁾
Logic input voltages (InH, InL, /SD)	V_{In}	-0.3	5.3	V	
OP input voltages (OP-, OP+)	V_{OP}	-0.3	5.3	V	⁴⁾
OP output voltage	V_{OPO}	-0.3	5.3	V	
CP input voltages (CP-, CP+)	V_{CP}	-0.3	5.3	V	⁴⁾
CP output voltage	V_{CPO}	-0.3	5.3	V	
CP output max. sink current	I_{CPO}	—	5	mA	
High side ground, voltage transient	dV_{GNDH}/dt	-50	50	V/ns	
Package power dissipation @ $T_{\text{A}}=25^{\circ}\text{C}$	P_{D}	—	2	W	⁵⁾
Thermal resistance (both chips active), junction to ambient	R_{THJA}	—	60	K/W	⁶⁾
Thermal resistance (high side chip), junction to ambient	$R_{\text{THJA(HS)}}$	—	110	K/W	⁶⁾
Thermal resistance (low side chip), junction to ambient	$R_{\text{THJA(LS)}}$	—	110	K/W	⁶⁾
Junction temperature	T_{J}	—	150	$^{\circ}\text{C}$	
Storage temperature	T_{S}	-55	150	$^{\circ}\text{C}$	

¹⁾ with reference to high side GNDH

²⁾ with reference to both GND and GNDL

³⁾ with reference to low side ground GNDL

⁴⁾ please note the different specifications for the operating range

⁵⁾ considering $R_{\text{THJA}} = 60 \text{ K/W}$, e.g. both chips active

⁶⁾ device soldered to reference PCB without cooling area

5.2 Operating range

Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND.

Parameter	Symbol	Limit values		Unit	Remark
		min.	max.		
High side ground	V_{GNDH}	-1200	1200	V	
High side supply voltage	V_{VSH}	13	18	V	¹⁾
Low side supply voltage	V_{VSL}	13	18	V	²⁾
Logic input voltages (InH, InL, /SD)	V_{In}	0	5	V	
OP input voltages (OP-, OP+)	V_{OP}	-0.1	2	V	
CP input voltages (CP-, CP+)	V_{CP}	-0.1	2	V	
Switching frequency	f_{S}	0	tbd	kHz	
Ambient temperature	T_{A}	-40	105	°C	

¹⁾ with reference to high side ground GNDH

²⁾ with reference to both GND and GNDL

5.3 Electrical characteristics

The electrical characteristics involve the spread of values for the supply voltages, load and junction temperature given below. Typical values represent the median values which are related to production processes. Unless otherwise noted all voltages are given with respect to ground (GND).

$V_{\text{VSL}} = 15 \text{ V}$, $V_{\text{VSH}} = 15 \text{ V}^{1)}$, $C_{\text{L}} = 1 \text{ nF}$, $T_{\text{A}} = 25^\circ\text{C}$. Positive currents are assumed to be flowing into pins.

5.3.1 Voltage Supply

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
High side leakage current	I_{GNDH}	—	0	—	μA	$V_{\text{GNDH}} = 1.2 \text{ kV}$ $V_{\text{GNDL}} = 0 \text{ V}$
High side quiescent supply current	I_{VSH}	—	2.4	3.2	mA	$V_{\text{VSH}} = 15 \text{ V}^{1)}$
High side under-voltage lockout, upper threshold	$V_{\text{VSH}}^{1)}$	10.9	12.2	13.5	V	
High side under-voltage lockout lower threshold	$V_{\text{VSH}}^{1)}$	—	11.2	—	V	
High side under-voltage lockout hysteresis	ΔV_{VSH}	0.7	1	1.3		
Low side quiescent supply current	I_{VSL}	—	2.4	3.2	mA	$V_{\text{VSL}} = 15 \text{ V}$
Low side under-voltage lockout, upper threshold	V_{VSL}	10.7	12	13.3	V	
Low side under-voltage lockout lower threshold	V_{VSL}	—	11	—	V	
Low side under-voltage lockout hysteresis	ΔV_{VSL}	0.7	1	1.3		

¹⁾ with reference to high side ground GNDH

5.3.2 Logic inputs

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
Logic "1" input voltages (InH, InL, /SD)	V_{In}	2	—	—	V	
Logic "0" input voltages (InH, InL, /SD)	V_{In}	—	—	0.8	V	
Logic "1" input current (InH, InL)	I_{In}	—	40	60	μA	$V_{In} = 5\text{ V}$
Logic "0" input current (InH, InL)	I_{In}	—	0	—	μA	$V_{In} = 0\text{ V}$
Logic "1" input current (/SD)	I_{In}	—	0	—	μA	$V_{In} = 5\text{ V}$
Logic "0" input current (/SD)	I_{In}	-60	-40	—	μA	$V_{In} = 0\text{ V}$

5.3.3 Gate drivers

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
High side high level output voltage	$V_{VSH} - V_{OutH}$	—	1.4	1.7	V	$I_{OutH} = -1\text{ mA}$ $V_{InH} = 5\text{ V}$
High side low level output voltage	$V_{OutH}^{1)}$	—	—	0.1	V	$I_{OutH} = 1\text{ mA}$ $V_{InH} = 0\text{ V}$
Low side high level output voltage	$V_{VSL} - V_{OutL}$	—	1.4	1.7	V	$I_{OutH} = -1\text{ mA}$ $V_{InH} = 0\text{ V}$
Low side low level output voltage	V_{OutL}	—	—	0.1	V	$I_{OutH} = 1\text{ mA}$ $V_{InH} = 0\text{ V}$
Output high peak current (OutL, OutH)	I_{Out}	—	—	-1	A	$V_{In} = 5\text{ V}$ $V_{Out} = 0\text{ V}$
Output low peak current (OutL, OutH)	I_{Out}	2	—	—	A	$V_{In} = 0\text{ V}$ $V_{Out} = 15\text{ V}$
High side active low clamping	$V_{OutH}^{1)}$	—	—	3	V	$V_{InH} = 0\text{ V}$ VSH open $I_{OutH} = 200\text{ mA}$
Low side active low clamping	V_{OutL}	—	—	3	V	$V_{InL} = 0\text{ V}$ VSL open $I_{OutL} = 200\text{ mA}$

¹⁾ with reference to high side ground GNDH

5.3.4 Dynamic characteristics

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
Turn-on propagation delay	t_{on}	—	55	tbd	ns	ref. to Figure 6
Turn-off propagation delay	t_{off}	—	55	tbd	ns	ref. to Figure 6
Shutdown propagation delay	$t_{/SD}$	—	55	tbd	ns	ref. to Figure 7
Turn-on rise time	t_r	—	40	tbd	ns	ref. to Figure 6
Turn-off rise time	t_f	—	40	tbd	ns	ref. to Figure 6
Delay mismatch (high and low side turn-on/off)	Δt	—	—	10	ns	ref. to Figure 8
Minimum turn-on (OutH)	t_{pON}	—	70	tbd	ns	ref. to Figure 9 ¹⁾
Minimum turn-off (OutH)	t_{pOFF}	—	70	tbd	ns	ref. to Figure 9 ¹⁾

¹⁾ InH pulses shorter than the "minimum turn-on/off input pulse length" are prolonged to 70 ns. The InL input doesn't have this feature.

5.3.5 General purpose operational amplifier

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
OP input offset voltage	ΔV_{In}	-10	0	10	mV	
OP input offset voltage drift	$\Delta V_{In}/\Delta T$	—	15	—	$\mu V/K$	
OP input high currents (OP-, OP+)	I_{In}	—	0	0.2	μA	$V_{In} = 2 V$
OP input high currents (OP-, OP+)	I_{In}	-0.2	0	—	μA	$V_{In} = 0 V$
OP high output voltage	V_{OPO}	4.9	—	—	V	$V_{OP-} = 0 V$ $V_{OP+} = 2 V$
OP low output voltage	V_{OPO}	—	—	0.1	V	$V_{OP-} = 2 V$ $V_{OP+} = 0 V$
OP output source current	I_{OPO}	—	—	-5	mA	$V_{OP+} = 2 V$ $V_{OP-} = 0 V$ $V_{OPO} = 0V$
OP output sink current	I_{OPO}	5	—	—	mA	$V_{OP+} = 0 V$ $V_{OP-} = 2 V$ $V_{OPO} = 5V$
OP open loop gain	A_{OL}	—	120	—	dB	
OP gain-bandwidth product	$A \times BW$	—	20	—	MHz	¹⁾
OP phase margin	Φ	—	70	—	°	^{1), 2)}

¹⁾ design value

²⁾ due to inevitable parasitics a minimum gain $A \geq 3$ is recommended

5.3.6 General purpose comparator

Parameter	Symbol	Limit Values			Unit	Test condition
		min.	typ.	max.		
CP input offset voltage	ΔV_{In}	-45	-30	-15	mV	$V_{CP+} = V_{CP-}$
CP input high current	I_{CP-}	—	20	35	μA	$V_{CP-} = 5 V$
CP input low current	I_{CP+}	-35	-20	—	μA	$V_{CP+} = 0 V$
CP low output voltage	V_{ICPO}	—	—	0.2	V	$V_{CP+} = 2 V$ $I_{ICPO} = 1 mA$
CP output leakage current	I_{ICPO}	—	—	5	μA	$V_{CP+} = 0 V$ $V_{CP-} = 2 V$ $V_{ICPO} = 5 V$
CP switch-on delay	t_d	—	100	—	ns	$R_{ICPO} = 4.7 k\Omega$ $V_{res} = 5 V$ $V_{ICPO} = 4 V$
CP switch-off delay	t_d	—	300	—	ns	$R_{ICPO} = 4.7 k\Omega$ $V_{res} = 5 V$ $V_{ICPO} = 1 V$

6 Diagrams

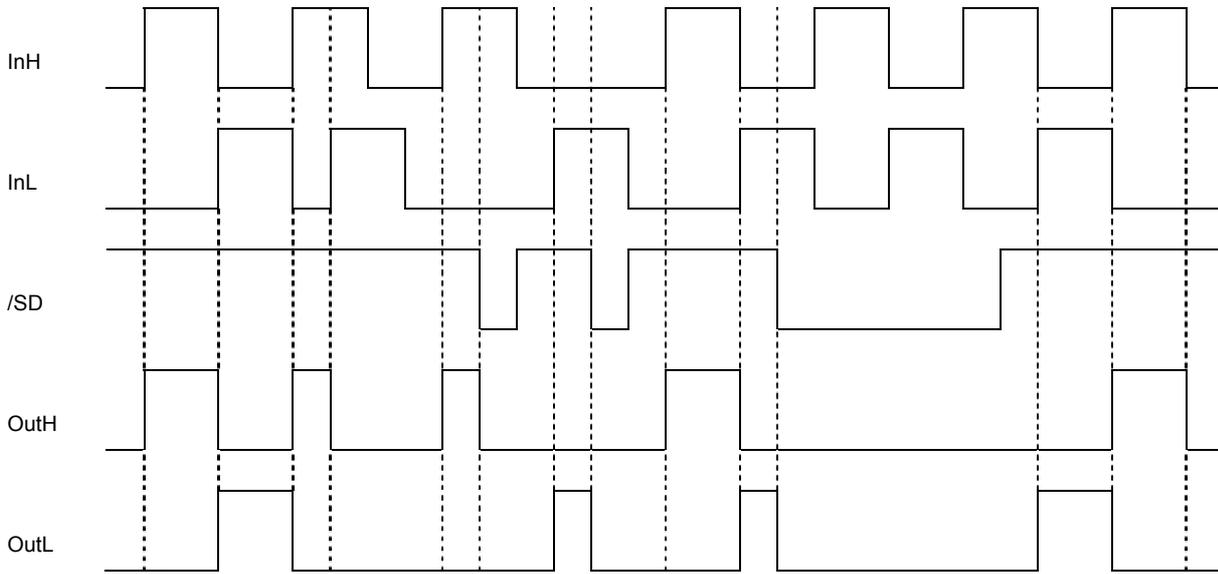


Figure 5 Input/Output timing diagram

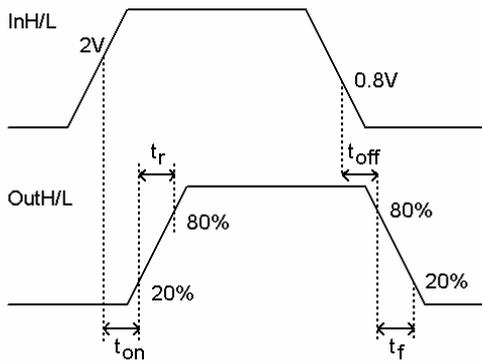


Figure 6: Switching time waveform definition

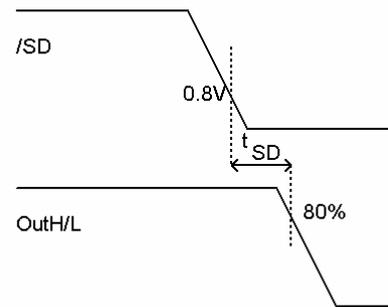


Figure 7: Shutdown waveform definition

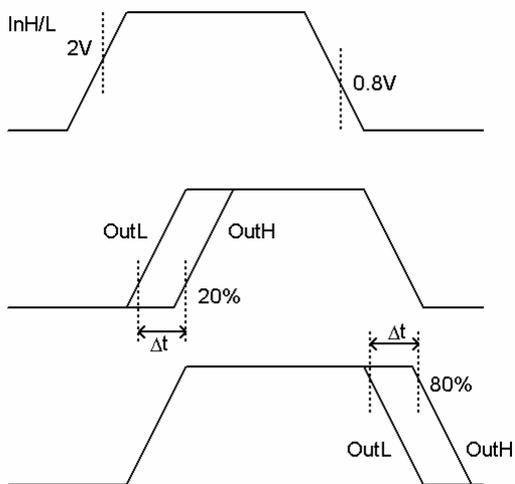


Figure 8: Delay matching waveform definitions

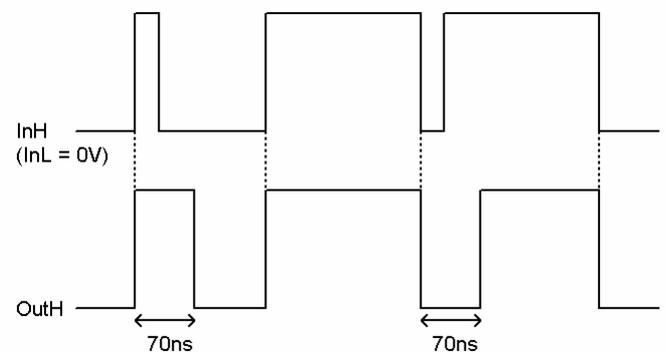


Figure 9: Short InH Pulses