

DATA SHEET

BSN274; BSN274A N-channel enhancement mode vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical D-MOS transistor

BSN274; BSN274A

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

PINNING (BSN274)

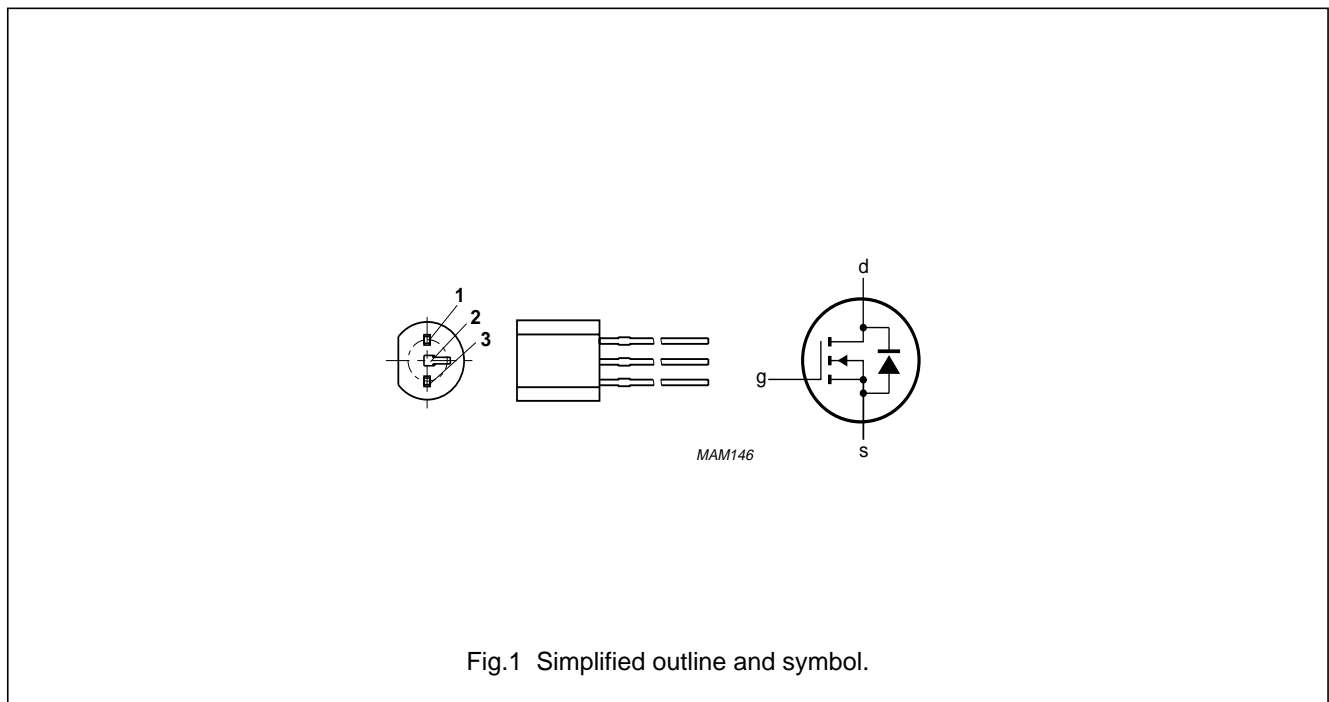
PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING (BSN274A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

PIN CONFIGURATION - TO-92 VARIANT



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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	250	mA
I_{DM}	drain current	peak	–	1	A
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ °C}$ (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain leads minimum 10 mm × 10 mm.

CHARACTERISTICS

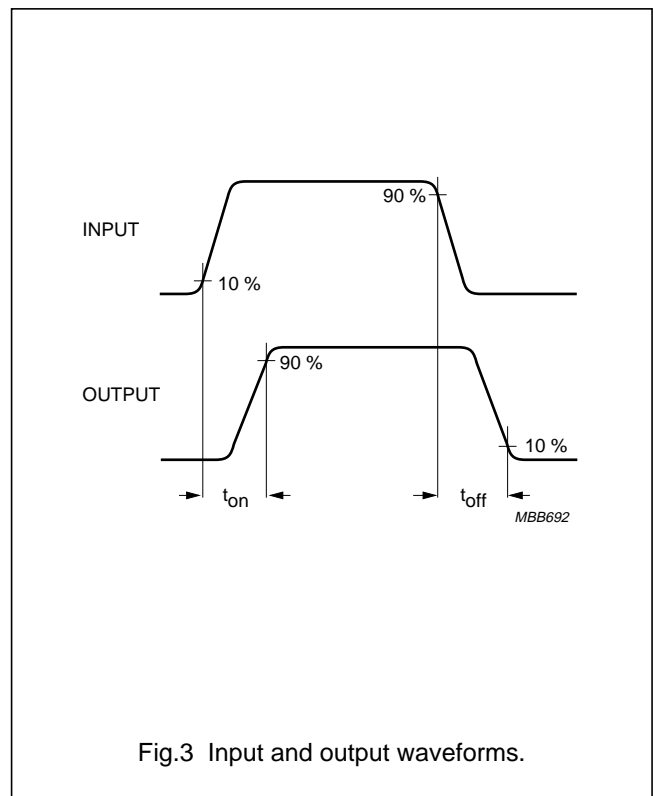
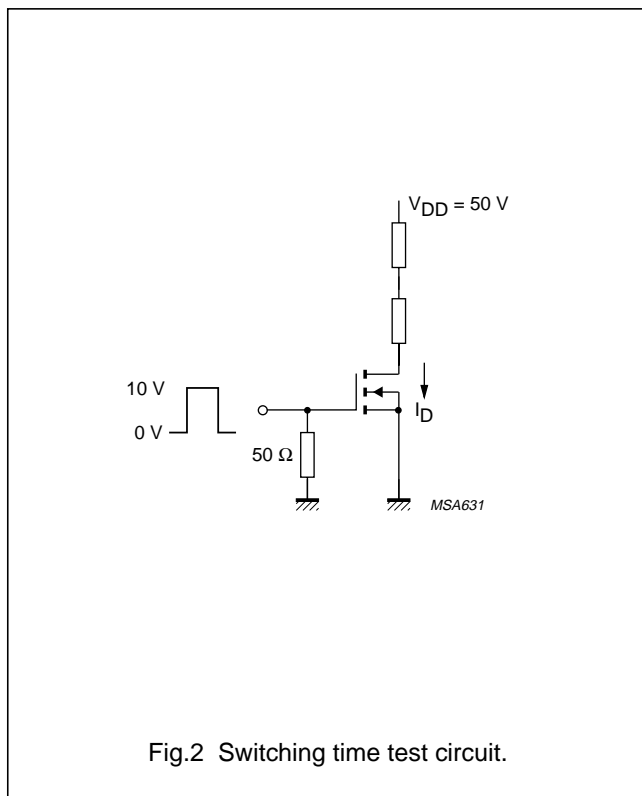
 $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ $I_D = 10\ \mu\text{A}$	270	–	–	V
I_{DSS}	drain-source leakage current	$V_{DS} = 220\text{ V}$ $V_{GS} = 0$	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}$ $V_{DS} = 0$	–	–	100	nA
$V_{GS(th)}$	gate threshold voltage	$I_D = 1\text{ mA}$ $V_{DS} = V_{GS}$	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 250\text{ mA}$ $V_{GS} = 10\text{ V}$	–	6.5	8	Ω
$R_{DS(on)}$	drain-source on-resistance	$I_D = 20\text{ mA}$ $V_{GS} = 2.4\text{ V}$	–	9	14	Ω
$ Y_{fs} $	transfer admittance	$I_D = 250\text{ mA}$ $V_{DS} = 25\text{ V}$	200	400	–	mS
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	–	65	90	pF
C_{oss}	output capacitance	$V_{DS} = 25\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	–	20	30	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	feedback capacitance	$V_{DS} = 25\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	$I_D = 250\text{ mA}$ $V_{DD} = 50\text{ V}$ $V_{GS} = 0\text{ to }10\text{ V}$	–	5	10	ns
t_{off}	switching-off time	$I_D = 250\text{ mA}$ $V_{DD} = 50\text{ V}$ $V_{GS} = 0\text{ to }10\text{ V}$	–	20	30	ns



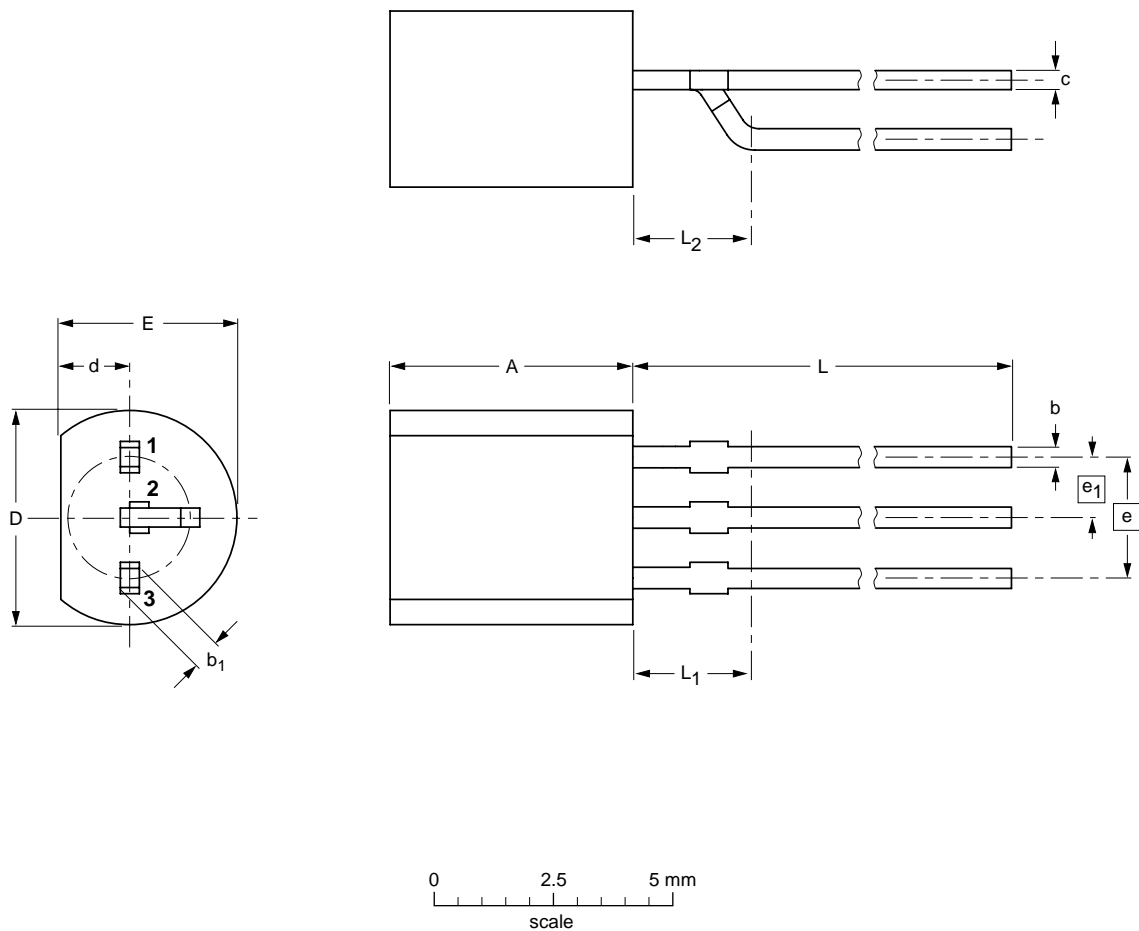
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

137107/00/01/pp8

Date of release: April 1995

Document order number: 9397 750 02463

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