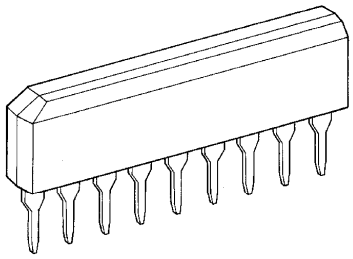
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8005S

5V VOLTAGE REGULATOR WITH WATCHDOG TIMER

The TA8005S is an IC specially designed for micro-computer systems. It incorporates a highly accurate constant-voltage power supply (5 ± 0.25V) and various system reset functions. For system reset, it monitors the output voltage of $V_{REG} \times 85\%$ and has a watchdog timer which can self-diagnose the microcomputer system so that program runaway can be prevented.
Since its bias current is as small as 1.4mA (max.), it can be connected directly to an automotive battery.



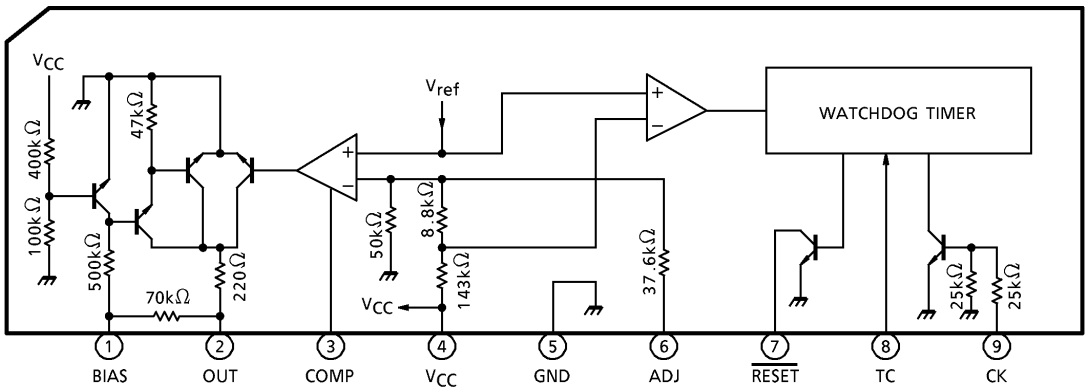
SIP9-P-2.54A

Weight : 0.92g (Typ.)

FEATURES

- Accurate output : 5 ± 0.25V
- Low bias current : 1.4mA (max.)
- Power-on reset timer incorporated
- Watchdog timer incorporated
- Wide operating voltage range : 40V (max.)
- Operating temperature range : from −40 to 85°C
- Output voltage adjusting pin attached
- Small SIP-9 pin

BLOCK DIAGRAM AND PIN LAYOUT



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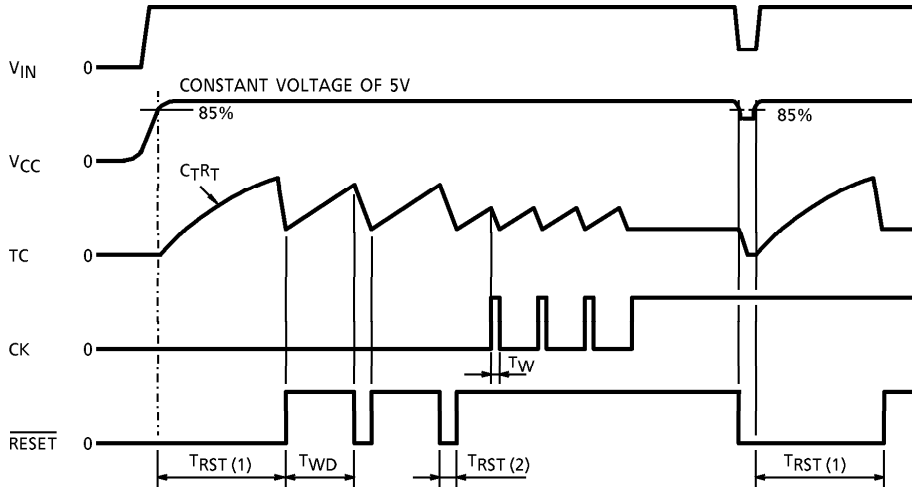
PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION
1	BIAS	Power supply starting pin. The starting current is supplied through a resistor to which the input voltage is applied. When V_{CC} rises above 3.0V, the starting current is absorbed in the internal circuit ; instead, I_{OUT} is supplied via V_{CC}.
2	OUT	Connected to the base of an external PNP transistor so that the output voltage is stabilized. Power supply design suitable for particular load capacities is thus possible. Since the recommended maximum I_{OUT} is 5mA, an output current of 300mA is assured if the external transistor has an H_{FE} of 60 or more.
3	COMP	Phase compensation pin for output stabilization
4	V_{CC}	Power supply pin for internal circuit. The output voltage can also be detected at this pin.
5	GND	Grounded
6	ADJ	Output voltage adjusting pin. The voltage will increase when a resistor is inserted between ADJ and GND. It will reduce when a resistor is inserted between ADJ and V_{CC}. It will become 10V when ADJ and GND are directly connected.
7	$\overline{RESET}$	NPN transistor open-collector output. (1) The signal goes low when the output drops below 85% of the specified level. (2) The pin supplies a reset signal determined by the CR combination connected to the TC pin. (3) The pin supplies reset pulses intermittently if no clock is given to the CK pin. This function is useful when the IC is used as a watchdog timer for a microcomputer system.
8	TC	Time setting pin for the reset and watchdog timers
9	CK	Input pin for watchdog timer. The pin is pulled up to V_{CC} if the IC is used only as a power-on reset timer.

TIMING CHART



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V_{IN1}	60 (1s)	V
	V_{IN2}	−5~V_{CC}	
Output Current	I_{OUT1}	10	mA
	I_{OUT2}	4	
Output Voltage	V_{OUT1}	60 (1s)	V
	V_{OUT2}	16	
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C
Lead Temperature-time	T_{sol}	260 (10s)	°C

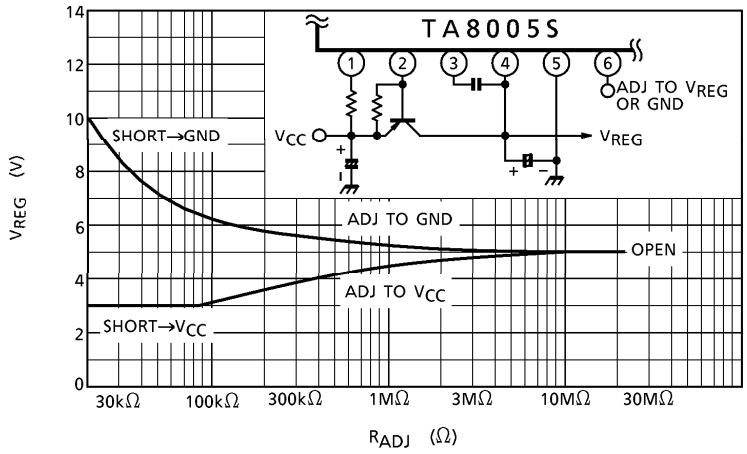
(Note) V_{IN1} : BIAS input
V_{IN2} : CK input
I_{OUT1}, V_{OUT1} : OUT output
I_{OUT2}, V_{OUT2} : $\overline{RESET}$ output

ELECTRICAL CHARACTERISTICS (V_{IN} = 6 to 17V, Ta = −40 to 85°C)

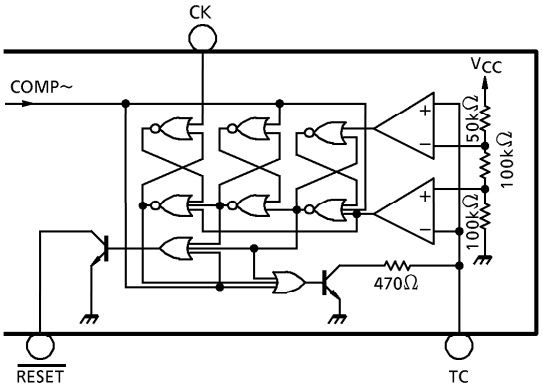
CHARACTERISTIC	SYMBOL	PIN	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{REG}	V_{CC}	—	—	4.75	5.0	5.25	V
Line Regulation	—	V_{CC}	—	V_{IN} = 6~40V	—	0.1	0.5	%
Load Regulation	—	V_{CC}	—	I_{LOAD} = 1~50mA	—	0.1	0.5	%
Temperature Coefficient	—	V_{CC}	—	—	—	0.01	—	% / °C
Output Voltage	V_{OL}	$\overline{RESET}$	—	I_{OL} = 2mA	—	—	0.5	V
Output Leakage Current	I_{LEAK}	$\overline{RESET}$	—	V_{OUT} = 10V	—	—	5	μA
Input Current	I_{IN}	TC	—	V_{IN} = 0~3.5V	−3	—	3	μA
Threshold Voltage	V_{IH}	TC	—	$\overline{RESET}$ High to Low	—	80% × V_{REG}	—	V
	V_{IL}		—	$\overline{RESET}$ Low to High	—	40% × V_{REG}	—	
Input Current	I_{IN}	CK	—	V_{IN} = 5V	—	0.18	0.4	mA
Input Voltage	V_{IH}	CK	—	—	2	—	—	V
	V_{IL}	CK	—	—	—	—	0.5	
Reset Detect Voltage	—	V_{CC}	—	—	82% × V_{REG}	85% × V_{REG}	88% × V_{REG}	V
Standby Current	I_S	V_{CC}	—	V_{IN} = 14V	—	0.85	1.4	mA
Watchdog Timer	T_{WD}	$\overline{RESET}$	—	—	0.9 × C_TR_T	1.1 × C_TR_T	1.3 × C_TR_T	—
Reset Timer (1)	$T_{RST\ (1)}$	$\overline{RESET}$	—	—	1.3 × C_TR_T	1.6 × C_TR_T	1.9 × C_TR_T	—
Reset Timer (2)	$T_{RST\ (2)}$	$\overline{RESET}$	—	—	150 × C_T	300 × C_T	600 × C_T	—
Clock Pulse Width	T_W	CK	—	—	3	—	—	μs

Note : Reset timer (1) : Power-on reset time
Reset timer (2) : Watchdog reset time

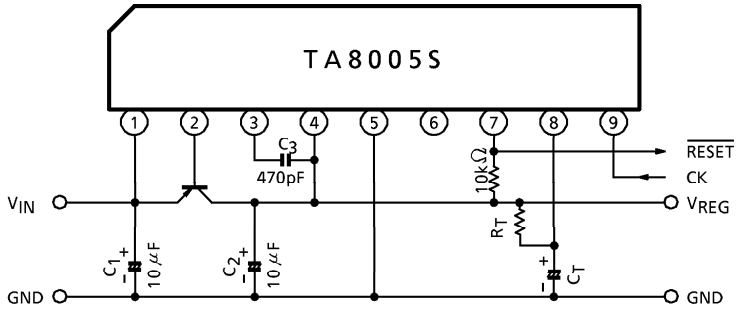
ADJ ADJUSTING RESISTOR DATA



RESET TIMER EQUIVALENT CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT



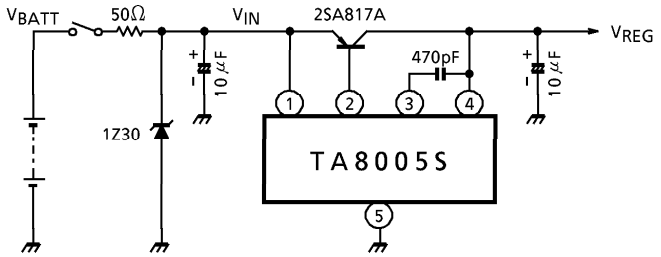
* Cautions for Wiring

1. C_1 and C_2 are for absorbing disturbance, noise, etc. Connect them as close to the IC as possible.
2. C_3 is for phase compensation. Also, connect C_3 close to the IC.

120 Vpeak LOAD DUMP
Note : No protection is needed if a voltage above 60V is not applied.

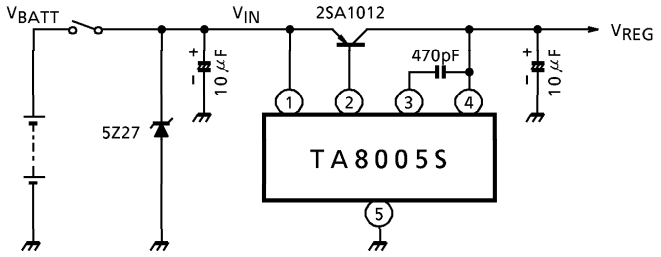
1. Low Output Current Circuit

   I_{LOAD} = 10mA Max., V_{BATT} = 6~17V

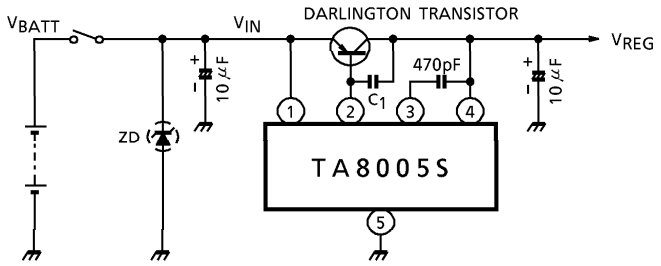


2. High Output Current Circuit

   I_{LOAD} = 300mA Max., V_{BATT} = 6~17V



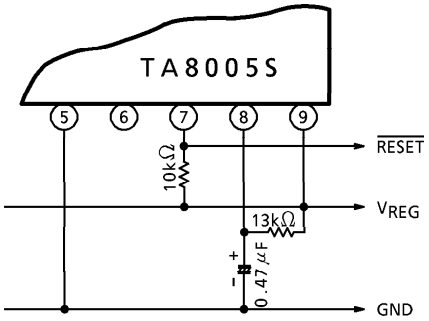
EXAMPLE OF APPLICATION CIRCUIT USING DARLINGTON TRANSISTOR



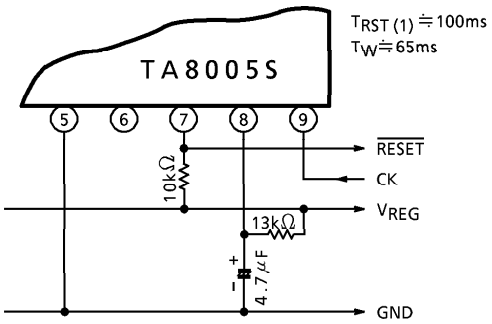
* ● Insert a C_1 value according to the working condition - - typically above 2000pF.
● Insert ZD when necessary.

APPLICATION CIRCUIT OF WATCHDOG / RESET TIMER

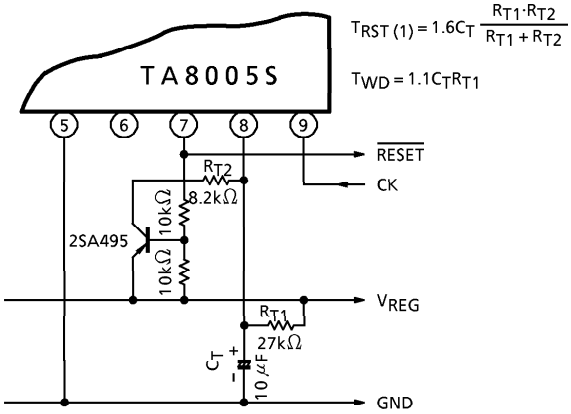
1. $T_{RST\,(1)} \fallingdotseq 10ms$ ····· Power-On Reset Timer



2. $T_{RST\,(1)} \fallingdotseq 1.5T_{WD}$



3. $T_{RST\,(1)} \fallingdotseq 100ms$, $T_{WD} \fallingdotseq 300ms$



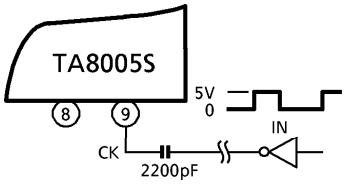
4. Recommended Conditions

PART NAME	MIN.	MAX.	UNIT
C_T	0.01	100	μF
R_T	5	100	kΩ
R_{T1}	—	100	kΩ
R_{T1} // R_{T2} (Note)	5	—	kΩ

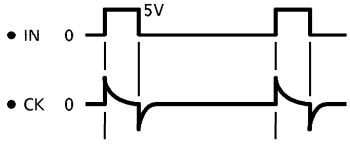
(Note : $R_{T1} // R_{T2} = (R_{T1} \times R_{T2}) / (R_{T1} + R_{T2})$

CK INPUT APPLICATION CIRCUIT

Capacitor Coupling



Timing Chart

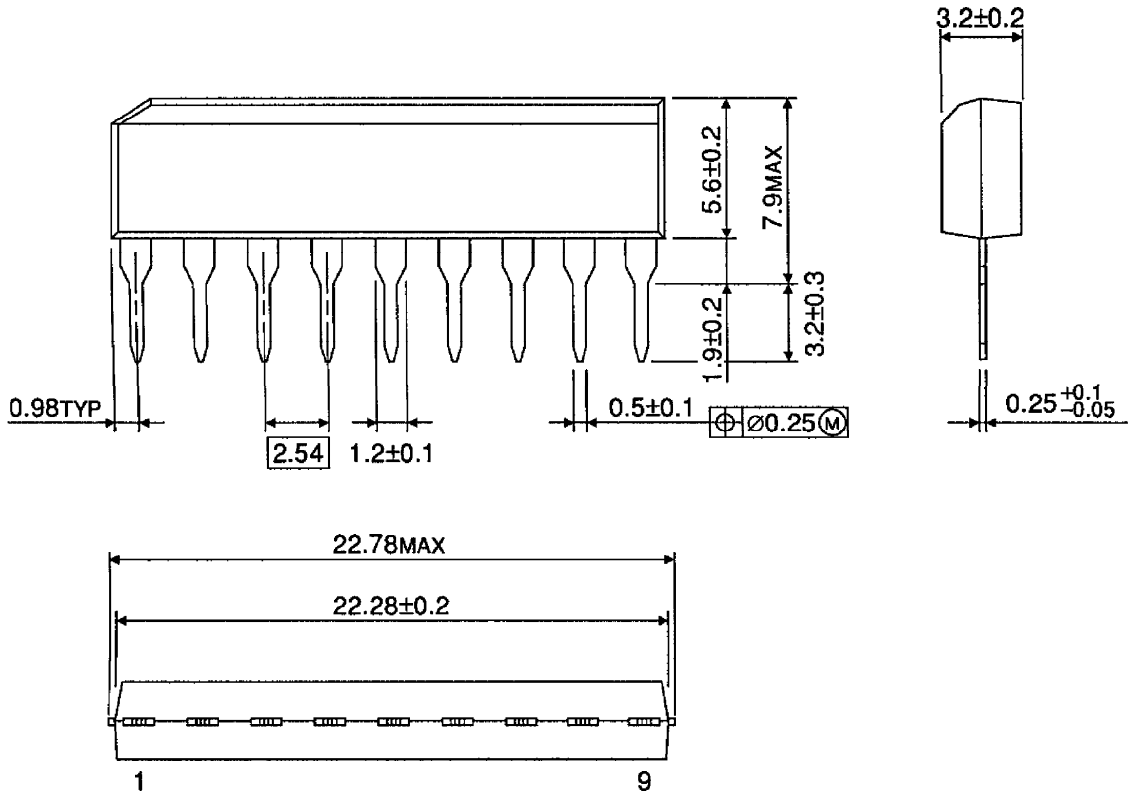


The capacitor coupling allows reset pulses to be supplied intermittently from the $\overline{\text{RESET}}$ pin whether the input level (IN) is high or low.

OUTLINE DRAWING

SIP9-P-2.54A

Unit : mm



Weight : 0.92g (Typ.)