

DRV8825 Stepper Motor Controller IC

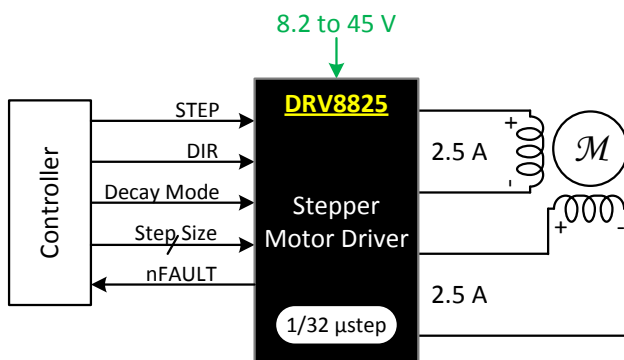
1 Features

- PWM Microstepping Stepper Motor Driver
 - Built-In Microstepping Indexer
 - Up to 1/32 Microstepping
- Multiple Decay Modes
 - Mixed Decay
 - Slow Decay
 - Fast Decay
- 8.2-V to 45-V Operating Supply Voltage Range
- 2.5-A Maximum Drive Current at 24 V and $T_A = 25^\circ\text{C}$
- Simple STEP/DIR Interface
- Low Current Sleep Mode
- Built-In 3.3-V Reference Output
- Small Package and Footprint
- Protection Features
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)
 - VM Undervoltage Lockout (UVLO)
 - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller Machines
- Money Handling Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

4 Simplified Schematic



3 Description

The DRV8825 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers and a microstepping indexer, and is intended to drive a bipolar stepper motor. The output driver block consists of N-channel power MOSFET's configured as full H-bridges to drive the motor windings. The DRV8825 is capable of driving up to 2.5 A of current from each output (with proper heat sinking, at 24 V and 25°C).

A simple STEP/DIR interface allows easy interfacing to controller circuits. Mode pins allow for configuration of the motor in full-step up to 1/32-step modes. Decay mode is configurable so that slow decay, fast decay, or mixed decay can be used. A low-power sleep mode is provided which shuts down internal circuitry to achieve very low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

Internal shutdown functions are provided for overcurrent, short circuit, under voltage lockout and over temperature. Fault conditions are indicated via the nFAULT pin.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-------------|-------------------|
| DRV8825 | HTSSOP (28) | 9.70 mm x 6.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Microstepping Current Waveform

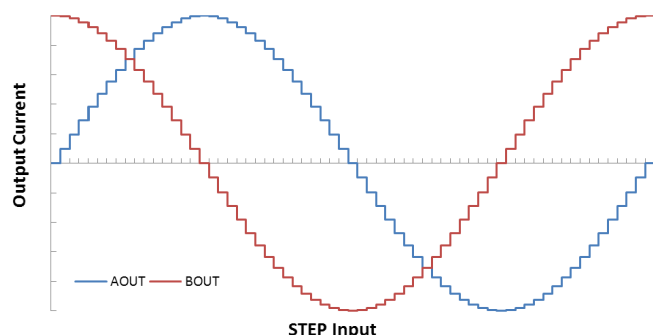


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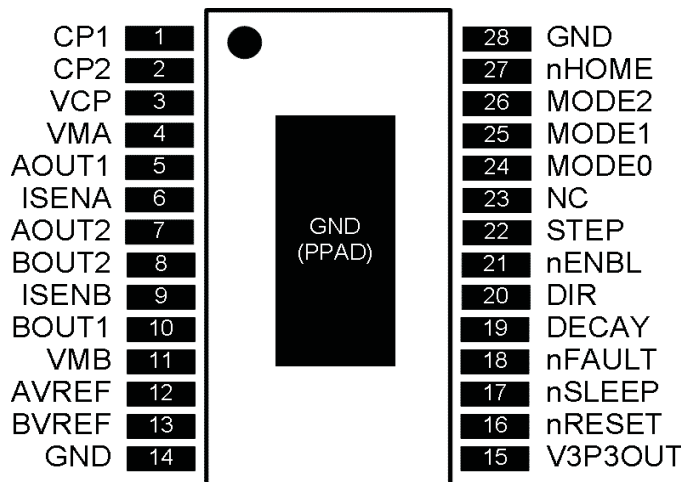
5 Revision History

Changes from Revision E (August 2013) to Revision F

Page

| | |
|--|----------|
| • Added new sections and reordered data sheet to fit new TI flow | 1 |
| • Updated pin descriptions | 3 |
| • Added power supply ramp rate and updated ISENSE pin voltage in <i>Absolute Maximum Ratings</i> | 4 |
| • Updated V_{IL} voltage minimum and typical in <i>Electrical Characteristics</i> | 6 |
| • Updated I_{IN} and t_{DEG} in <i>Electrical Characteristics</i> | 6 |

6 Pin Configuration and Functions


Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|-------------------------|--------|--------------------|--------------------------------------|--|
| NAME | NO. | | | |
| POWER AND GROUND | | | | |
| CP1 | 1 | I/O | Charge pump flying capacitor | Connect a 0.01- μ F 50-V capacitor between CP1 and CP2. |
| CP2 | 2 | I/O | Charge pump flying capacitor | |
| GND | 14, 28 | — | Device ground | |
| VCP | 3 | I/O | High-side gate drive voltage | Connect a 0.1- μ F 16-V ceramic capacitor and a 1-M Ω resistor to VM. |
| VMA | 4 | — | Bridge A power supply | Connect to motor supply (8.2 to 45 V). Both pins must be connected to the same supply, bypassed with a 0.1- μ F capacitor to GND, and connected to appropriate bulk capacitance. |
| VMB | 11 | — | Bridge B power supply | |
| V3P3OUT | 15 | O | 3.3-V regulator output | Bypass to GND with a 0.47- μ F 6.3-V ceramic capacitor. Can be used to supply VREF. |
| CONTROL | | | | |
| AVREF | 12 | I | Bridge A current set reference input | Reference voltage for winding current set. Normally AVREF and BVREF are connected to the same voltage. Can be connected to V3P3OUT. |
| BVREF | 13 | I | Bridge B current set reference input | |
| DECAY | 19 | I | Decay mode | Low = slow decay, open = mixed decay, high = fast decay. Internal pulldown and pullup. |
| DIR | 20 | I | Direction input | Level sets the direction of stepping. Internal pulldown. |
| MODE0 | 24 | I | Microstep mode 0 | MODE0 through MODE2 set the step mode - full, 1/2, 1/4, 1/8/1/16, or 1/32 step. Internal pulldown. |
| MODE1 | 25 | I | Microstep mode 1 | |
| MODE2 | 26 | I | Microstep mode 2 | |
| NC | 23 | — | No connect | Leave this pin unconnected. |
| nENBL | 21 | I | Enable input | Logic high to disable device outputs and indexer operation, logic low to enable. Internal pulldown. |
| nRESET | 16 | I | Reset input | Active-low reset input initializes the indexer logic and disables the H-bridge outputs. Internal pulldown. |
| nSLEEP | 17 | I | Sleep mode input | Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown. |
| STEP | 22 | I | Step input | Rising edge causes the indexer to move one step. Internal pulldown. |
| STATUS | | | | |
| nFAULT | 18 | OD | Fault | Logic low when in fault condition (overtemp, overcurrent) |

(1) Directions: I = input, O = output, OD = open-drain output, IO = input/output

Pin Functions (continued)

| PIN | | I/O ⁽¹⁾ | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---------------|-----|--------------------|--------------------------|---|
| NAME | NO. | | | |
| nHOME | 27 | OD | Home position | Logic low when at home state of step table |
| OUTPUT | | | | |
| AOUT1 | 5 | O | Bridge A output 1 | Connect to bipolar stepper motor winding A. Positive current is AOUT1 → AOUT2 |
| AOUT2 | 7 | O | Bridge A output 2 | |
| BOUT1 | 10 | O | Bridge B output 1 | Connect to bipolar stepper motor winding B. Positive current is BOUT1 → BOUT2 |
| BOUT2 | 8 | O | Bridge B output 2 | |
| ISENA | 6 | I/O | Bridge A ground / Isense | Connect to current sense resistor for bridge A. |
| ISENB | 9 | I/O | Bridge B ground / Isense | Connect to current sense resistor for bridge B. |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | | MIN | MAX | UNIT |
|----------------------|--|---|--------------------|------|
| V _(VMx) | Power supply voltage | -0.3 | 47 | V |
| | Power supply ramp rate | | 1 | V/μs |
| | Digital pin voltage | -0.5 | 7 | V |
| V _(xVREF) | Input voltage | -0.3 | 4 | V |
| | ISENSEx pin voltage ⁽³⁾ | -0.8 | 0.8 | V |
| | Peak motor drive output current, t < 1 μs | | Internally limited | A |
| | Continuous motor drive output current ⁽⁴⁾ | 0 | 2.5 | A |
| | Continuous total power dissipation | See Thermal Information | | |
| T _J | Operating junction temperature range | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Transients of ±1 V for less than 25 ns are acceptable
- (4) Power dissipation and thermal limits must be observed.

7.2 Handling Ratings

| | | MIN | MAX | UNIT |
|--------------------|---------------------------|--|------|------|
| T _{stg} | Storage temperature range | -60 | 150 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | | |
| | | -2000 | 2000 | |
| | | -500 | 500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------|---|-----|-----|-----|------|
| V _(VMx) | Motor power supply voltage range ⁽¹⁾ | 8.2 | | 45 | V |
| V _(VREF) | VREF input voltage ⁽²⁾ | 1 | | 3.5 | V |
| I _{V3P3} | V3P3OUT load current | 0 | | 1 | mA |

- (1) All V_M pins must be connected to the same supply voltage.
- (2) Operational at VREF between 0 to 1 V, but accuracy is degraded.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DRV8825 | UNIT |
|-------------------------------|---|---------|------|
| | | PWP | |
| | | 28 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽²⁾ | 31.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance ⁽³⁾ | 15.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance ⁽⁴⁾ | 5.6 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 0.2 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 5.5 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | 1.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

 over operating free-air temperature range of -40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|------|------|------|--------------------|
| POWER SUPPLIES | | | | | | |
| I_{VM} | VM operating supply current | $V_{(VMx)} = 24\text{ V}$ | | 5 | 8 | mA |
| I_{VMQ} | VM sleep mode supply current | $V_{(VMx)} = 24\text{ V}$ | | 10 | 20 | μA |
| V3P3OUT REGULATOR | | | | | | |
| V_{3P3} | V3P3OUT voltage | $\text{IOUT} = 0\text{ to }1\text{ mA}$ | 3.2 | 3.3 | 3.4 | V |
| LOGIC-LEVEL INPUTS | | | | | | |
| V_{IL} | Input low voltage | | 0 | | 0.7 | V |
| V_{IH} | Input high voltage | | 2.2 | | 5.25 | V |
| V_{HYS} | Input hysteresis | | 0.3 | 0.45 | 0.6 | V |
| I_{IL} | Input low current | $V_{IN} = 0$ | -20 | | 20 | μA |
| I_{IH} | Input high current | $V_{IN} = 3.3\text{ V}$ | | | 100 | μA |
| R_{PD} | Internal pulldown resistance | | | 100 | | k Ω |
| nHOME, nFAULT OUTPUTS (OPEN-DRAIN OUTPUTS) | | | | | | |
| V_{OL} | Output low voltage | $I_O = 5\text{ mA}$ | | | 0.5 | V |
| I_{OH} | Output high leakage current | $V_O = 3.3\text{ V}$ | | | 1 | μA |
| DECAY INPUT | | | | | | |
| V_{IL} | Input low threshold voltage | For slow decay mode | | | 0.8 | V |
| V_{IH} | Input high threshold voltage | For fast decay mode | 2 | | | V |
| I_{IN} | Input current | | -40 | | 40 | μA |
| R_{PU} | Internal pullup resistance (to 3.3 V) | | | 130 | | k Ω |
| R_{PD} | Internal pulldown resistance | | | 80 | | k Ω |
| H-BRIDGE FETS | | | | | | |
| $R_{DS(ON)}$ | HS FET on resistance | $V_{(VMx)} = 24\text{ V}, I_O = 1\text{ A}, T_J = 25^{\circ}\text{C}$ | | 0.2 | | Ω |
| | | $V_{(VMx)} = 24\text{ V}, I_O = 1\text{ A}, T_J = 85^{\circ}\text{C}$ | | 0.25 | 0.32 | |
| | LS FET on resistance | $V_{(VMx)} = 24\text{ V}, I_O = 1\text{ A}, T_J = 25^{\circ}\text{C}$ | | 0.2 | | |
| | | $V_{(VMx)} = 24\text{ V}, I_O = 1\text{ A}, T_J = 85^{\circ}\text{C}$ | | 0.25 | 0.32 | |
| I_{OFF} | Off-state leakage current | | -20 | | 20 | μA |
| MOTOR DRIVER | | | | | | |
| f_{PWM} | Internal current control PWM frequency | | | 30 | | kHz |
| t_{BLANK} | Current sense blanking time | | | 4 | | μs |
| t_R | Rise time | | 30 | | 200 | ns |
| t_F | Fall time | | 30 | | 200 | ns |
| PROTECTION CIRCUITS | | | | | | |
| V_{UVLO} | VM undervoltage lockout voltage | $V_{(VMx)}$ rising | | 7.8 | 8.2 | V |
| I_{OCP} | Overcurrent protection trip level | | 3 | | | A |
| t_{DEG} | Overcurrent deglitch time | | | 3 | | μs |
| t_{TSD} | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | $^{\circ}\text{C}$ |
| CURRENT CONTROL | | | | | | |
| I_{REF} | xVREF input current | $V_{(xVREF)} = 3.3\text{ V}$ | -3 | | 3 | μA |
| V_{TRIP} | xISENSE trip voltage | $V_{(xVREF)} = 3.3\text{ V}, 100\%$ current setting | 635 | 660 | 685 | mV |
| ΔI_{TRIP} | Current trip accuracy (relative to programmed value) | $V_{(xVREF)} = 3.3\text{ V}, 5\%$ current setting | -25% | | 25% | |
| | | $V_{(xVREF)} = 3.3\text{ V}, 10\%$ to 34% current setting | -15% | | 15% | |
| | | $V_{(xVREF)} = 3.3\text{ V}, 38\%$ to 67% current setting | -10% | | 10% | |
| | | $V_{(xVREF)} = 3.3\text{ V}, 71\%$ to 100% current setting | -5% | | 5% | |
| A_{ISENSE} | Current sense amplifier gain | Reference only | | 5 | | V/V |

7.6 Timing Requirements

| | | | MIN | MAX | UNIT |
|---|----------------|--|-----|-----|---------|
| 1 | f_{STEP} | Step frequency | | 250 | kHz |
| 2 | $t_{WH(STEP)}$ | Pulse duration, STEP high | 1.9 | | μ s |
| 3 | $t_{WL(STEP)}$ | Pulse duration, STEP low | 1.9 | | μ s |
| 4 | $t_{SU(STEP)}$ | Setup time, command before STEP rising | 650 | | ns |
| 5 | $t_{H(STEP)}$ | Hold time, command after STEP rising | 650 | | ns |
| 6 | t_{ENBL} | Enable time, nENBL active to STEP | 650 | | ns |
| 7 | t_{WAKE} | Wakeup time, nSLEEP inactive high to STEP input accepted | | 1.7 | ms |

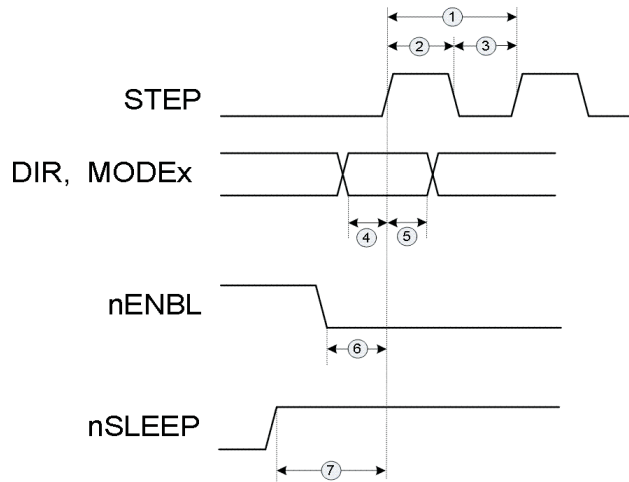


Figure 1. Timing Diagram

7.7 Typical Characteristics

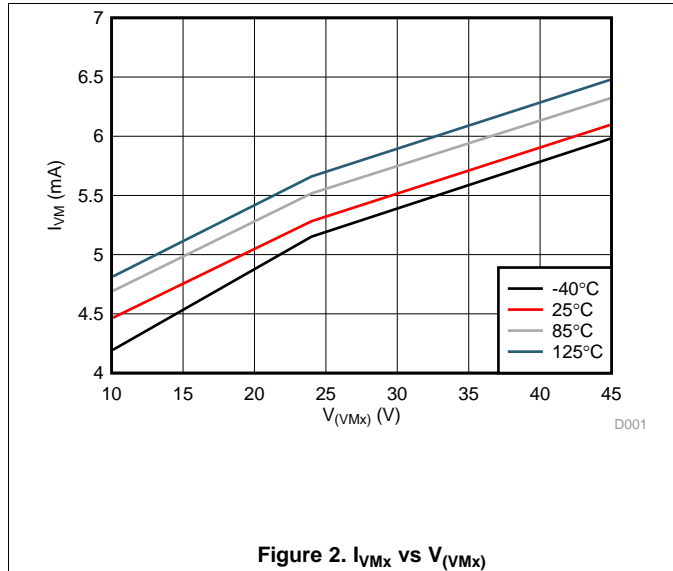


Figure 2. I_{VMx} vs V_{VMx}

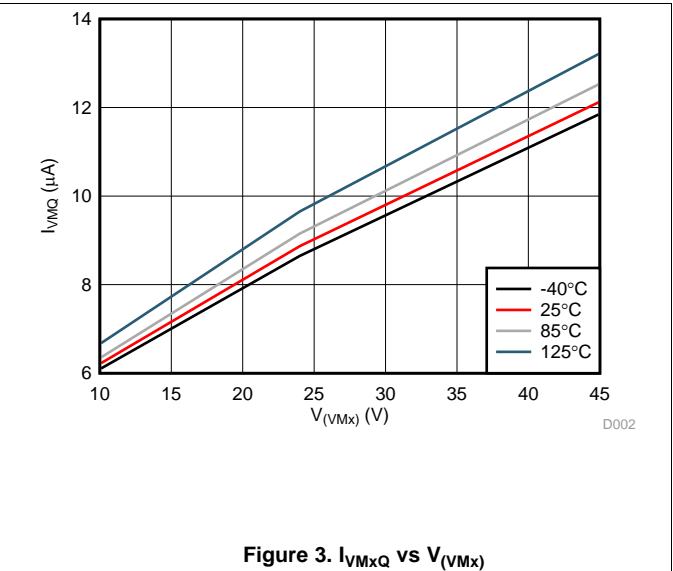


Figure 3. I_{VMxQ} vs V_{VMx}

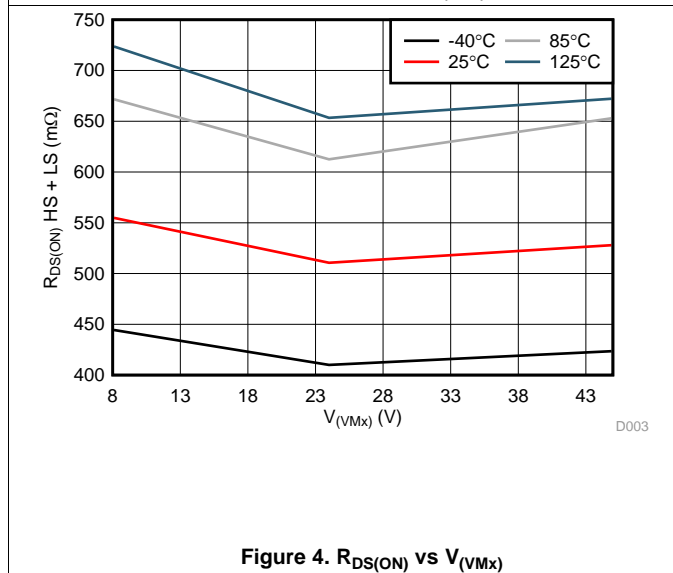


Figure 4. $R_{DS(ON)}$ vs V_{VMx}

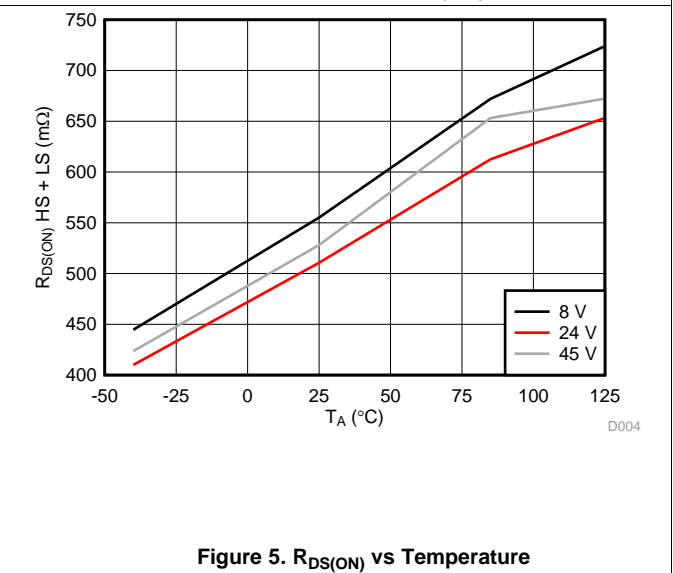


Figure 5. $R_{DS(ON)}$ vs Temperature

8 Detailed Description

8.1 Overview

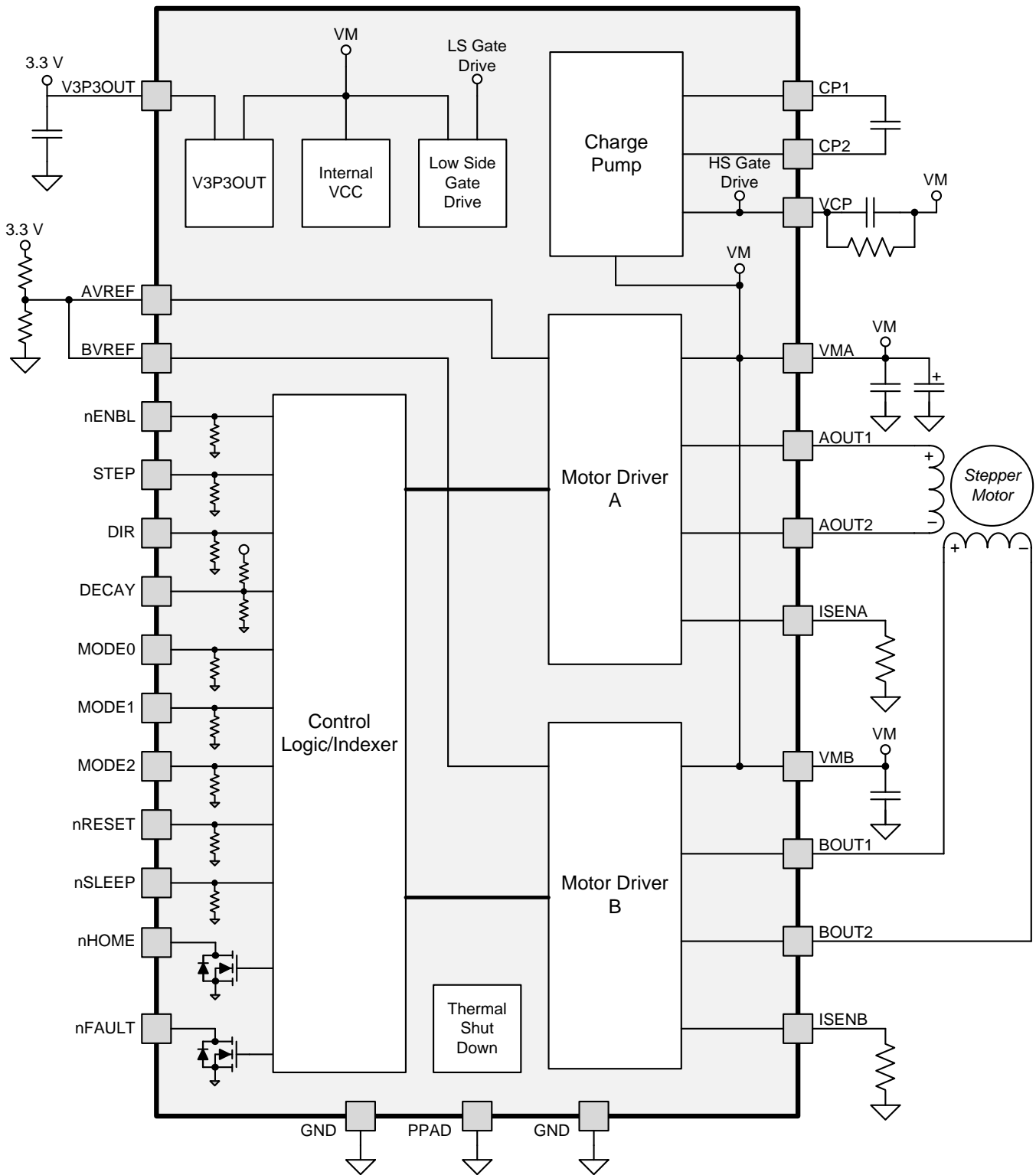
The DRV8825 is an integrated motor driver solution for bipolar stepper motors. The device integrates two NMOS H-bridges, current sense, regulation circuitry, and a microstepping indexer. The DRV8825 can be powered with a supply voltage between 8.2 and 45 V and is capable of providing an output current up to 2.5 A full-scale.

A simple STEP/DIR interface allows for easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level.

The current regulation is highly configurable, with three decay modes of operation. Depending on the application requirements, the user can select fast, slow, and mixed decay.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Motor Drivers

The DRV8825 contains two H-bridge motor drivers with current-control PWM circuitry. Figure 6 shows a block diagram of the motor control circuitry.

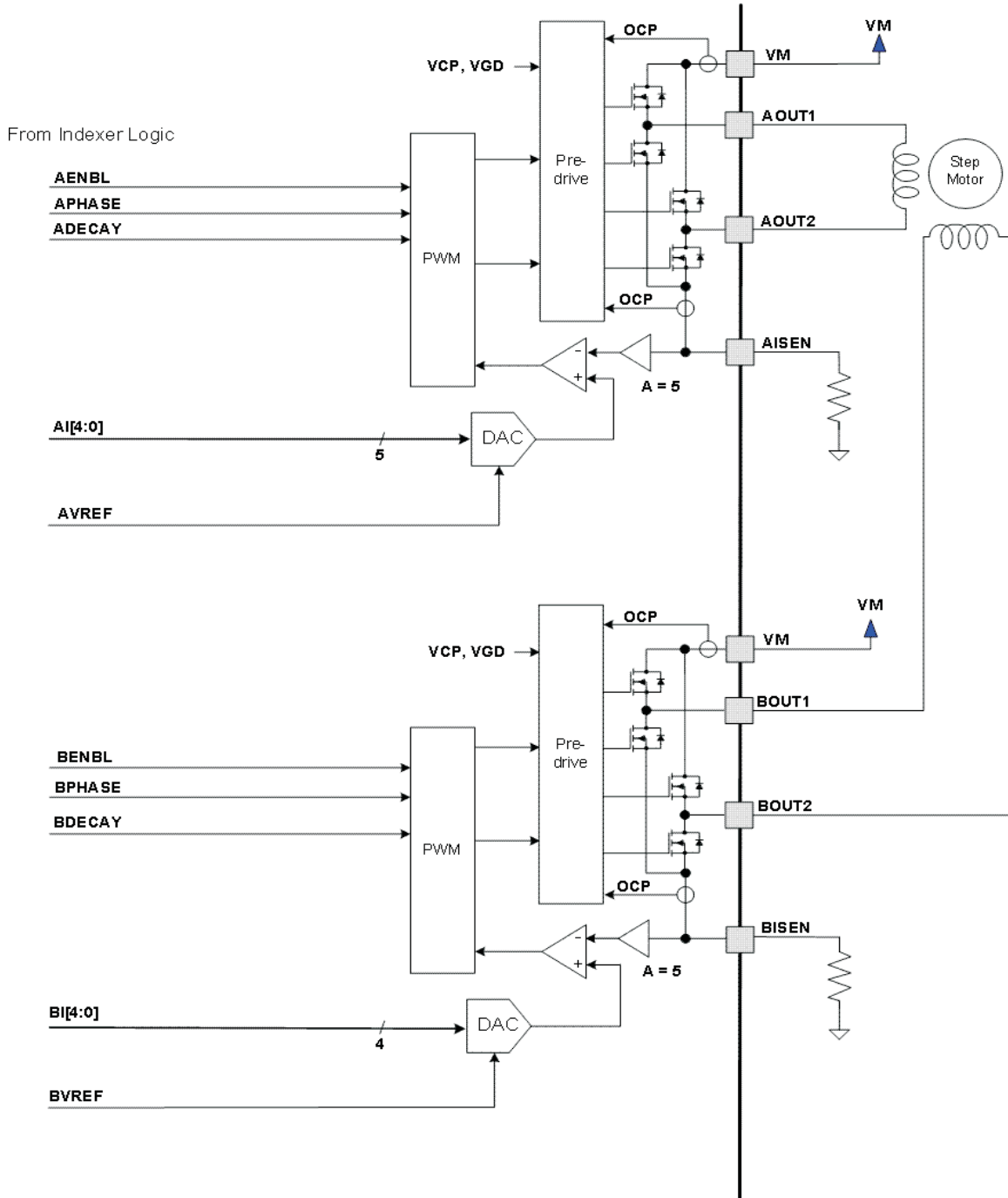


Figure 6. Motor Control Circuitry

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

Feature Description (continued)

8.3.2 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

In stepping motors, current regulation is used to vary the current in the two windings in a semi-sinusoidal fashion to provide smooth motion.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins.

The full-scale (100%) chopping current is calculated in [Equation 1](#).

$$I_{\text{CHOP}} = \frac{V_{(\text{xREF})}}{5 \times R_{\text{ISENSE}}} \quad (1)$$

Example:

If a 0.25-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be $2.5 \text{ V} / (5 \times 0.25 \text{ } \Omega) = 2 \text{ A}$.

The reference voltage is scaled by an internal DAC that allows fractional stepping of a bipolar stepper motor, as described in the microstepping indexer section below.

8.3.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in [Figure 7](#) as case 1. The current flow direction shown indicates positive current flow.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches 0, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in [Figure 7](#) as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in [Figure 7](#) as case 3.

Feature Description (continued)

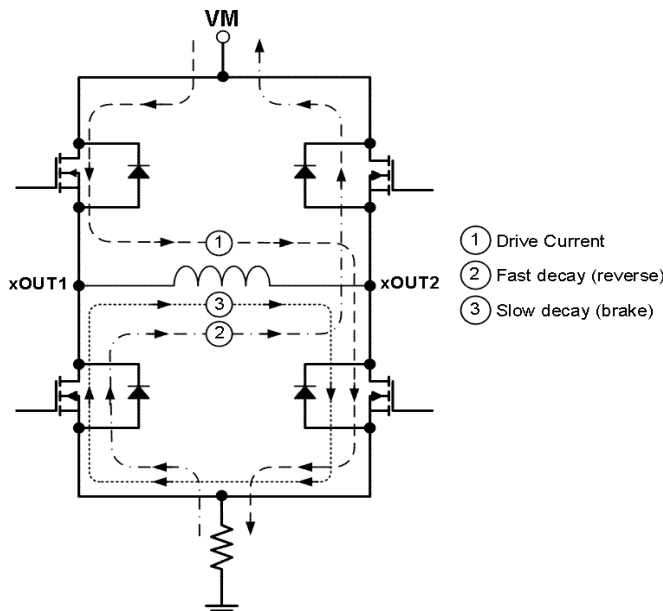


Figure 7. Decay Mode

The DRV8825 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin; logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period. This occurs only if the current through the winding is decreasing (per the indexer step table); if the current is increasing, then slow decay is used.

8.3.4 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs. Note that the blanking time also sets the minimum on time of the PWM.

8.3.5 Microstepping Indexer

Built-in indexer logic in the DRV8825 allows a number of different stepping configurations. The MODE0 through MODE2 pins are used to configure the stepping format as shown in Table 1.

Table 1. Stepping Format

| MODE2 | MODE1 | MODE0 | STEP MODE |
|-------|-------|-------|---|
| 0 | 0 | 0 | Full step (2-phase excitation) with 71% current |
| 0 | 0 | 1 | 1/2 step (1-2 phase excitation) |
| 0 | 1 | 0 | 1/4 step (W1-2 phase excitation) |
| 0 | 1 | 1 | 8 microsteps/step |
| 1 | 0 | 0 | 16 microsteps/step |
| 1 | 0 | 1 | 32 microsteps/step |
| 1 | 1 | 0 | 32 microsteps/step |
| 1 | 1 | 1 | 32 microsteps/step |

Table 2 shows the relative current and step directions for different settings of MODEx. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that if the step mode is changed while stepping, the indexer will advance to the next valid state for the new MODEx setting at the rising edge of STEP.

The home state is 45°. This state is entered at power-up or application of nRESET. This is shown in **Table 2** by the shaded cells. The logic inputs DIR, STEP, nRESET, and MODEx have internal pulldown resistors of 100 kΩ.

Table 2. Relative Current and Step Directions

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|-----------|-----------|----------|----------|----------|------------------|----------------------|----------------------|---------------------|
| 1 | 1 | 1 | 1 | 1 | | 100% | 0% | 0 |
| 2 | | | | | | 100% | 5% | 3 |
| 3 | 2 | | | | | 100% | 10% | 6 |
| 4 | | | | | | 99% | 15% | 8 |
| 5 | 3 | 2 | | | | 98% | 20% | 11 |
| 6 | | | | | | 97% | 24% | 14 |
| 7 | 4 | | | | | 96% | 29% | 17 |
| 8 | | | | | | 94% | 34% | 20 |
| 9 | 5 | 3 | 2 | | | 92% | 38% | 23 |
| 10 | | | | | | 90% | 43% | 25 |
| 11 | 6 | | | | | 88% | 47% | 28 |
| 12 | | | | | | 86% | 51% | 31 |
| 13 | 7 | 4 | | | | 83% | 56% | 34 |
| 14 | | | | | | 80% | 60% | 37 |
| 15 | 8 | | | | | 77% | 63% | 39 |
| 16 | | | | | | 74% | 67% | 42 |
| 17 | 9 | 5 | 3 | 2 | 1 | 71% | 71% | 45 |
| 18 | | | | | | 67% | 74% | 48 |
| 19 | 10 | | | | | 63% | 77% | 51 |
| 20 | | | | | | 60% | 80% | 53 |
| 21 | 11 | 6 | | | | 56% | 83% | 56 |
| 22 | | | | | | 51% | 86% | 59 |
| 23 | 12 | | | | | 47% | 88% | 62 |
| 24 | | | | | | 43% | 90% | 65 |
| 25 | 13 | 7 | 4 | | | 38% | 92% | 68 |
| 26 | | | | | | 34% | 94% | 70 |
| 27 | 14 | | | | | 29% | 96% | 73 |
| 28 | | | | | | 24% | 97% | 76 |
| 29 | 15 | 8 | | | | 20% | 98% | 79 |
| 30 | | | | | | 15% | 99% | 82 |
| 31 | 16 | | | | | 10% | 100% | 84 |
| 32 | | | | | | 5% | 100% | 87 |
| 33 | 17 | 9 | 5 | 3 | | 0% | 100% | 90 |
| 34 | | | | | | -5% | 100% | 93 |
| 35 | 18 | | | | | -10% | 100% | 96 |
| 36 | | | | | | -15% | 99% | 98 |
| 37 | 19 | 10 | | | | -20% | 98% | 101 |
| 38 | | | | | | -24% | 97% | 104 |
| 39 | 20 | | | | | -29% | 96% | 107 |

Table 2. Relative Current and Step Directions (continued)

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|-----------|-----------|----------|----------|----------|------------------|----------------------|----------------------|---------------------|
| 40 | | | | | | -34% | 94% | 110 |
| 41 | 21 | 11 | 6 | | | -38% | 92% | 113 |
| 42 | | | | | | -43% | 90% | 115 |
| 43 | 22 | | | | | -47% | 88% | 118 |
| 44 | | | | | | -51% | 86% | 121 |
| 45 | 23 | 12 | | | | -56% | 83% | 124 |
| 46 | | | | | | -60% | 80% | 127 |
| 47 | 24 | | | | | -63% | 77% | 129 |
| 48 | | | | | | -67% | 74% | 132 |
| 49 | 25 | 13 | 7 | 4 | 2 | -71% | 71% | 135 |
| 50 | | | | | | -74% | 67% | 138 |
| 51 | 26 | | | | | -77% | 63% | 141 |
| 52 | | | | | | -80% | 60% | 143 |
| 53 | 27 | 14 | | | | -83% | 56% | 146 |
| 54 | | | | | | -86% | 51% | 149 |
| 55 | 28 | | | | | -88% | 47% | 152 |
| 56 | | | | | | -90% | 43% | 155 |
| 57 | 29 | 15 | 8 | | | -92% | 38% | 158 |
| 58 | | | | | | -94% | 34% | 160 |
| 59 | 30 | | | | | -96% | 29% | 163 |
| 60 | | | | | | -97% | 24% | 166 |
| 61 | 31 | 16 | | | | -98% | 20% | 169 |
| 62 | | | | | | -99% | 15% | 172 |
| 63 | 32 | | | | | -100% | 10% | 174 |
| 64 | | | | | | -100% | 5% | 177 |
| 65 | 33 | 17 | 9 | 5 | | -100% | 0% | 180 |
| 66 | | | | | | -100% | -5% | 183 |
| 67 | 34 | | | | | -100% | -10% | 186 |
| 68 | | | | | | -99% | -15% | 188 |
| 69 | 35 | 18 | | | | -98% | -20% | 191 |
| 70 | | | | | | -97% | -24% | 194 |
| 71 | 36 | | | | | -96% | -29% | 197 |
| 72 | | | | | | -94% | -34% | 200 |
| 73 | 37 | 19 | 10 | | | -92% | -38% | 203 |
| 74 | | | | | | -90% | -43% | 205 |
| 75 | 38 | | | | | -88% | -47% | 208 |
| 76 | | | | | | -86% | -51% | 211 |
| 77 | 39 | 20 | | | | -83% | -56% | 214 |
| 78 | | | | | | -80% | -60% | 217 |
| 79 | 40 | | | | | -77% | -63% | 219 |
| 80 | | | | | | -74% | -67% | 222 |
| 81 | 41 | 21 | 11 | 6 | 3 | -71% | -71% | 225 |
| 82 | | | | | | -67% | -74% | 228 |
| 83 | 42 | | | | | -63% | -77% | 231 |
| 84 | | | | | | -60% | -80% | 233 |
| 85 | 43 | 22 | | | | -56% | -83% | 236 |
| 86 | | | | | | -51% | -86% | 239 |

Table 2. Relative Current and Step Directions (continued)

| 1/32 STEP | 1/16 STEP | 1/8 STEP | 1/4 STEP | 1/2 STEP | FULL STEP 70% | WINDING CURRENT A | WINDING CURRENT B | ELECTRICAL ANGLE |
|-----------|-----------|----------|----------|----------|------------------|----------------------|----------------------|---------------------|
| 87 | 44 | | | | | -47% | -88% | 242 |
| 88 | | | | | | -43% | -90% | 245 |
| 89 | 45 | 23 | 12 | | | -38% | -92% | 248 |
| 90 | | | | | | -34% | -94% | 250 |
| 91 | 46 | | | | | -29% | -96% | 253 |
| 92 | | | | | | -24% | -97% | 256 |
| 93 | 47 | 24 | | | | -20% | -98% | 259 |
| 94 | | | | | | -15% | -99% | 262 |
| 95 | 48 | | | | | -10% | -100% | 264 |
| 96 | | | | | | -5% | -100% | 267 |
| 97 | 49 | 25 | 13 | 7 | | 0% | -100% | 270 |
| 98 | | | | | | 5% | -100% | 273 |
| 99 | 50 | | | | | 10% | -100% | 276 |
| 100 | | | | | | 15% | -99% | 278 |
| 101 | 51 | 26 | | | | 20% | -98% | 281 |
| 102 | | | | | | 24% | -97% | 284 |
| 103 | 52 | | | | | 29% | -96% | 287 |
| 104 | | | | | | 34% | -94% | 290 |
| 105 | 53 | 27 | 14 | | | 38% | -92% | 293 |
| 106 | | | | | | 43% | -90% | 295 |
| 107 | 54 | | | | | 47% | -88% | 298 |
| 108 | | | | | | 51% | -86% | 301 |
| 109 | 55 | 28 | | | | 56% | -83% | 304 |
| 110 | | | | | | 60% | -80% | 307 |
| 111 | 56 | | | | | 63% | -77% | 309 |
| 112 | | | | | | 67% | -74% | 312 |
| 113 | 57 | 29 | 15 | 8 | 4 | 71% | -71% | 315 |
| 114 | | | | | | 74% | -67% | 318 |
| 115 | 58 | | | | | 77% | -63% | 321 |
| 116 | | | | | | 80% | -60% | 323 |
| 117 | 59 | 30 | | | | 83% | -56% | 326 |
| 118 | | | | | | 86% | -51% | 329 |
| 119 | 60 | | | | | 88% | -47% | 332 |
| 120 | | | | | | 90% | -43% | 335 |
| 121 | 61 | 31 | 16 | | | 92% | -38% | 338 |
| 122 | | | | | | 94% | -34% | 340 |
| 123 | 62 | | | | | 96% | -29% | 343 |
| 124 | | | | | | 97% | -24% | 346 |
| 125 | 63 | 32 | | | | 98% | -20% | 349 |
| 126 | | | | | | 99% | -15% | 352 |
| 127 | 64 | | | | | 100% | -10% | 354 |
| 128 | | | | | | 100% | -5% | 357 |

8.3.6 nRESET, nENBL, and nSLEEP Operation

The nRESET pin, when driven active low, resets internal logic, and resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while nRESET is active.

The nENBL pin is used to control the output drivers and enable/disable operation of the indexer. When nENBL is low, the output H-bridges are enabled, and rising edges on the STEP pin are recognized. When nENBL is high, the H-bridges are disabled, the outputs are in a high-impedance state, and the STEP input is ignored.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before applying a STEP input, to allow the internal circuitry to stabilize. Note that nRESET and nENBL have internal pulldown resistors of approximately 100 k Ω . The nSLEEP pin has an internal pulldown resistor of 1 M Ω . nSLEEP and nRESET signals need to be driven to logic high for device operation.

8.3.7 Protection Circuits

The DRV8825 is fully protected against undervoltage, overcurrent, and overtemperature events.

8.3.7.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device remains disabled until either nRESET pin is applied, or VM is removed and reapplied.

Overcurrent conditions on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or xVREF voltage.

8.3.7.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. After the die temperature has fallen to a safe level, operation automatically resumes.

8.3.7.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the UVLO threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_(VMx) rises above the UVLO threshold.

8.4 Device Functional Modes

8.4.1 STEP/DIR Interface

The STEP/DIR interface provides a simple method for advancing through the indexer table. For each rising edge on the STEP pin, the indexer travels to the next state in the table. The direction it moves in the table is determined by the input to the DIR pin. The signals applied to the STEP and DIR pins should not violate the timing diagram specified in [Figure 1](#).

8.4.2 Microstepping

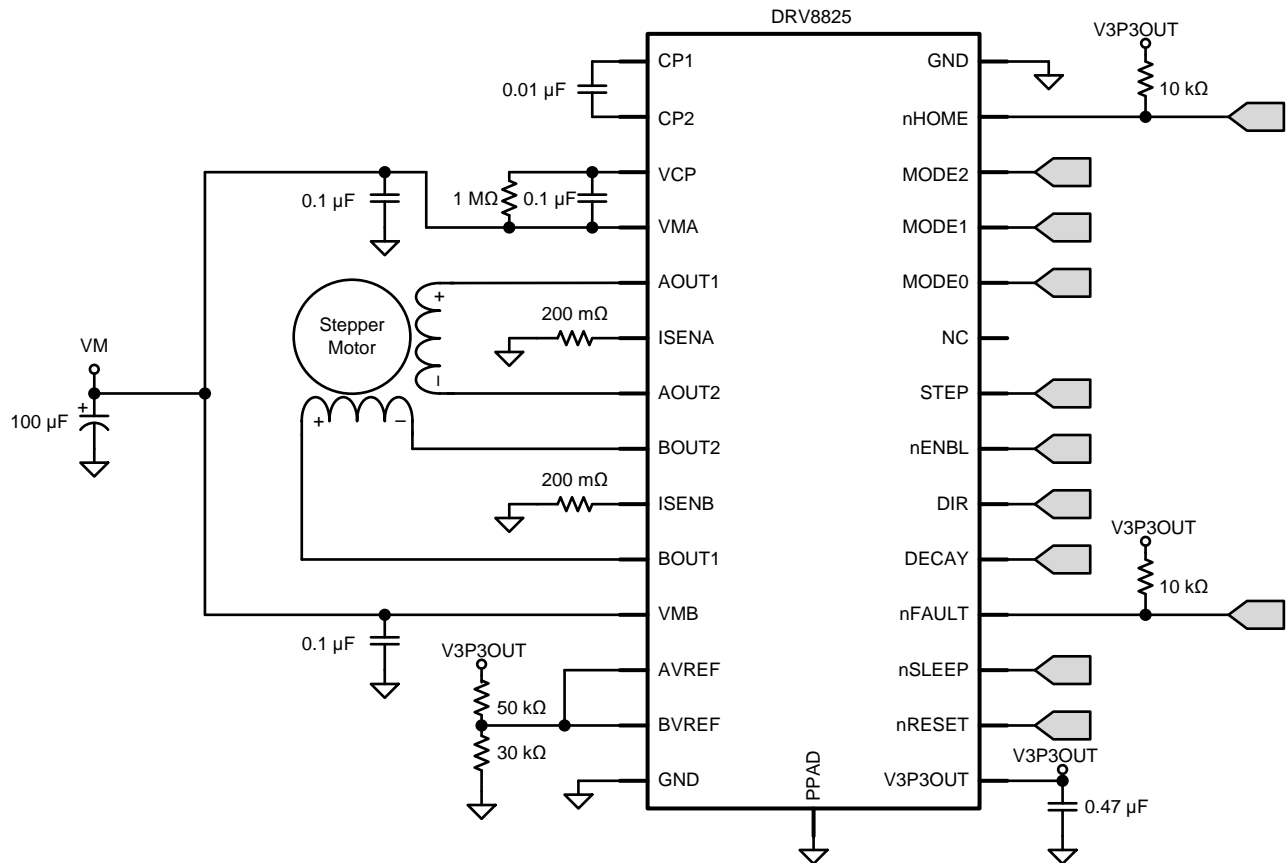
The microstepping indexer allows for a variety of stepping configurations. The state of the indexer is determined by the configuration of the three MODE pins (refer to [Table 1](#) for configuration options). The DRV8825 supports full step up to 1/32 microstepping.

9 Application and Implementation

9.1 Application Information

The DRV8825 is used in bipolar stepper control. The microstepping motor driver provides additional precision and a smooth rotation from the stepper motor. The following design is a common application of the DRV8825.

9.2 Typical Application



9.2.1 Design Requirements

| Design Parameter | Reference | Example Value |
|----------------------------|-----------------|-------------------|
| Supply Voltage | VM | 24 V |
| Motor Winding Resistance | RL | 3.9 Ω |
| Motor Winding Inductance | IL | 2.9 mH |
| Motor Full Step Angle | θ_{step} | 1.8°/step |
| Target Microstepping Level | nm | 8 µsteps per step |
| Target Motor Speed | v | 120 rpm |
| Target Full-Scale Current | IFS | 1.25 A |

9.2.2 Detailed Design Procedure

9.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8825 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor startup speed is too high, the motor will not spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{\text{step}} \left(\frac{\mu\text{steps}}{\text{second}} \right) = \frac{v \left(\frac{\text{rotations}}{\text{minute}} \right) \times 360 \left(\frac{^\circ}{\text{rotation}} \right) \times n_m \left(\frac{\mu\text{steps}}{\text{step}} \right)}{60 \left(\frac{\text{seconds}}{\text{minute}} \right) \times \theta_{\text{step}} \left(\frac{^\circ}{\text{step}} \right)} \quad (2)$$

$$f_{\text{step}} \left(\frac{\mu\text{steps}}{\text{second}} \right) = \frac{120 \left(\frac{\text{rotations}}{\text{minute}} \right) \times 360 \left(\frac{^\circ}{\text{rotation}} \right) \times 8 \left(\frac{\mu\text{steps}}{\text{step}} \right)}{60 \left(\frac{\text{seconds}}{\text{minute}} \right) \times 1.8 \left(\frac{^\circ}{\text{step}} \right)} \quad (3)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8825, the microstepping level is set by the MODE pins and can be any of the settings in [Table 1](#). Higher microstepping will mean a smoother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

9.2.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the $x\text{VREF}$ analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8825 is set for 5 V/V.

$$I_{\text{FS}} \text{ (A)} = \frac{x\text{VREF (V)}}{A_v \times R_{\text{SENSE}} \text{ (}\Omega\text{)}} = \frac{x\text{VREF (V)}}{5 \times R_{\text{SENSE}} \text{ (}\Omega\text{)}} \quad (4)$$

To achieve $I_{\text{FS}} = 1.25 \text{ A}$ with R_{SENSE} of 0.2Ω , $x\text{VREF}$ should be 1.25 V .

9.2.2.3 Decay Modes

The DRV8825 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8825 will place the winding in one of the three decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time, t_{BLANK} , defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK} , so the winding current may overshoot the trip level.

9.2.3 Application Curves

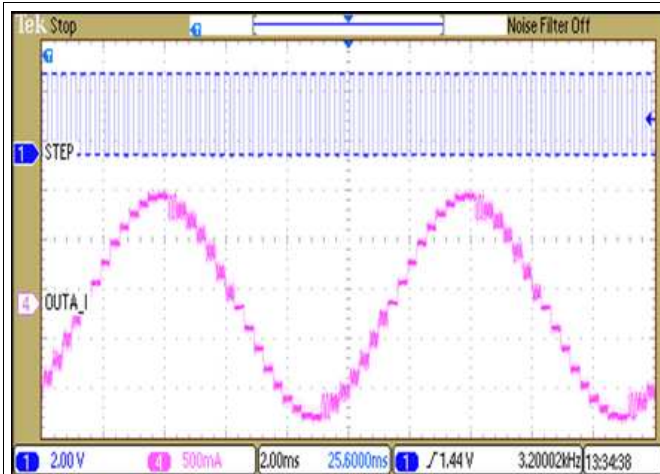


Figure 8. Microstepping Current (Phase A) vs STEP Input, Mixed Decay

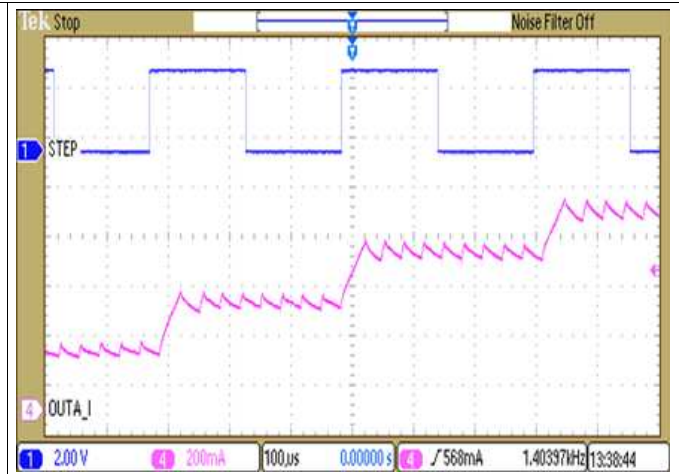


Figure 9. Microstepping Current (Phase A) vs STEP Input, Slow Decay on Increasing Steps

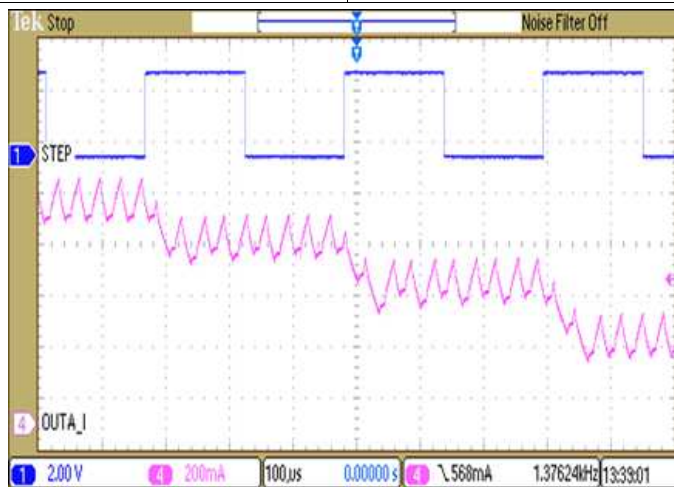


Figure 10. Microstepping Current (Phase A) vs STEP Input, Mixed Decay on Decreasing Steps

10 Power Supply Recommendations

The DRV8825 is designed to operate from an input voltage supply (VMx) range between 8.2 and 45 V. Two 0.1- μ F ceramic capacitors rated for VMx must be placed as close as possible to the VMA and VMB pins respectively (one on each pin). In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

10.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. You should size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

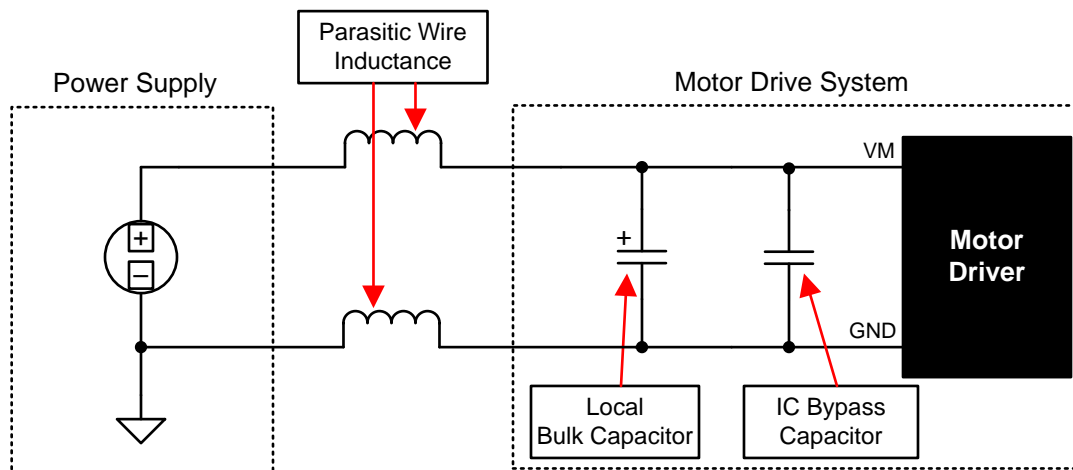


Figure 11. Setup of Motor Drive System With External Power Supply

10.2 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8825. It is okay for digital input signals to be present before VMx is applied. After VMx is applied to the DRV8825, it begins operation based on the status of the control pins.

11 Layout

11.1 Layout Guidelines

The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1- μF rated for VMx. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

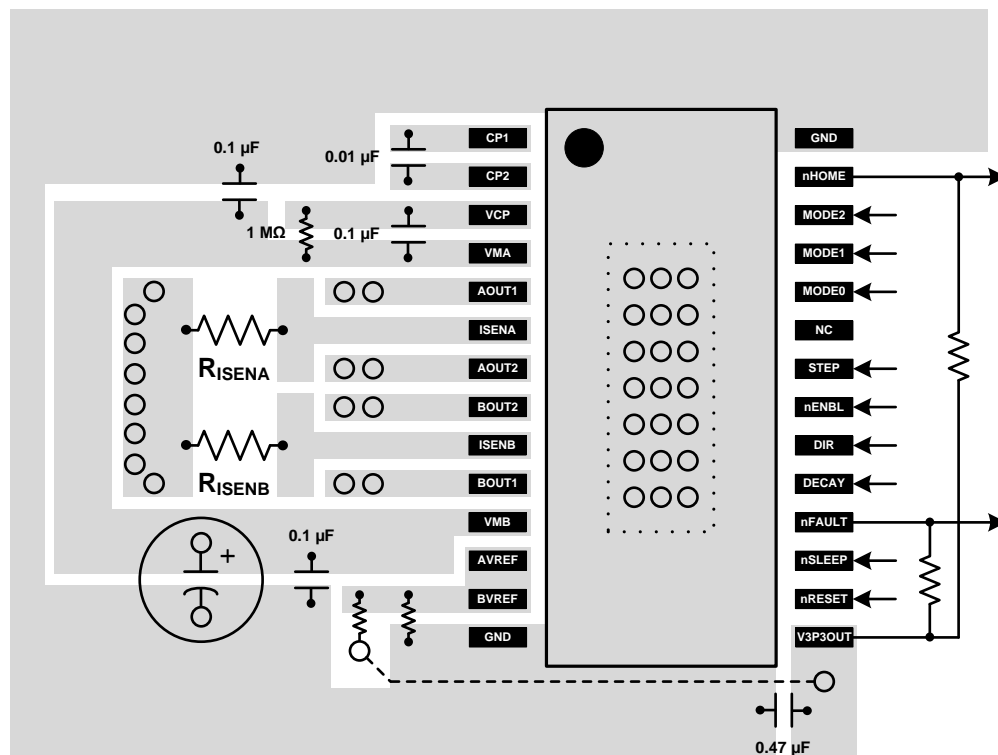
The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8825.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. TI recommends a value of 0.01- μF rated for VMx. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. TI recommends a value of 0.1- μF rated for 16 V. Place this component as close to the pins as possible. Also, place a 1-M Ω resistor between VCP and VMA.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible

11.2 Layout Example



11.3 Thermal Protection

The DRV8825 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.1 Power Dissipation

Power dissipation in the DRV8825 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by [Equation 5](#).

Thermal Protection (continued)

$$P_{TOT} = 4 \times R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (5)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

11.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report [SLMA002](#), "PowerPAD™ Thermally Enhanced Package" and TI application brief [SLMA004](#), *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. It can be seen that the heatsink effectiveness increases rapidly to about 20 cm², then levels off somewhat for larger areas.

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DRV8825PWP | ACTIVE | HTSSOP | PWP | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8825 | Samples |
| DRV8825PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8825 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV8825PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV8825PWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |

MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE

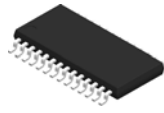


4073225-6/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

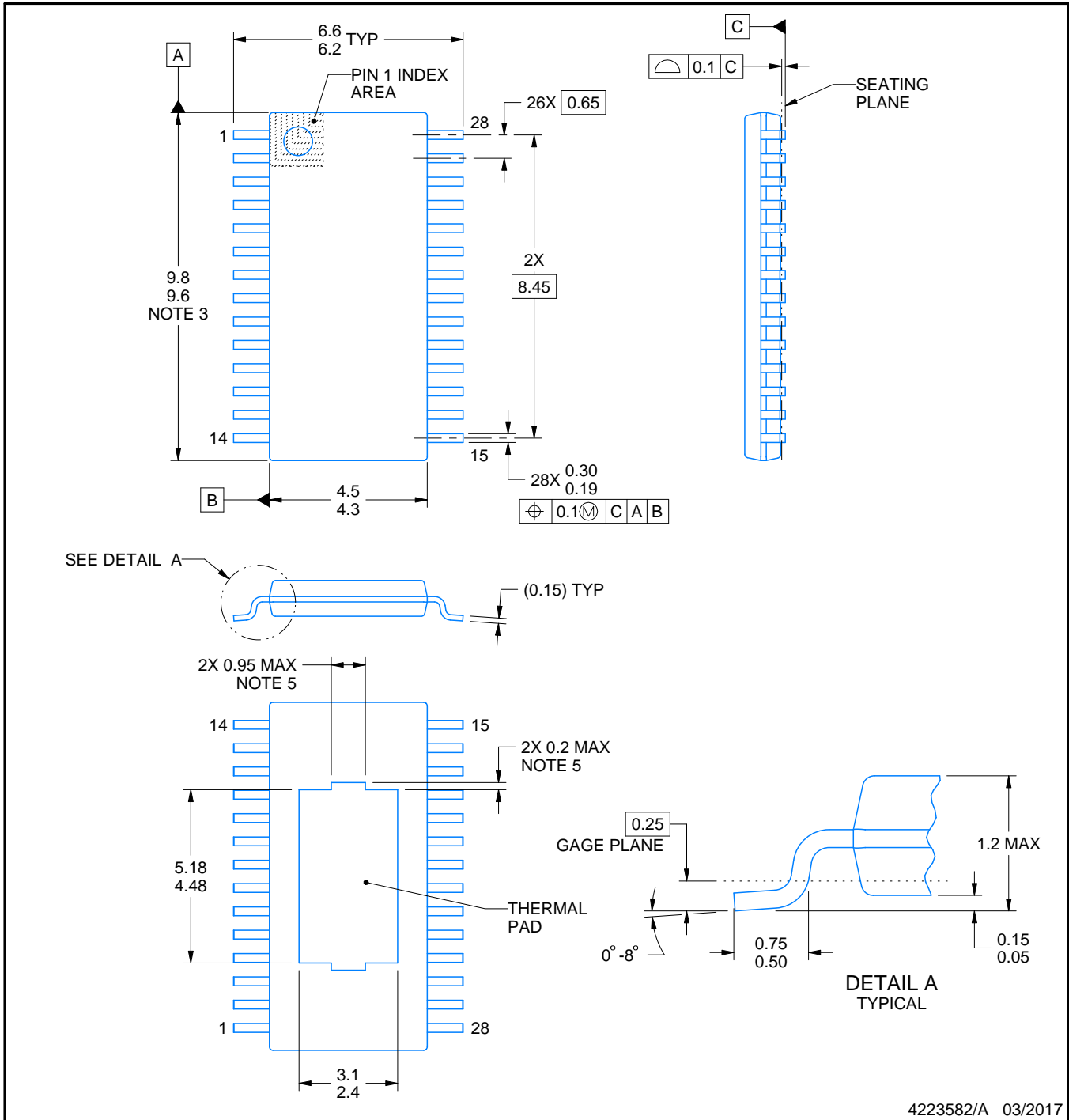
PWP0028C



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223582/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

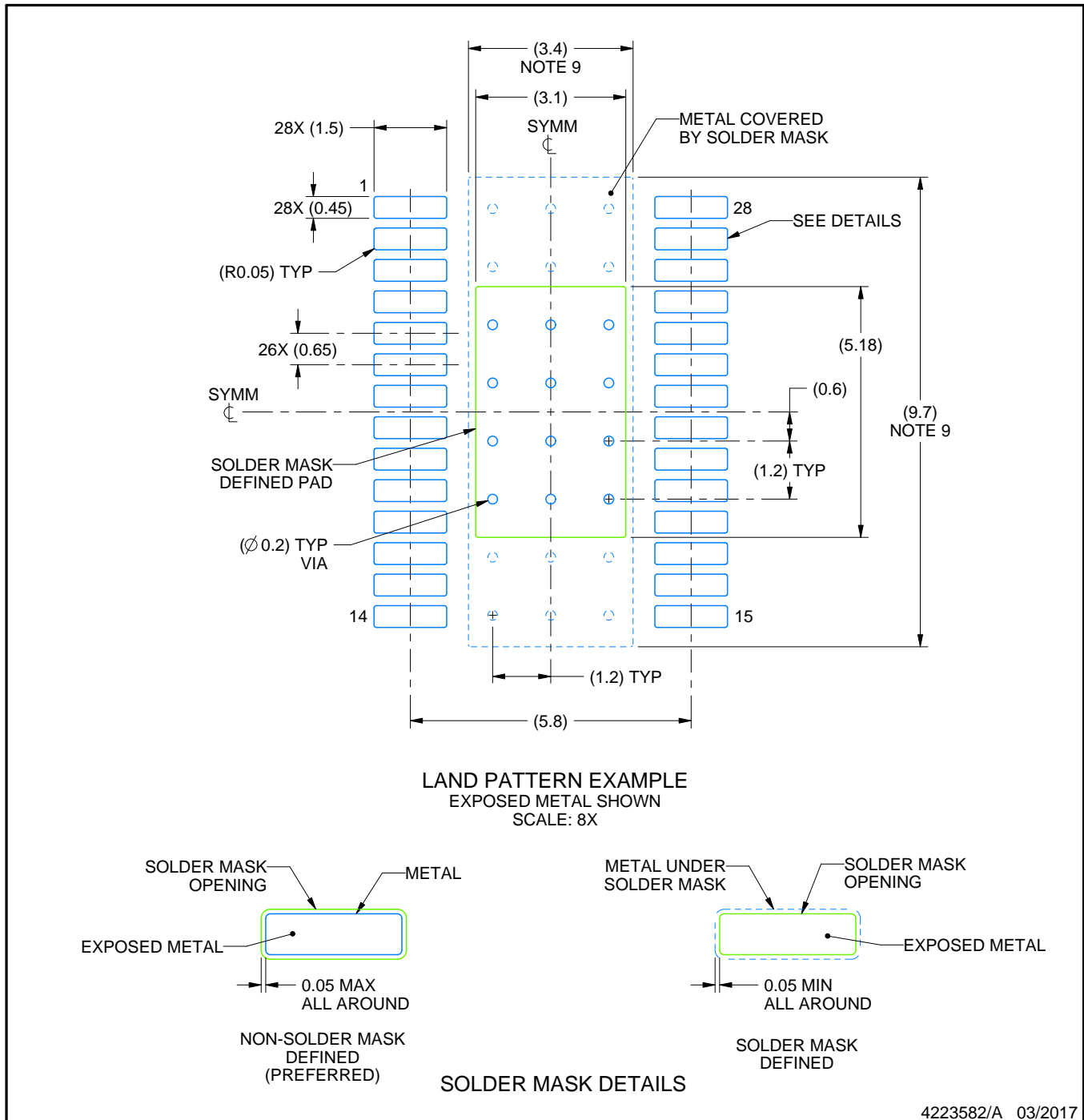
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

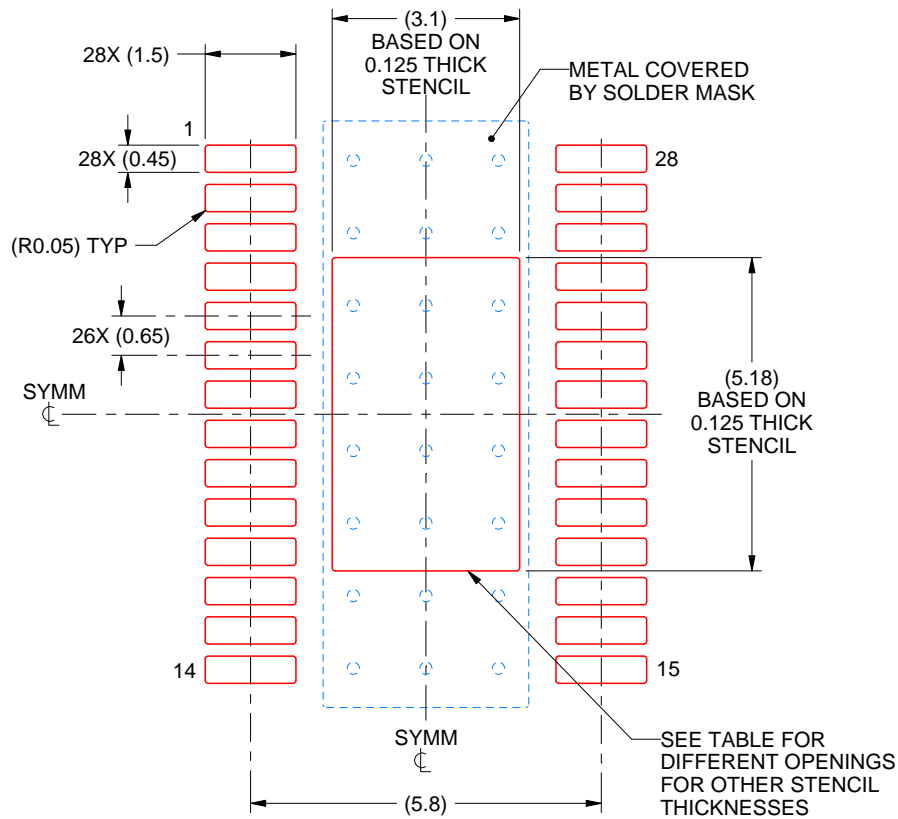
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- Size of metal pad may vary due to creepage requirement.
- Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 3.47 X 5.79 |
| 0.125 | 3.10 X 5.18 (SHOWN) |
| 0.15 | 2.83 X 4.73 |
| 0.175 | 2.62 X 4.38 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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