



DAC8043

CMOS 12-Bit Serial Input Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT ACCURACY IN 8-PIN MINI-DIP AND 8-PIN SOIC
- FAST 3-WIRE SERIAL INTERFACE
- LOW INL AND DNL: $\pm 1/2$ LSB max
- GAIN ACCURACY TO ± 1 LSB max
- LOW GAIN TEMPCO: 5ppm/ $^{\circ}$ C max
- OPERATES WITH +5V SUPPLY
- TTL/CMOS COMPATIBLE
- ESD PROTECTED

APPLICATIONS

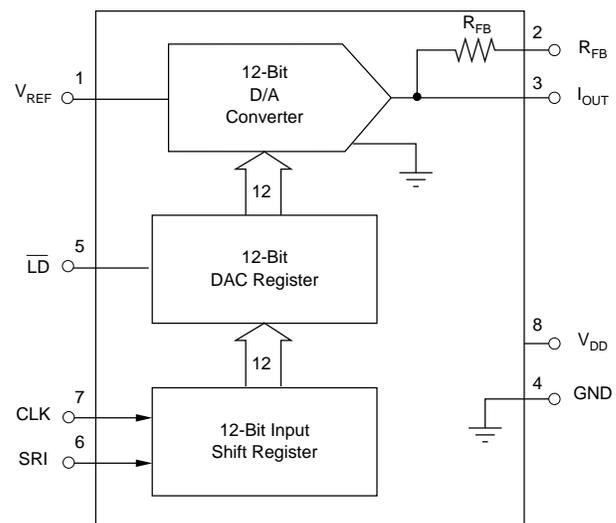
- AUTOMATIC CALIBRATION
- MOTION CONTROL
- MICROPROCESSOR CONTROL SYSTEMS
- PROGRAMMABLE AMPLIFIER/ ATTENUATORS
- DIGITALLY CONTROLLED FILTERS

DESCRIPTION

The DAC8043 is a 12-bit current output multiplying digital-to-analog converter (DAC) that is packaged in a space saving surface mount 8-pin SOIC and an 8-pin Mini-DIP. Its 3-wire serial interface saves additional circuit board space which results in low power dissipation. When used with microprocessors having a serial port, the DAC8043 minimizes the digital noise feedthrough from its input to output. The serial port can be used as a dedicated analog bus and kept inactive while the DAC8043 is in use. Serial interfacing reduces the complexity of opto or transformer isolation applications.

The DAC8043 contains a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial input (SRI) data is clocked into the input register on the rising edge of the clock (CLK) pulse. When the new data word had been clocked in, it is loaded into the DAC register by taking the $\overline{\text{LD}}$ input low. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043 operates from a single +5V power supply which makes the DAC8043 an ideal low power, small size, high performance solution for several applications.



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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At $V_{DD} = +5V$; $V_{REF} = +10V$; $I_{OUT} = GND = 0V$; $T_A =$ Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8043P, U			DAC8043PC, UC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution	N		12			12			Bits
Nonlinearity ⁽¹⁾	INL				±1			±1/2	LSB
Differential Nonlinearity ⁽²⁾	DNL				±1			±1/2	LSB
Gain Error ⁽³⁾	FSE	$T_A = +25^\circ C$ $T_A =$ Full Temp Range			±2			±1	LSB
Gain Tempco ⁽⁵⁾	TC_{FSE}				±2			±2	LSB
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD} = \pm 5\%$ $T_A = +25^\circ C$ $T_A =$ Full Temp Range		±0.0006	±0.002		±0.0006	±0.002	ppm/°C
Output Leakage Current ⁽⁴⁾	I_{LKG}				±5			±5	nA
Zero Scale Error ^(7, 12)	I_{ZSE}	$T_A = +25^\circ C$ $T_A =$ Full Temp Range			±100			±25	nA
Input Resistance ⁽⁸⁾	R_{IN}		7	11	15	7	11	15	kΩ
AC PERFORMANCE									
Output Current Settling Time ^(5, 6)	t_S	$T_A = +25^\circ C$		0.25	1		0.25	1	μs
Digital-to-Analog Glitch Energy ^(5, 10)	Q	$V_{REF} = 0V$ $I_{OUT} =$ Load = 100Ω $C_{EXT} = 13pF$		2	20		2	20	nVs
Feedthrough Error ^(5, 11) (V_{REF} to I_{OUT})	FT	DAC Register Loaded Alternately with all 0s and all 1s $V_{REF} = 20Vp-p$ at $f = 10kHz$ Digital Input = 0000 0000 0000		0.7	1		0.7	1	mVp-p
Total Harmonic Distortion ⁽⁵⁾	THD	$T_A = +25^\circ C$ $V_{REF} = 6V_{RMS}$ at 1kHz DAC Register Loaded with all 1s		-85			-85		dB
Output Noise Voltage Density ^(5, 13)	e_N	10Hz to 100kHz Between R_{FB} and I_{OUT}			17			17	nV/√Hz
DIGITAL INPUTS									
Digital Input High	V_{IH}		2.4			2.4			V
Digital Input Low	V_{IL}				0.8			0.8	V
Input Leakage Current ⁽⁹⁾	I_{IL}	$V_{IN} = 0V$ to +5V			±1			±1	μA
Input Capacitance ^(5, 11)	C_{IN}	$V_{IN} = 0V$			8			8	pF
ANALOG OUTPUTS									
Output Capacitance ⁽⁵⁾	C_{OUT}	Digital Inputs = V_{IH} Digital Inputs = V_{IL}			110 80			110 80	pF pF
TIMING CHARACTERISTICS^(5, 14)									
Data Setup Time	t_{DS}	$T_A =$ Full Temperature Range	40			40			ns
Data Hold Time	t_{DH}	$T_A =$ Full Temperature Range	80			80			ns
Clock Pulse Width High	t_{CH}	$T_A =$ Full Temperature Range	90			90			ns
Clock Pulse Width Low	t_{CL}	$T_A =$ Full Temperature Range	120			120			ns
Load Pulse Width	t_{LD}	$T_A =$ Full Temperature Range	120			120			ns
LSB Clock into Input Register to Load DAC Register Time	t_{ASB}	$T_A =$ Full Temperature Range	0			0			ns
POWER SUPPLY									
Supply Voltage	V_{DD}		4.75	5	5.25	4.75	5	5.25	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}			500 100			500 100	μA μA

NOTES: (1) ±1/2 LSB = ±0.012% of Full Scale. (2) All grades are monotonic to 12-bits over temperature. (3) Using internal feedback resistor. (4) Applies to I_{OUT} . All digital inputs = 0V. (5) Guaranteed by design and not tested. (6) I_{OUT} Load = 100Ω, $C_{EXT} = 13pF$, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_S = propagation delay (t_{PD}) + 9τ where τ = measured time constant of the final RC decay. (7) $V_{REF} = +10V$, all digital inputs = 0V. (8) Absolute temperature coefficient is less than ±50ppm/°C. (9) Digital inputs are CMOS gates: I_{IN} is typically 1nA at +25°C. (10) $V_{REF} = 0V$, all digital inputs = 0V to V_{DD} or V_{DD} to 0V. (11) All digital inputs = 0V. (12) Calculated from worst case R_{REF} : I_{ZSE} (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096) / V_{REF}$. (13) Calculations from $e_N = \sqrt{4K TRB}$ where: K = Boltzmann constant, J/°K, R = resistance, Ω. T = Resistor temperature, °K, B = bandwidth, Hz. (14) Tested at $V_{IN} = 0V$ or V_{DD} .

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	0V, +7V
V_{REF} to GND	$\pm 25V$
V_{RFB} to GND	$\pm 25V$
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 3)	-0.3 V to V_{DD}
Operating Temperature Range	
AD	0°C to +70°C
P, PC, U, UC	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
$\theta_{JA}^{(1)}$	
U Package	+100°C/W
P Package	+96°C/W
θ_{JC}	
U Package	+42°C/W
P Package	+37°C/W

NOTE: (1) θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for PDIP packages.

CAUTION: 1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2). 2. The digital control inputs are ESD protected: however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. 3. Use proper anti-static handling procedures. 4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ORDERING INFORMATION

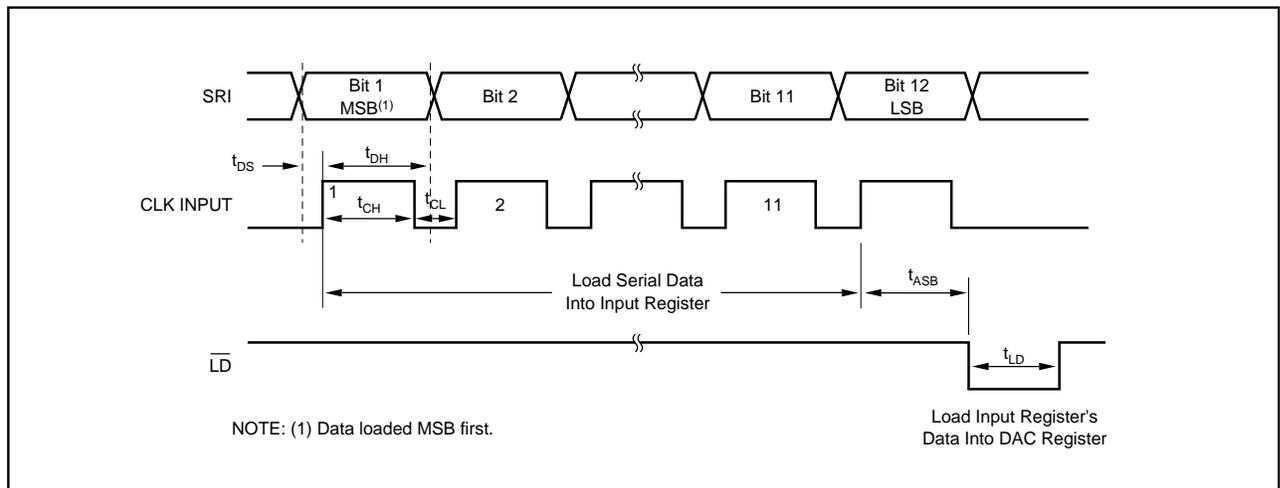
MODEL	INL	TEMPERATURE RANGE	PACKAGE
DAC8043P	1LSB	-40°C to +85°C	8-pin Plastic DIP
DAC8043PC	1/2LSB	-40°C to +85°C	8-pin Plastic DIP
DAC8043U	1LSB	-40°C to +85°C	8-pin SOIC
DAC8043UC	1/2LSB	-40°C to +85°C	8-pin SOIC

PACKAGING INFORMATION

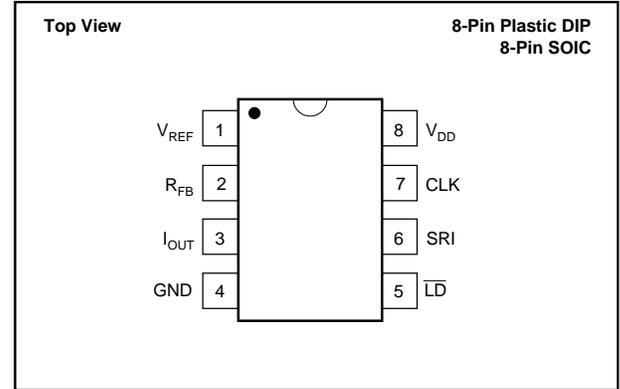
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
DAC8043P	8-Pin PDIP	006
DAC8043PC	8-Pin PDIP	006
DAC8043U	8-Pin SOIC	182
DAC8043UC	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

WRITE CYCLE TIMING DIAGRAM



PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

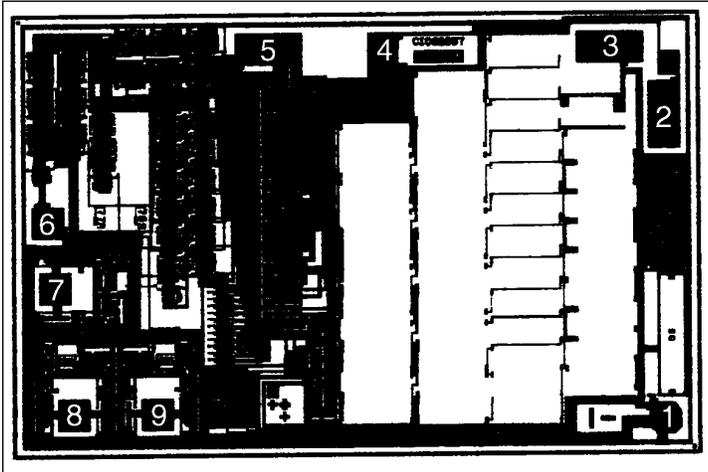
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Digital Inputs: All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed and has been tested to withstand five 2500V positive and negative discharges (100pF in series with 1500 Ω) applied to each digital input.

Analog Pins: Each analog pin has been tested to Burr-Brown's analog ESD test consisting of five 1000V positive and negative discharges (100pF in series with 1500 Ω) applied to each pin. V_{REF} and R_{FB} show some sensitivity.

DICE INFORMATION



DAC8043 DIE TOPOGRAPHY

PAD	FUNCTION
1	V _{DD}
2	V _{REF}
3	R _{FB}
4	I _{OUT}
5	AGND
6	DGND
7	L _D
8	SRI
9	CLK

Substrate Bias: +V_{DD}.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	70x 110 ±5	1.78 x 2.79 ±0.13
Die Thickness	14 ±3	0.35 ±3
Min. Pad Size	4 x 4	0.1 x 0.1
Metallization	Aluminum	
Backing	Chrome Silver	

WAFER TEST LIMITS

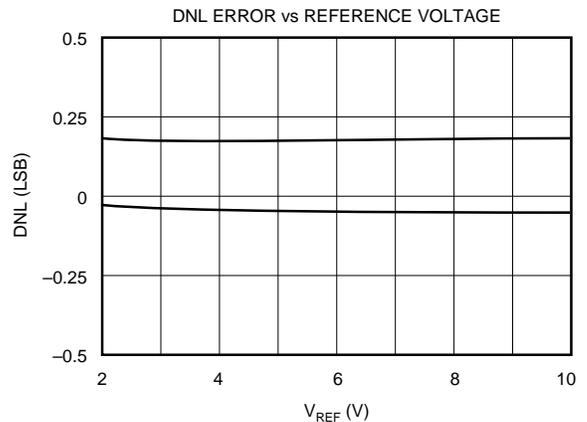
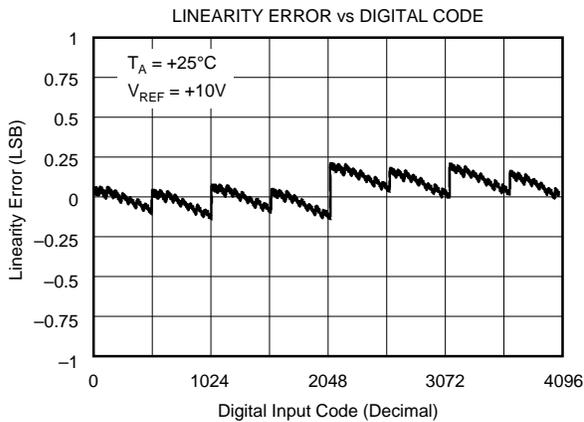
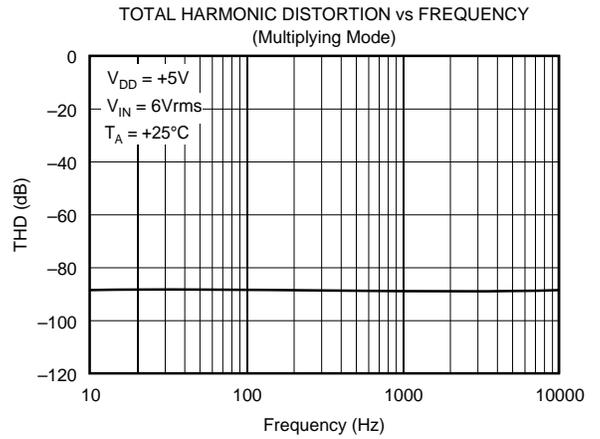
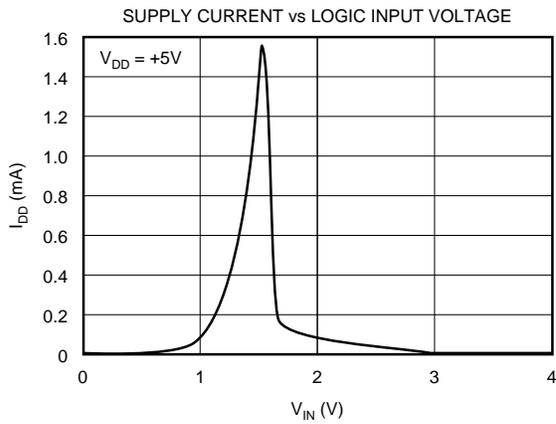
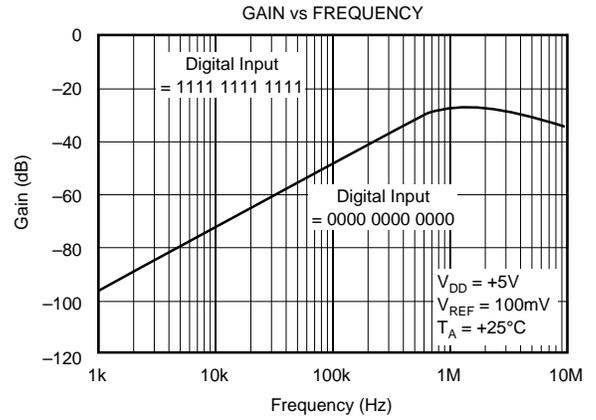
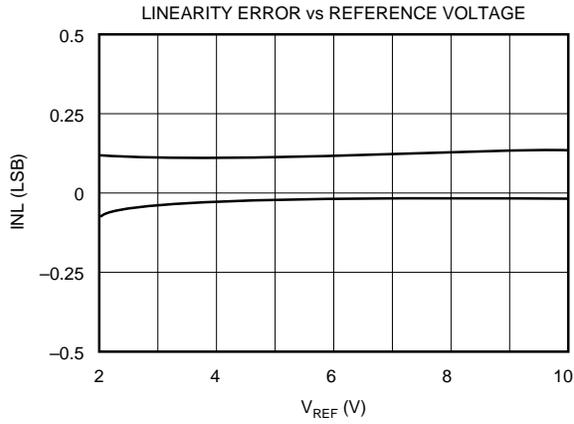
At V_{DD} = +5V; V_{REF} = +10V; I_{OUT} = GND = 0V; T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	LIMIT	DAC8043 UNITS
STATIC ACCURACY				
Resolution	N		12	Bits min
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Gain Error	G _{FSE}	Using Internal Feedback Resistor	±2	LSB max
Power Supply Rejection Ratio	PSRR	ΔV _{DD} = ±5%	±0.002	%/% max
Output Leakage Current (I _{OUT})	I _{LKG}	Digital Inputs = V _{IL}	±5	nA max
REFERENCE INPUT				
Input Resistance	R _{IN}		7/15	kΩ min/max
DIGITAL INPUTS				
Digital Input HIGH	V _{IH}	V _{IN} = 0V to V _{DD}	2.4	V min
Digital Input LOW	V _{IL}		0.8	V max
Input Leakage Current	I _{IL}		±1	μA max
POWER SUPPLY				
Supply Current	I _{DD}	Digital Inputs = V _{IH} or V _{IL}	500	μA max
		Digital Inputs = 0V to V _{DD}	100	μA max

NOTE: Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CURVES

At $V_{DD} = +5V$; $V_{REF} = +10V$; $I_{OUT} = GND = 0V$; $T_A = \text{Full Temperature Range}$ specified under Absolute Maximum Ratings unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term, also known as end point linearity or integral linearity, describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line, after zero and full scale errors have been adjusted to zero.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output when the input code changes by 1LSB. A differential nonlinearity specification of 1LSB maximum guarantees monotonicity.

GAIN ERROR

Gain error is the difference between the full-scale DAC output and the ideal value. The ideal full scale output value for the DAC8043 is $-(4095/4096)V_{REF}$. Gain error may be adjusted to zero using external trims as shown in Figure 4.

OUTPUT LEAKAGE CURRENT

The current which appears at I_{OUT} with the DAC loaded with all zeros.

OUTPUT CAPACITANCE

The parasitic capacitance measured from I_{OUT} to GND.

FEEDTHROUGH ERROR

The AC output error due to capacitive coupling from V_{REF} to I_{OUT} with the DAC loaded with all zeros.

OUTPUT CURRENT SETTling TIME

The time required for the output current to settle to within $\pm 0.01\%$ of final value for a full scale step.

DIGITAL-TO-ANALOG GLITCH ENERGY

The integrated area of the glitch pulse measured in nanovolt-seconds. The key contributor to digital-to-analog glitch is charge injected by digital logic switching transients.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of a DAC8043. The current from the V_{REF} pin is switched between I_{OUT} and GND by 12 single-pole double-throw CMOS switches. This main-

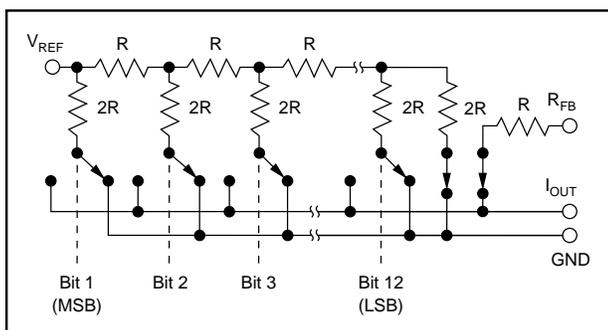


FIGURE 1. Simplified Circuit Diagram for the DAC.

tains a constant current in each leg of the ladder regardless of the input code. The input resistance at V_{REF} is therefore constant and can be driven by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to $\pm 20V$.

A CMOS switch transistor, included in series with the ladder terminating resistor and in series with the feedback resistor, R_{FB} , compensates for the temperature drift of the ON resistance of the ladder switches.

Figure 2 shows an equivalent circuit for the DAC. C_{OUT} is the output capacitance due to the N-channel switches and varies from about 80pF to 110pF with digital input code. The current source I_{LKG} is the combination of surface and junction leakages to the substrate. I_{LKG} approximately doubles every $10^\circ C$. R_O is the equivalent output resistance of the D/A and it varies with input code.

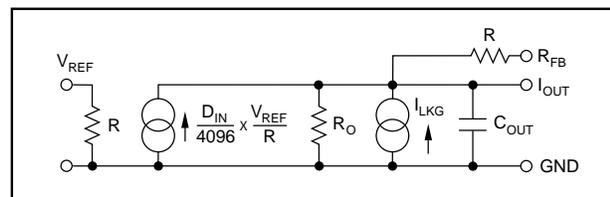


FIGURE 2. Equivalent Circuit for the DAC.

INSTALLATION

ESD PROTECTION

All digital inputs of the DAC8043 incorporate on-chip ESD protection circuitry. This protection is designed to withstand 2.5kV (using the Human Body Model, 100pF and 1500 Ω). However, industry standard ESD protection methods should be used when handling or storing these components. When not in use, devices should be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket potential before devices are removed.

POWER SUPPLY CONNECTIONS

The DAC8043 is designed to operate on $V_{DD} = +5V \pm 5\%$. For optimum performance and noise rejection, power supply decoupling capacitors C_D should be added as shown in the application circuits. These capacitors (1 μF tantalum recommended) should be located close to the D/A. Output op amp analog common (+ input) should be connected as near to the GND pins of the DAC8043 as possible.

WIRING PRECAUTIONS

To minimize AC feedthrough when designing a PC board, care should be taken to minimize capacitive coupling between the V_{REF} lines and the I_{OUT} lines. Coupling from any of the digital control or data lines might degrade the glitch performance. Solder the DAC8043 directly into the PC board without a socket. Sockets add parasitic capacitance (which can degrade AC performance).

AMPLIFIER OFFSET VOLTAGE

The output amplifier used with the DAC8043 should have low input offset voltage to preserve the transfer function linearity. The voltage output of the amplifier has an error component which is the offset voltage of the op amp multiplied by the “noise gain” of the circuit. This “noise gain” is equal to $(R_F/R_O + 1)$ where R_O is the output impedance of the D/A I_{OUT} terminal and R_F is the feedback network impedance. The nonlinearity occurs due to the output impedance varying with code. If the 0 code case is excluded (where $R_O = \text{infinity}$), the R_O will vary from R to $3R$ providing a “noise gain” variation between $4/3$ and 2 . In addition, the variation of R_O is nonlinear with code, and the largest steps in R_O occur at major code transitions where the worst differential nonlinearity is also likely to be experienced. The nonlinearity seen at the amplifier output is

$$2V_{OS} - 4V_{OS}/3 = 2V_{OS}/3.$$

Thus, to maintain good nonlinearity the op amp offset should be much less than $1/2\text{LSB}$.

UNIPOLAR CONFIGURATION

Figure 3 shows DAC8043 in a typical unipolar (two-quadrant) multiplying configuration. The analog output values

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096) = $-1/2V_{REF}$
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

TABLE I. Unipolar Output Code.

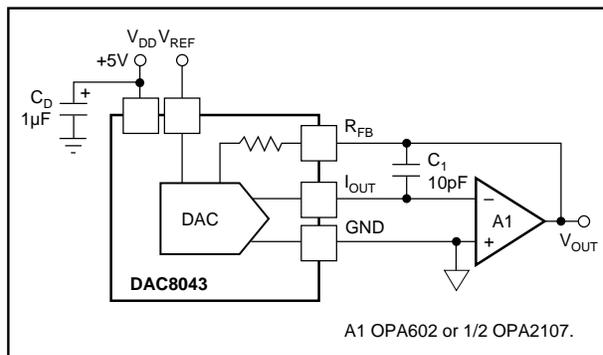


FIGURE 3. Unipolar Configuration.

versus digital input code are listed in Table I. The operational amplifiers used in this circuit can be single amplifiers such as the OPA602, or a dual amplifier such as the OPA2107. C_1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier.

If an application requires the D/A to have zero gain error, the circuit shown in Figure 4 may be used. Resistor R_2 induces a positive gain error greater than worst-case initial negative gain error. Trim resistor R_1 provides a variable negative gain error and have sufficient trim range to correct for the worst-case initial positive gain error plus the error produced by R_2 .

BIPOLAR CONFIGURATION

Figure 5 shows the DAC8043 in a typical bipolar (four-quadrant) multiplying configuration. The analog output values versus digital input code are listed in Table II.

The operational amplifiers used in this circuit can be single amplifiers such as the OPA602 or a dual amplifier such as the OPA2107. C_1 provides phase compensation to minimize settling time and overshoot when using a high speed operational amplifier. The bipolar offset resistors R_1 – R_2 should be ratio-matched to 0.01% to ensure the specified gain error performance.

DATA INPUT	ANALOG OUTPUT
MSB ↓ ↓ LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0001	$+V_{REF}$ (1/2048)
0000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Output Code.

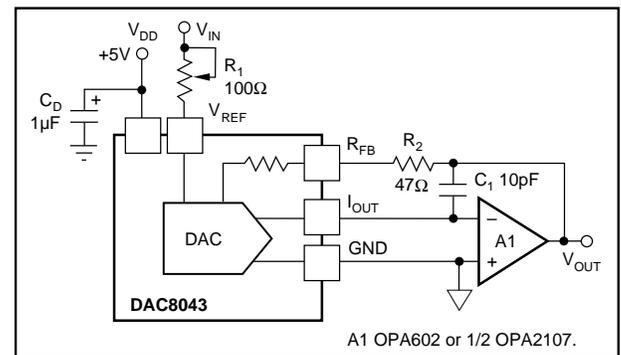


FIGURE 4. Unipolar Configuration with Gain Trim.

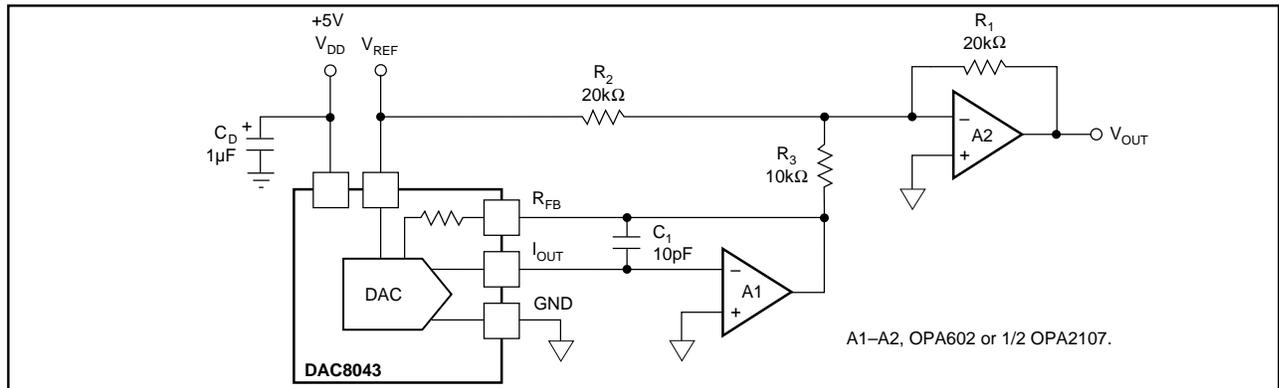
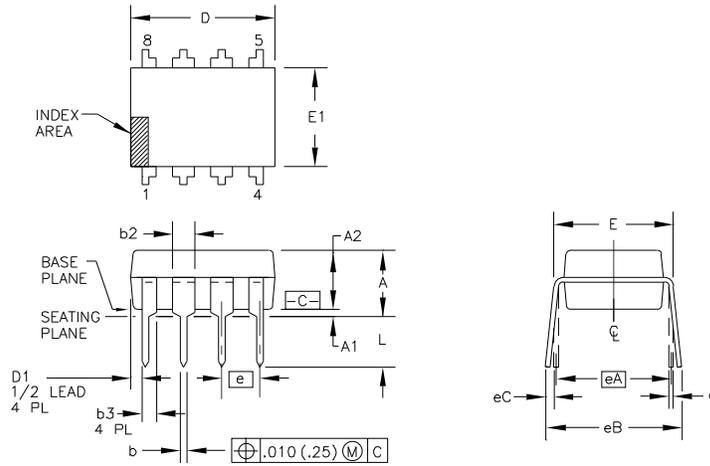


FIGURE 5. Bipolar Configuration.

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6

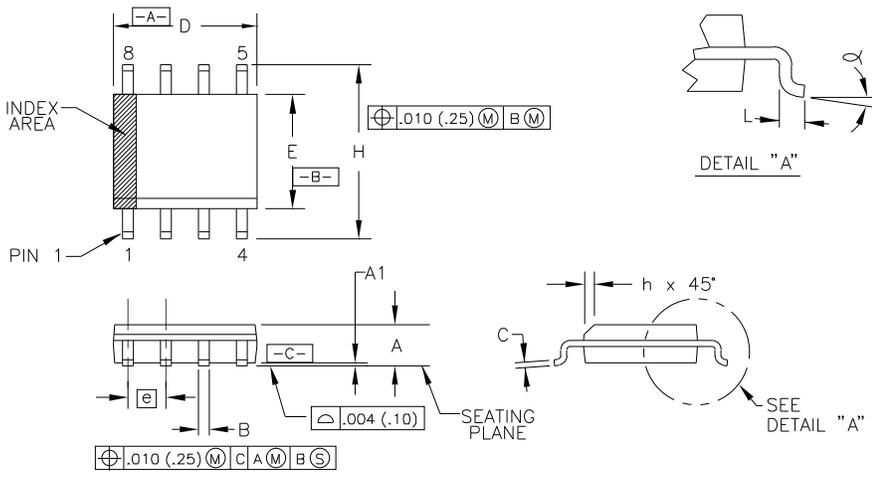
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:
 1. ALL DIMENSIONS ARE IN INCHES.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
 3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
 4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
 5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM [-C-].
 6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
 7. N IS THE MAXIMUM OF TERMINAL POSITIONS.

8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
 9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
 10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
 11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
 12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: Z2006 REV.: E
 JEDEC NUMBER: MS-001-BA

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050	BASIC	1.27	BASIC	
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
alpha	0°	8°	0°	8°	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eA	.004	.10			

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
 2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
 3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
 4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT,

A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
 5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
 6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
 7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
 8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: Z2182 REV.: G
 JEDEC NUMBER: MS-012-AA