SEEQ
Technology Incorporated

83C92C
Ethernet Transceiver

February 17, 1998

Introduction

The 83C92C is an Ethernet and Thin Net (Cheapernet) Transceiver that provides a complete Local Area Network interface for a station, with or without a transceiver cable, see Figure 1.

The 83C92C is compatible with ANSI/IEEE 802.3 and ISO 8802-3, and meets or exceeds the specification of the National Semiconductor DP8392A and DP8392B.

The 83C92C is part of a chipset manufactured by SEEQ Technology to provide the basic components for a LAN interface board. The other components include the 8005 or 80C04A Advanced Ethernet Data Link Controller (AEDLC™) and the 8020 or 8023A Manchester Code Converter (MCC™).

Note: Check for latest Data Sheet revision before starting any designs.

Call SEEQ Technology (510) 226-7400 x3051.

SEEQ Data Sheets are now on the Web, access SEEQ Home Page www.seeq.com.

Features

- ***The 83C92C is Compatible with ANSI/IEEE 802.3 and ISO 8802-3 Standards for Ethernet (10BASE5) and Thin Net (10BASE2).***
- ***Meets or exceeds all data sheet specifications of the National Semiconductor DP8392A, DP8392B DP8392C and DP8392C-1.***
- ***Squelch circuits on all signal inputs to eliminate noise.***
- ***Contains all transceiver functions on one chip, except power and DC isolation. For a complete Module Solution, refer to the EM2C data sheet.***
- ***Collision Test Generator, externally deselectable to work with any ANSI/IEEE 802.3 and ISO 8802-3 repeater.***
- ***Detects and reports network collisions in both transmit and receive modes.***
- ***Implemented with SEEQ proprietary high voltage (20V) and high performance CMOS process.***
- ***Loopback test detects network cable opens or shorts.***
- ***Power On Reset prevents transmission during power up.***
- ***Temperature Ranges,***
  • Commercial 0°C to +70°C

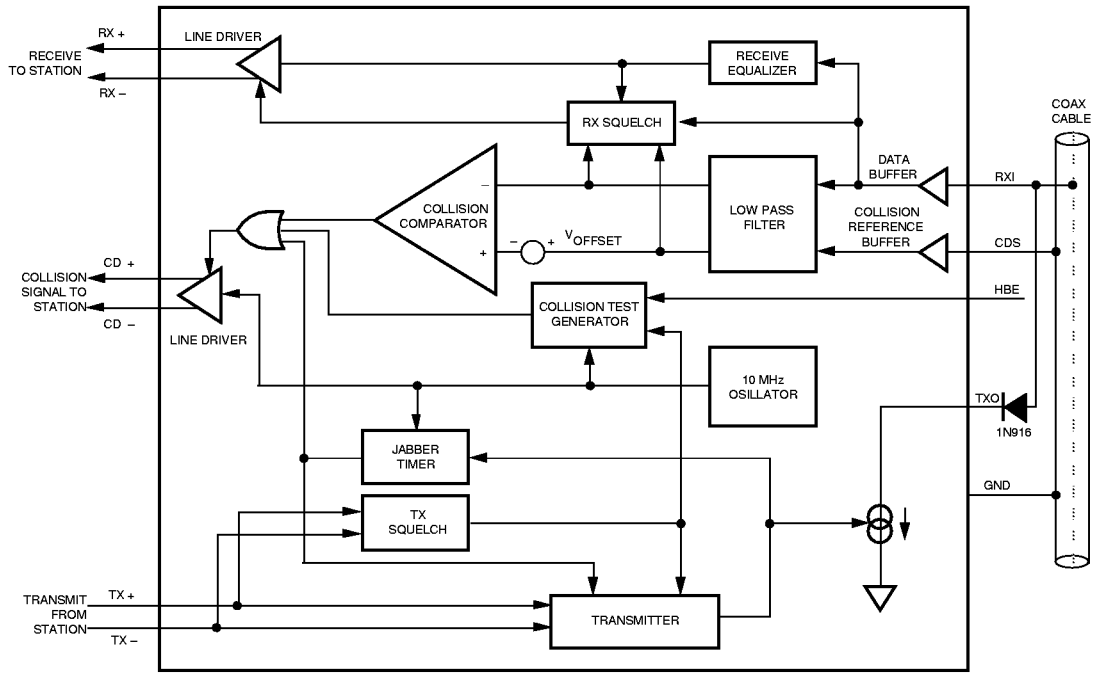

Figure 1. 83C92C Ethernet Transceiver Block Diagram

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Description

The 83C92C Ethernet Transceiver connects the station equipment to an Ethernet or Thin Net (Cheapernet) COAX cable. The 83C92C provides the drive current and wave shaping for the transmit signals. It supplies receive signal equalization, collision detection and squelch.

When used in an Ethernet LAN, the 83C92C Transceiver is mounted on the Ethernet COAX cable, and connects to the station equipment through a transceiver cable. The 83C92C may be located up to 50 meters from the station equipment.

When used for a Thin Net (Cheapernet) LAN, the 83C92C is usually mounted on the LAN adapter board in the station equipment, where it connects to the RG58 COAX through a BNC connector.

Description of the Pin Functions

(See Figure 2) Dual-In-Line

PIN #	***FUNCTION***
1 - 2	*CD± Collision Output. A balanced 10 MHz differential output to the station equipment when a collision is detected, when excessive data transmission occurs (jabber), or during the Collision Test (Heartbeat Test). These are open-source outputs with V_{EE} (–9 volts) pull down resistors, 500 ohms when operating with a 78-ohm Ethernet transceiver cable, and up to 1.5 kohms with an on-board transceiver for the Thin Net LAN cable.*

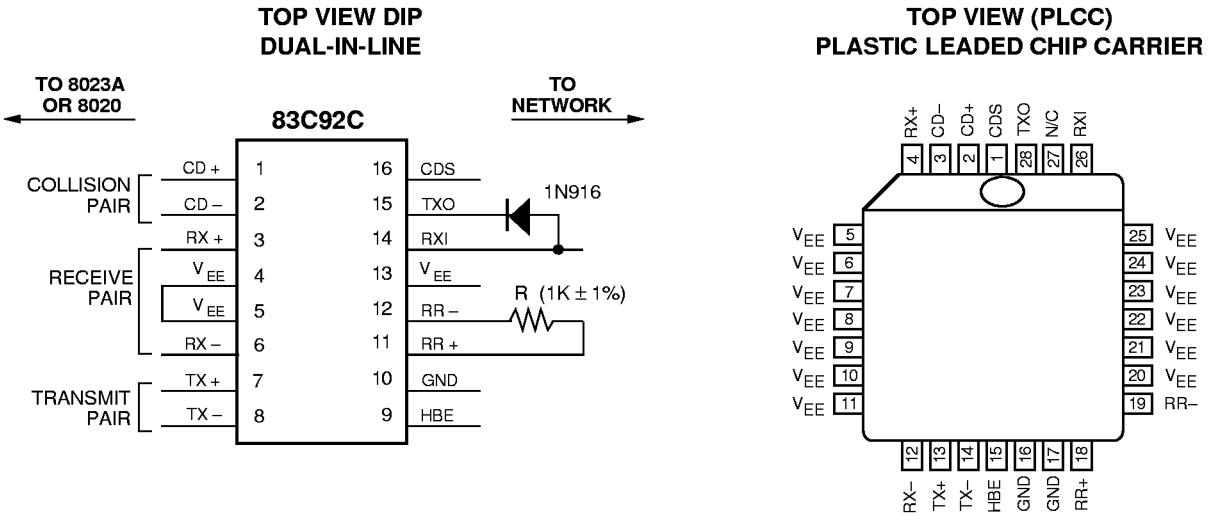


Figure 2. 83C92C Ethernet Transceiver Pin Configuration

3, 6	RX± Receive Data Output. Line Driver output from the 83C92C to the MCC Receive inputs, a balanced differential output with 500 ohm pull down resistors. These are open-source outputs with V_{EE} (–9 volts) pulldown resistors, 500 ohms when operating with a 78-ohm Ethernet transceiver cable, and up to 1.5 kohms with an onboard transceiver for the Thin Net LAN cable.
4, 5, 13	V_{EE} Negative Supply. Nominally –9 volts referenced to COAX shield ground.
7 - 8	TX± Transmit Data Input. A balanced line receiver input to the 83C92C from the MCC for transmit packets.
9	HBE Heartbeat Enable. This input enables the Collision (also called Heartbeat) Test when connected to ground or floating, and disables the test when connected to V_{EE}.
10	GND Ground. Ground is the positive supply for the 83C92C, and connects to the network COAX shield. A 0.1 microfarad ceramic decoupling capacitor must be connected across ground and V_{EE} as close to the device as possible. A DC-DC power converter provides –9 volt power for the 83C92C, and DC isolation from the station equipment to prevent ground loop current. Do not connect this ground to any station equipment power supply voltage or chassis ground, since the COAX shield must be isolated from the station equipment.
11 - 12	RR± External Resistor. To set the internal current levels, connect a 1K 1% resistor across these pins. RR– connects to V_{EE} internally.
14	RXI Network Signal Receiver. Connects to the network COAX center conductor, and receives packet data and detects the collision voltage level.
15	TXO Network Signal Transmitter. Connects to the network COAX center conductor through an external 1N916 diode[1], and transmits all signals from the MCC to the network.
16	CDS Collision Detect Sense. Connects directly to the network shield, and references the collision detection voltage level.

Description of the 83C92C Functions

The 83C92C has four main functions, as shown in the block diagram. These are the Transmitter; the Collision Detector; the Jabber Timer; and the Receiver.

The Transmitter

The Transmitter takes differential output signals from the MCC, and outputs these signals at the correct levels to the network.

The transmit signal is sent to the 83C92C via a balanced differential pair (TX±). A squelch circuit prevents the Transmitter Output from responding to noise on the TX ± pair. The Transmitter has an open-drain current driver output using the V_{EE} supply. Rise and fall times are controlled and set at 25 ns to lessen the higher harmonics. Drive current levels are set by a bandgap voltage reference and a 1K resistor installed across pins 11 and 12. An external diode should be added to reduce COAX loading and capacitance to comply with the ISO and ANSI/IEEE specifications.

NOTE

1. 1N916 diode or equivalent with low capacitance less than or equal to 1 pf value. This diode is needed for all 83C92C designs.

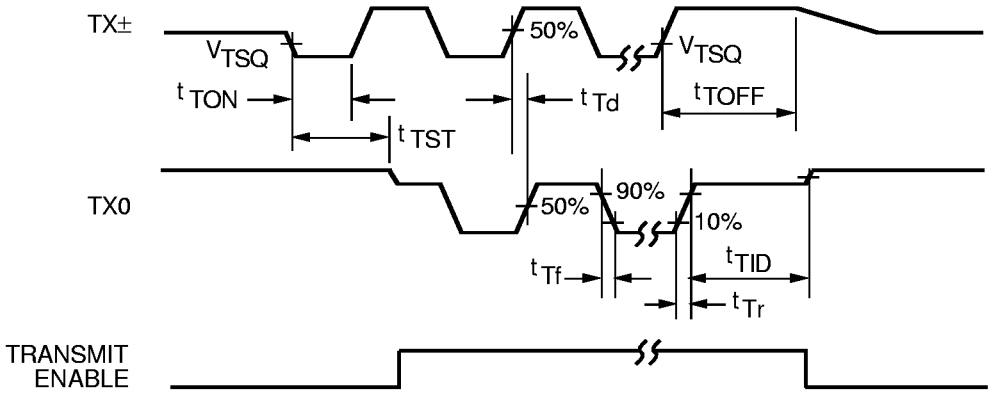


Figure 3. Transmitter Timing

The transmit squelch circuit blocks signals with pulse widths less than 15 nanoseconds, (negative-going), or with levels of less than –175 millivolts. The squelch circuits turn the Transmitter off at the end of a packet if the signal stays higher than –175 millivolts for more than 190 nanoseconds. See Figure 3, the Transmitter Timing Diagram.

The TXO signal is disabled when not transmitting to prevent noise on the network. If the COAX cable is shorted or open, no transmitted data appears on the Receiver input. This condition can be detected by the station equipment by running a loopback test.

Collision Detection

The Collision detector monitors the COAX Center Conductor and senses the voltage conditions created by a collision, where the COAX shield is used as a reference. A collision condition can be detected when two or more stations are transmitting, whether or not the local Transmitter is activated. This is called Receive Mode Collision Detection.

The detector signals a collision by sending the 10 MHz oscillator signal through the Collision Pair (CD±) to the MCC. The HeartbeatTest is performed at the end of each transmitted data packet to verify the operation of the detector.

A collision causes a –2.0 volt average DC level on the center conductor of the network cable. This level passes through a 4-pole Bessel low-pass filter for averaging. The resulting signal is measured by a voltage comparator against the threshold voltage V_{CD} of about -1.5 volts. A collision is indicated when the center conductor average level is more negative than the CDS level by the threshold V_{CD}. The line driver is enabled within 900 ns of the onset of the collision, and the 10 MHz signal is sent to the station equipment.

The HeartbeatTest is a short burst of the collision signal generated immediately after the transmission of a packet. This test enables the 10 MHz collision signal for about 1 microsecond starting about 1.1 microseconds after the end of transmission. The test can be disabled for operation with repeaters by connecting the HBE pin to V_{EE}.

The Jabber Timer

The Jabber Timer monitors the operation of the Transmitter. If the Transmitter operates continuously for more than 40 Milliseconds (typically), the Jabber Timer disables the Transmitter and enables the Collision Detector outputs. The Transmitter is automatically re-enabled after the station has been silent for 500 milliseconds.

The Receiver

The Receiver detects any signal on the COAX center conductor that triggers its squelch circuits, and sends the signal through a differential line driver to the MCC. The Receiver provides amplification and equalization; a squelch circuit prevents noise activating the Receiver circuits. See Figure 4.

The receive signal goes through a buffer with a high input impedance and low capacitance to reduce loading and reflections on the network COAX. An equalizer passes high frequencies and attenuates low frequency signals from the network, flattening the network pass band. The signal is output through a differential line driver presenting a balanced signal to the station. The line driver has 4 nanosecond rise and fall times.

A 4-pole Bessel low-pass filter provides the average DC level from the received signal. It sends this level to the Collision Comparator and RX Squelch circuits. The squelch circuit activates the Receive Line Driver only when it detects a true signal. This prevents noise triggering the receiver.

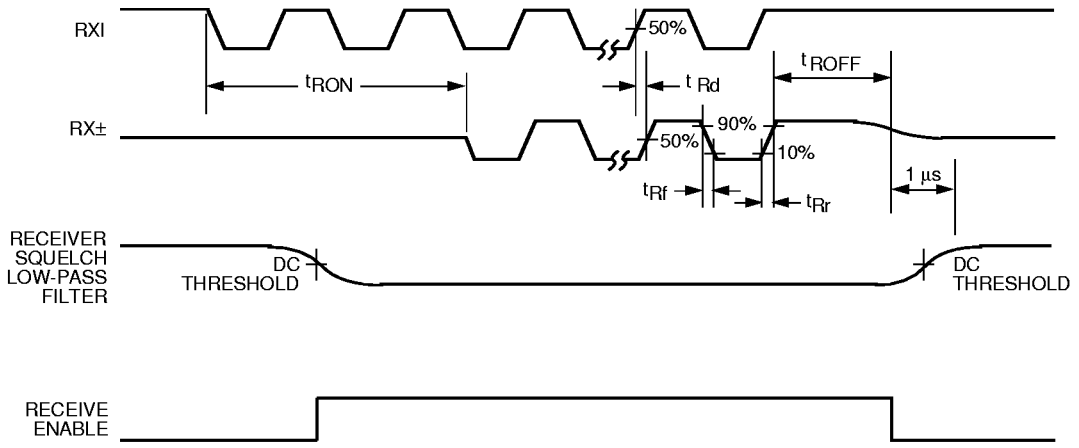
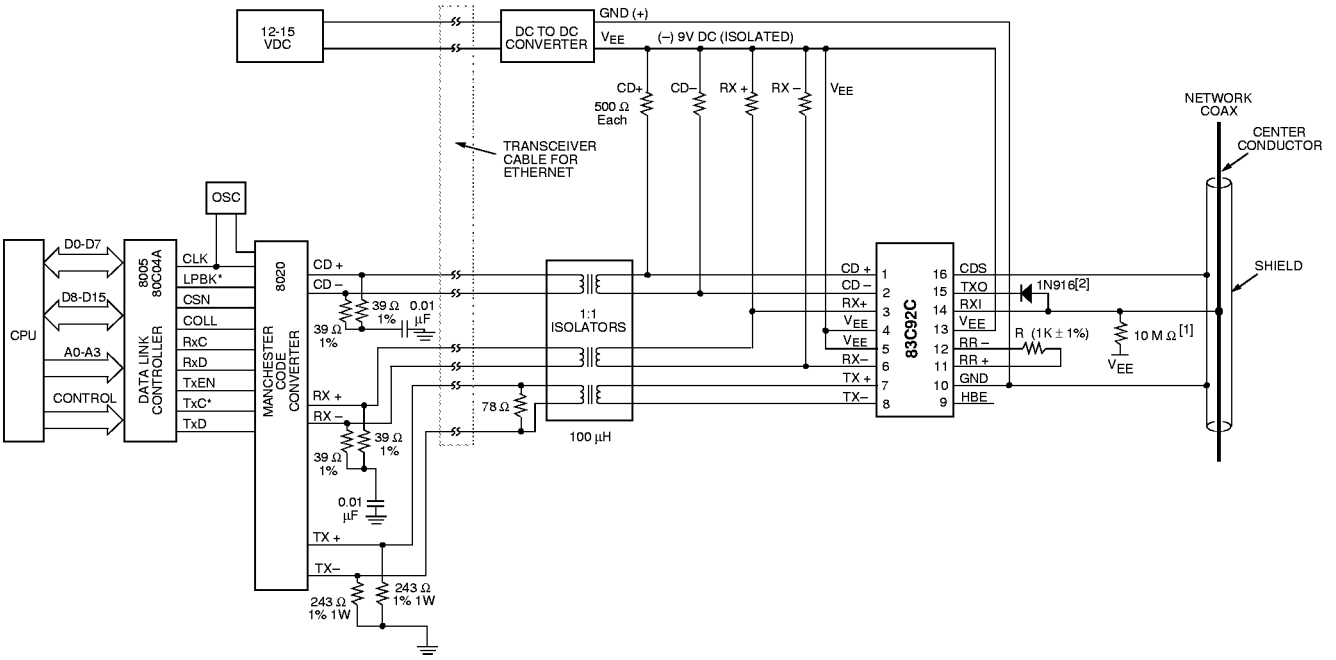


Figure 4. Receiver Timing



Notes: 1. 10 M Ω resistor is optional. 83C92C will assert "collision" signal when COAX cable is disconnected even if there is no transmit signal on TXO, with the 10 M Ω resistor option.

2. 1N916 diode or equivalent with low capacitance less than or equal to 1 pf value. This diode is needed for all 83C92C designs.

Figure 5. 83C92C Ethernet Transceiver System Connections

When a packet is detected, the DC level from the Low-pass Filter becomes more negative than the DC squelch threshold, which is typically –250 mV DC and the Receiver turns on. The squelch circuit AC timing detects high level signals of more than 225 nanoseconds, and turns the Receiver off. The Receiver stays off if within 1 microsecond (typical) the low pass filter level becomes more positive than the DC squelch threshold. See the Receiver Timing Diagram, Figure 4.

The System Connections diagram shows the transceiver connections in a station environment. RX± and CD± differential signals to the MCC are biased by 500-ohm pull-down resistors and are isolated from the MCC. For Thin Net applications where the 83C92C is located in the station equipment, the pull-down resistors can be increased to 1.5 kohms, and the termination resistors omitted to save power. The DC supply is converted to –9V by a DC to DC converter. This converter also provides DC isolation between the +12 volt and –9 volt sides.

The COAX center conductor connects to the Receive and Transmit pins of the transceiver. A 1N916 external diode minimizes network loading when power is on or off. COAX tap capacitance contributed by the 83C92C is less than 2 pF at 10 MHz, powered and unpowered, not transmitting. CDS, Collision Detection Sense detects the Collision reference level. This is ground-referenced sense pin. It should be connected directly to the COAX shield to prevent ground-loop interference.

The Transceiver assembly includes the DC - DC Converter and the RX±, TX± and CD± signal isolators. A Transceiver cable up to 50 meters (164 feet) long connects the MCC to the Transceiver assembly. These components are usually mounted on the computer adapter board in the Thin Net configuration, on a separate board for Ethernet configurations. See Figure 5.

Reliability

The 83C92C package will give one million hours Mean Time Between Failure (MTBF) under continuous operation as defined by the IEEE 802.3 standard.

Absolute Maximum Ratings (See Note 1)

Supply Voltage (V_{EE}) ..... –12V/ +0.3V Reverse Bias
Package Power Rating at 25°C ..... 1.5 Watts
(PC Board Mounted) Refer to the Pin Number Description
Derate linearly at the rate of 28.6 mW/*C
Input Voltage ..... +0.3V to V_{EE} –0.3V
Maximum I/O Current (RXI, CDS, HBE, RR+, RR–, TX+, TX–) ..... ±10mA
Maximum Current into TXO ..... +10mA/–100mA
Maximum Current into CD+, CD– ..... +40mA/–10mA
Absolute Maximum Voltage, RXI ..... +0.3V/–12V
Absolute Maximum Voltage, all pins except V_{EE}, RXI ..... +0.3V above ground/–0.3V below V_{EE}
Electrostatic Discharge all pins [Except RXI pin (±1600V min.)] (Human body model) ..... ±2500V min.
Latch-up DC Current ..... –100mA min.
Storage Temperature ..... –65°C to 150°C
Lead Temp. (Soldering, 10 seconds) ..... 260°C

For actual power dissipation of the device, refer to Electrical Characteristics Table.

NOTES

1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Electrical Characteristics

V_{EE} = –9V ±5%, T_A = Commercial 0°C to +70°, (See Notes 1, 2 & 3)

Symbol	Parameter	Min	Typ	Max	Units
I_{EE1}	Supply Current Out of V_{EE} Pin—Non Transmitting		–55	–70	mA
I_{EE2}	Supply Current Out of V_{EE} Pin—Transmitting		–100	–130	mA
I_{RXI}	Receive Input Bias Current (RXI)[3]	–2	–1	+25	µA
I_{TDC}	Transmit Output DC Current Level (TXO)	37	41	45	mA
I_{TAC}	Transmit Output AC Current Level (TXO)	±28		I_{TDC}	mA
V_{CD}	Collision Threshold (Receive Mode)[2]	–1.45	–1.53	–1.58	V
V_{OD}	Differential Output Voltage (RX±, CD±)[2]	±550		±1200	mV
V_{OC}	DC Common Mode Output Voltage (RX±, CD±)[1]	–1.5	–2.0	–2.5	V
V_{OB}	Idle State Differential Offset Voltage (RX±, CD±)			±40	mV
V_{OA}	AC Common Mode Output Voltage (RX±, CD±)[2]			±40	mV
V_{RSQ}	Receiver DC Squelch Threshold (RXI)	–150	–250	–350	mV
V_{TSQ}	Transmitter Squelch Threshold (TX±)	–175	–225	–300	mV
C_X	TAP Capacitance[4]		3.0	4.0	pF
R_{RXI}	Shunt Resistance—Non Transmitting (RXI)[5]	100			KΩ
R_{TXO}	Shunt Resistance—Transmitting(TXO)[2] [6]	10			KΩ
	Harmonic Content Relative to Fundamental				
$H_{C2,3}$	Second and Third Harmonics	–20			dB
$H_{C4,5}$	Fourth and Fifth Harmonics	–30			dB
$H_{C6,7}$	Sixth and Seventh Harmonics	–40			dB

NOTES

1. V_{OC} has no impact on system performance, since the twisted pair is transformer - isolated.
2. As required to meet ANSI/IEEE 802.3 and ISO 8802-3 specifications.
3. All currents into device pins are positive, all currents out of device pins are negative. All voltages referenced to ground unless otherwise specified.
4. Measured at RXI with a diode between TXO and RXI as shown in the recommended layout in Figure 5. The maximum diode capacitance is 1 pF. Guaranteed through characterization.
5. Current is measured on RXI while first forcing 0 volt and measuring the current, and then forcing –2 volts and measuring the current.

   Thus:
   $$R = \frac{\Delta V}{\Delta I} = \frac{2V}{[I @ 0V] - [I @ -2V]}$$

6. TX± is first set to 1 volt differential (DC voltage) to surpass the squelch level.
   Current is measured on TXO while first forcing 0 volt and measuring the current, and then forcing –2 volts and measuring the current. Calculation is the same as item 5 above.

Recommended Operating Conditions

Supply Voltage (V_{EE}) ..... –9V ± 5%
Temperature Range
(T_A) Commercial ..... 0° to +70°C

Switching Characteristics V_{EE} = –9V ±5%, T_A = Commercial 0°C to +70°, (See Note 1) For Test Load Conditions and Parameters, refer to Figure 10.

Symbol	Parameter	Fig	Min	Typ	Max	Units
t_{RON}	Receiver Startup Delay (RXI to RX±)[2]	4		4	5	bits
t_{ROFF}	Receiver High to Idle Time (RXI)[2,3]	4		300		ns
t_{Rd}	Receiver Propagation Delay (RXI to RX±)	4		15	50	ns
t_{Rr}	Differential Outputs Rise Time (RX±, CD±)	4		4	7	ns
t_{Rf}	Differential Outputs Fall Time (RX±,CD±)	4		4	7	ns
t_{RJ}	Receiver & Cable Total Jitter (including diode)			±2	±6	ns
t_{TST}	Transmitter Startup Delay (TX ± to TXO)[2]	3		1	2	bits
t_{Td}	Transmitter Propagation Delay (TX ± to TXO)	3	15	25	50	ns
t_{TID}	Transmit Idle Delay (Transmit Current < 2mA)[2]	3			400	ns
t_{Tr}	Transmitter Rise Time — 10% to 90% (TXO)	3	20	25	30	ns
t_{Tf}	Transmitter Fall Time — 90% to 10% (TXO)	3	20	25	30	ns
t_{TM}	t_{Tr} and t_{Tf} Mismatch			0.5	±2.0	ns
t_{TS}	Transmitter Skew (TXO)			±0.5	±1.0	ns
t_{TON}	Transmit Turn-On Pulse Width at V_{TSQ} (TX±)	3	15	20	40	ns
t_{TOFF}	Transmit Turn-Off Pulse Width at V_{TSQ} (TX±)[2,3]	3	130	175	200	ns
t_{CON}	Collision Turn-On Delay[2]	6		7	13	bits
t_{COFF}	Collision Turn-Off Delay	6			20	bits
f_{CD}	Collision Frequency (CD±)[4]	6	8.5		11.5	MHz
t_{CP}	Collision Pulse Width (CD±)[2]	6	35		70	ns
t_{HON}	CD Heartbeat Delay (TX± to CD±)	7	0.6		1.6	µs
t_{HW}	CD Heartbeat Duration (CD±)	7	0.5	1.0	1.5	µs
t_{JA}	Jabber Activation Delay (TX± to TXO and CD±)[2]	8	20	40	60	ms
t_{JR}	Jabber Reset Timeout (TX± to TXO and CD±)	8	250	500	750	ms

NOTES

1. All typicals are given for V_{EE} = –9V and T_A = 25°C.
2. As required to meet ANSI/IEEE 802.3 and ISO 8802–3 specifications.
3. Time to detect end of packet.
4. f_{CD} < 11.5 MHz at max. operating temp (70°C), f_{CD} < 12.5 MHz at min operating temp (0°C).

Timing and Load Diagrams

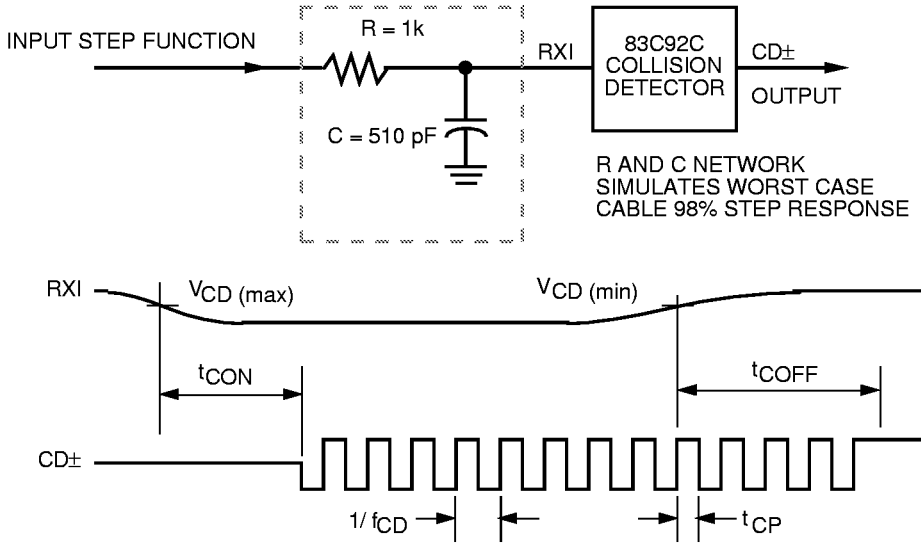


Figure 6. Collision Timing

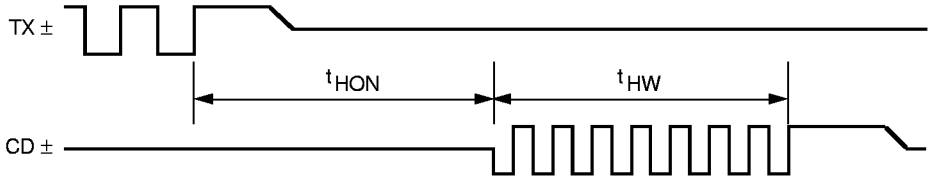


Figure 7. Heartbeat Timing

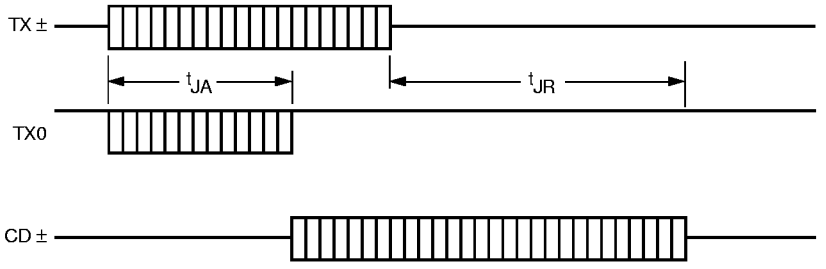


Figure 8. Jabber Timing

Timing and Load Diagrams (continued)

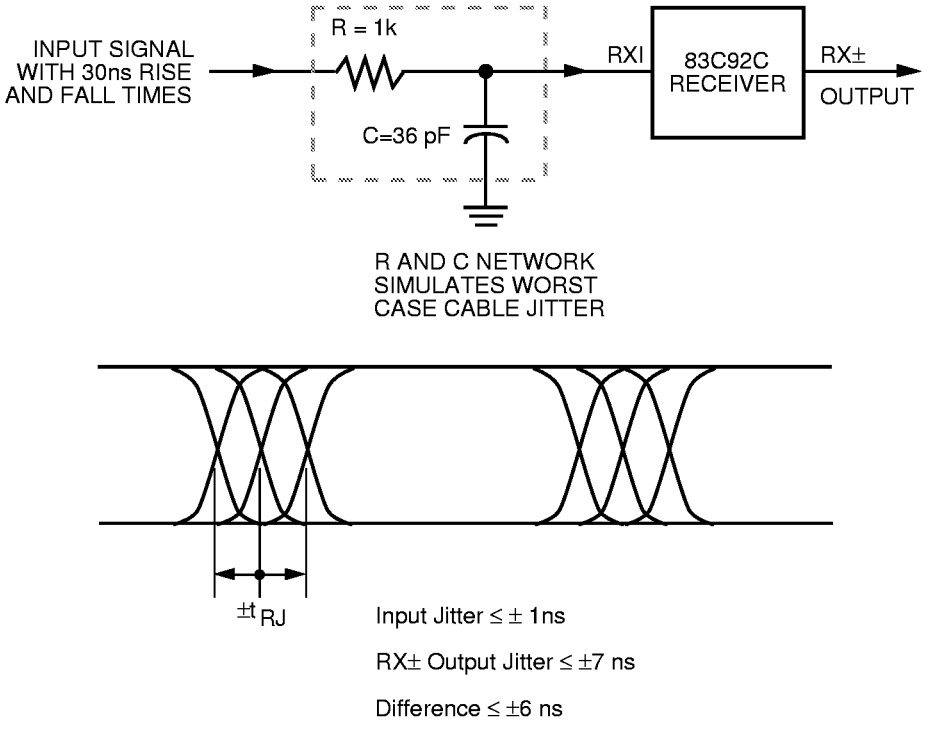
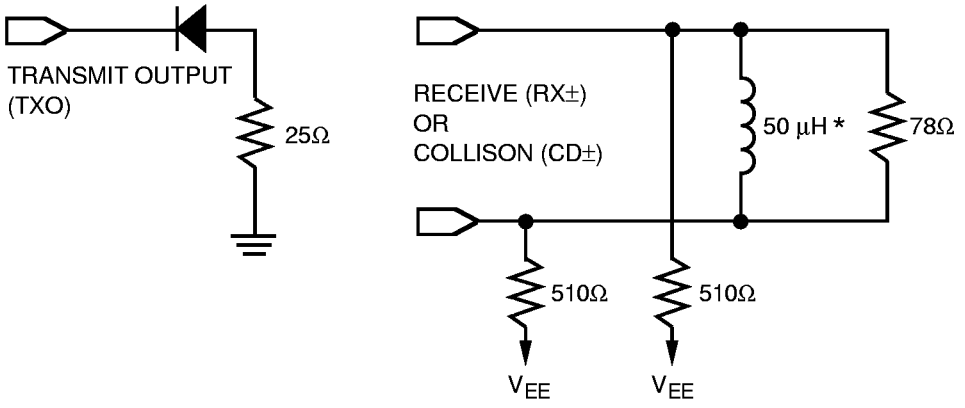


Figure 9. Receive Jitter Timing



* The 50µH Inductance is for testing purposes. Pulse transformers with higher inductances are recommended (see Figure 5).

Figure 10. Test Loads

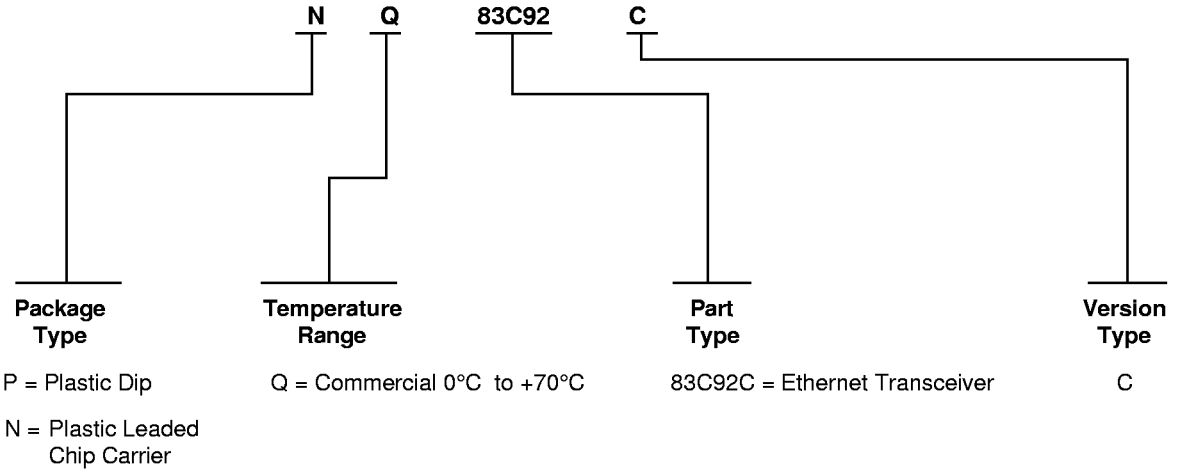


Figure 11. Ordering Information

Revision History

4/23/96

- Page 2; Figure 2. 20 Pin Plastic Leaded Chip Carrier:
  - This figure has been replaced with a new figure.

- Page 11; Figure 11. Ordering Information:
  - This figure has been replaced with a new figure.

9/5/96

- Page 13; The dimension diagram on this page has changed, for more details call SEEQ Technology, (510) 226-7400 ext. 3051.

2/17/98

Document Revision Change to MD400137/C

Global Change: All references to Extended Temperature Range –40°C to +85°C have been deleted.

Global Change: All references to 83C92C is fully compatible with ANSI/IEEE 802.3 and 8802-3, has been changed to 83C92C is compatible with ANSI/IEEE 802.3 and 8802-3.

Page 2: Figure 83C92C Ethernet Transceiver Pin Configuration;
- 20 Pin Plastic Leaded Chip Carrier has been deleted.

Page 7: Electrical Characteristics;
- I_{EE2} (MAX) has been changed from –120 to –130.
- V_{CD} (MIN) has been changed from –1.49 to –1.45.

Revision History

Page 8: Switching Characteristics
- f_{CD} Parameter, Collision Frequency (CD±) has been changed to Collision Frequency (CD±)[4]
- Addition of Note 4; f_{CD} < 11.5 MHz at max. operating temp (70°C), f_{CD} < 12.5 MHz at min operating temp (0°C).

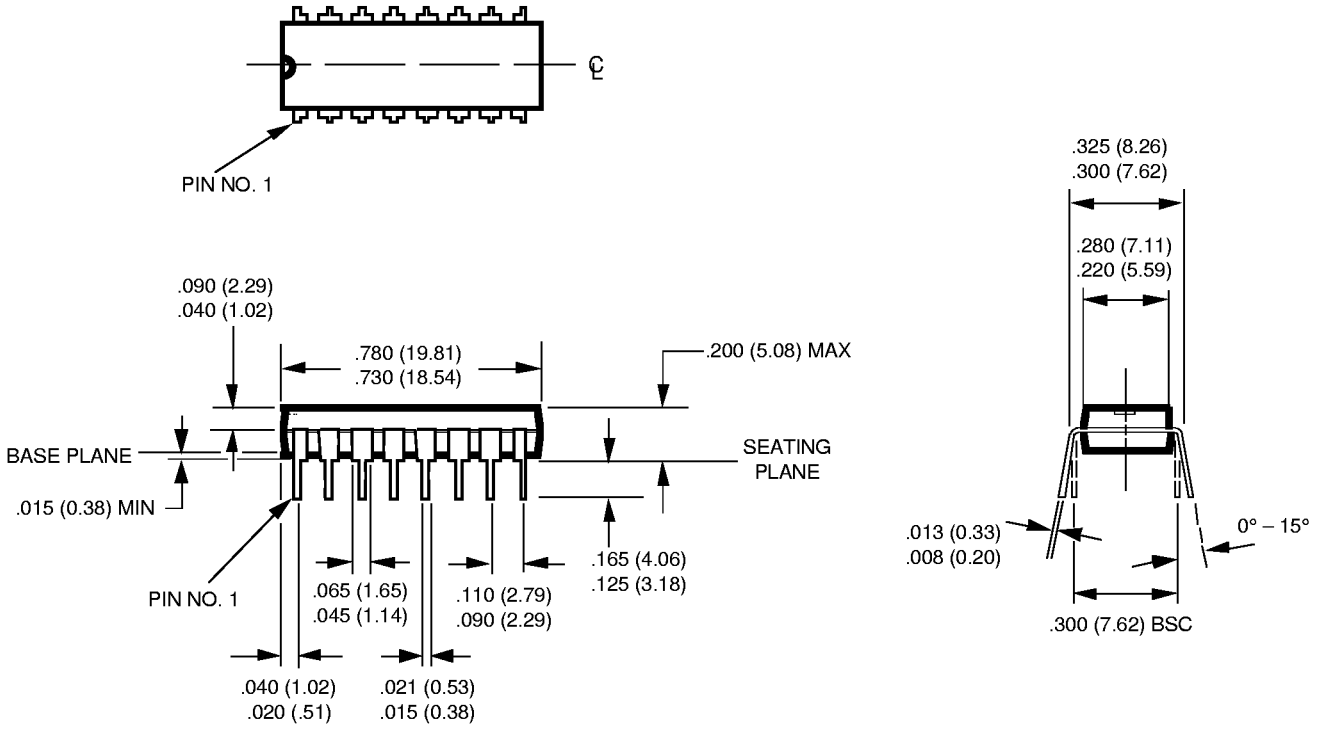
Page 11: Figure 11. Ordering Information;
- Reference to 20 Pin PLCC has been deleted.
- Reference to IEEE 802.3 has been deleted

Page 12: Pagination Change

Page 14: 20 Pin PLCC Dimension Diagram has been deleted.

PLASTIC DUAL-IN-LINE PACKAGES

16 LEAD (.300 CENTER) PLASTIC DIP PACKAGE TYPE P

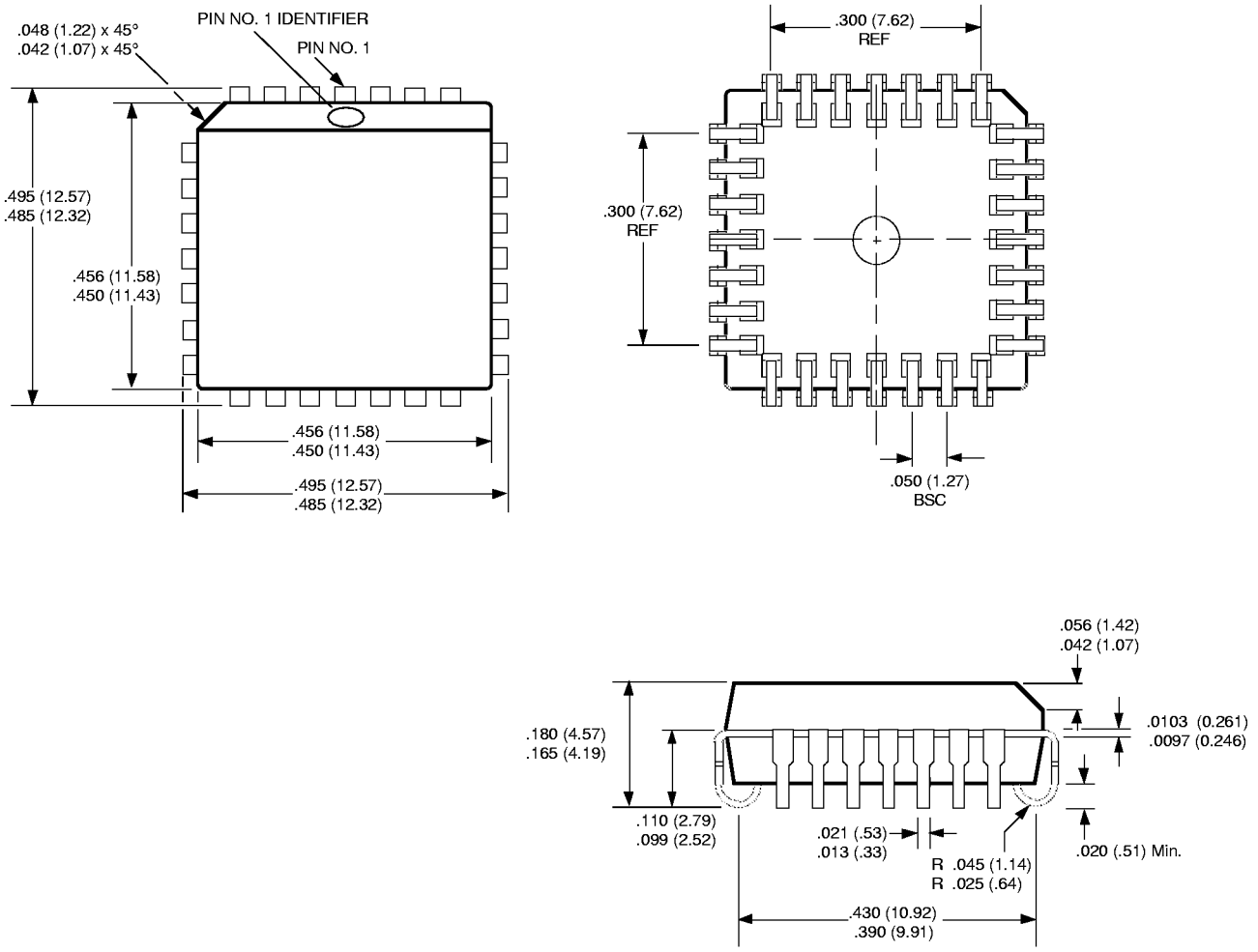


SEEQ OUTLINE P008/–

NOTES
1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Maximum allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are ± .010 (.25) unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

SURFACE MOUNT PACKAGES

28-PIN PLASTIC LEADED CHIP CARRIER TYPE N



NOTES

1. All dimensions are in inches and (millimeters).

2. Dimensions do not include mold flash. Maximum allowable flash is .008 (.20).

3. Formed leads shall be planar with respect to one another within 0.004 inches.