



Fremont Micro Devices

FT61E14

Data Sheet

Key Features

8-bit EEPROM-based RISC MCU

Program: 4k x 14; RAM: 512 x 8; Data: 128 x 8

8 / 10 / 14 / 16 / 20 Pins

12-bit high accuracy ADC (11-bit accuracy at $V_{ADC-REF} = 0.5V$)

4 Timers, 7 independent PWMs-3 with Deadband

USART

Low Standby, WDT and Operating Current

POR, LVR, LVD – Single Input Comparator

Selectable Source and Sink Current

High ESD, High EFT

Low V_{DD} Operating Voltage

Tunable HIRC

Rev1.00

www.fremontmicro.com

8-bit CPU (EEPROM)

- 49 RISC instructions: 2T or 4T
- 16 MHz / 2T ($V_{DD} \geq 2.7$)
- Up to 20 pins

Memory

- PROGRAM: 4k x 14 (R/W Protect)
- DATA: 128 x 8
- RAM: 512 x 8
- 16-level Hardware Stack
- Sector encryption, support IAP

Operation Conditions (5V, 25°C)

- V_{DD} ($V_{POR} \leq 1.9V$) $V_{POR} \sim 5.5 V$
(Self-regulated by POR, $\leq 1.7V$ for above 0°C)
- Operation temperature Grade $-40 \sim +85^\circ C$
- Low Standby 0.4 μA
- WDT 3.1 μA
- Normal Mode (16 MHz) 286 $\mu A/mips$

High Reliability

- 100k cycles of erasures (typical)
- > 20 years / 85°C storage (typical)
- ESD > 7 kV, EFT > 5.5 kV

ADC (12-bit)

- 12-bit accuracy (≤ 2 MHz ADC clock)
- 7 + 1 channels
- $V_{ADC-REF}$
 - ✓ Internal: 0.5, 2.0, 3.0, V_{DD}
 - ✓ External: +, - optional
- Automatic threshold comparison

PWM (Total 7)

- Support RUN in SLEEP
- 7 capture/compare/PWM channels:
 - ✓ Independent: Duty Cycle, Polarity
- 3 channels (up to 6 I/O):
 - ✓ Complementary + Deadband
- Auto Fault-Breaking (I/O, LVD, ADC)
- Edge-aligned, Center-aligned
- One-Pulse mode

Timers

- WDT (16-bit): 3-bit prescaler
- Timer1 (16-bit): 16-bit prescaler
- Timer2 (16-bit): 4-bit prescaler
- Timer4 (8-bit): 3-bit prescaler

- Auto-reloading
- Support RUN in SLEEP
- Sysclk, LIRC, 1 or 2x {HIRC, Crystal, EC}

Communication Interface

- USART

I/O PORTS (Up to 18 I/O)

- Resistive Pull-Up/Pull-Down
- Open-Drain
- 18 I/O I_{SOURCE} : 4, 8 or 26 mA (5V, 25°C)
- 18 I/O I_{SINK} : 53 or 62 mA (5V, 25°C)
- 18 I/O: Interrupt/Wake-Up

Power Management

- SLEEP
- LVR: 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1 (V)
- LVD: 2.0, 2.4, 2.8, 3.0, 3.6, 4.0 (V)
(LVD also functions as a single input comparator with selectable polarity.)

System Clock (SysClk)

- HIRC High Speed Internal Oscillator
 - ✓ 16MHz $< \pm 0.5\%$ typical (2.5–5.5V, 25°C)
 - ✓ Tunable
 - ✓ 1, 2, 4, 8, 16, 32, 64, 128 divider
- LIRC Low Power Internal Oscillator
 - ✓ 32 kHz or 256 kHz
- External Clock (I/O input)
- LP/XT crystal input
 - ✓ HIRC or LIRC during startup
 - ✓ Fail-Safe Clock Monitor(FSCM)

Other Features (Welcome to enquire)

- ADC minimum resolution is 0.12mV, accuracy is 0.24mV, suitable for current detection
- $\frac{1}{2} V_{DD}$ LCD bias

Integrated Development Environment (IDE)

- On-Chip Debug (OCD), ISP
- 3 hardware breakpoints
- Software-Reset, Stop, Single Step, Skip

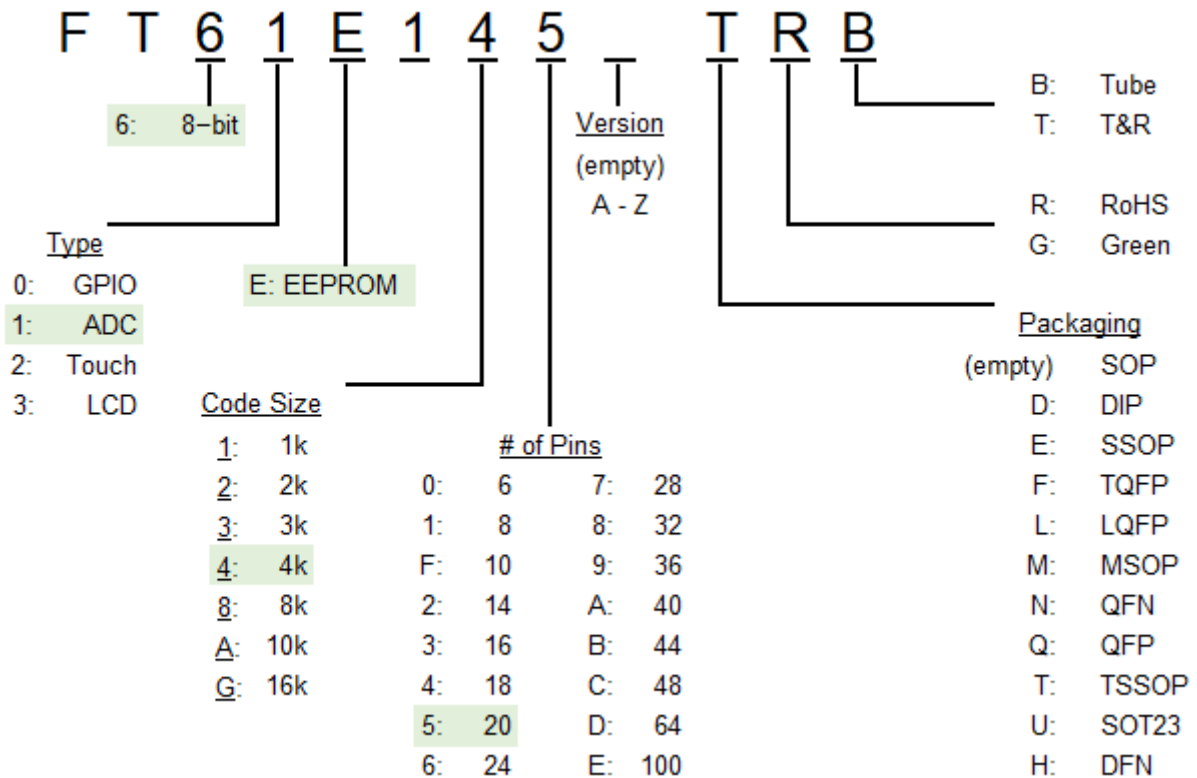
Packages

- | | | | |
|--------|---------|-------|-------|
| • SOP8 | MSOP10 | SOP14 | SOP16 |
| SOP20 | TSSOP20 | QFN20 | |

PARTS INFORMATION AND SELECTIONS

Part Number	Number of I/O	Package
FT61E141- <u>ab</u>	6	SOP8
FT61E14F- <u>Mab</u>	8	MSOP10
FT61E142- <u>ab</u>	12	SOP14
FT61E143- <u>ab</u>	14	SOP16
FT61E143A- <u>ab</u>		
FT61E143B- <u>ab</u>		
FT61E145- <u>ab</u>	18	SOP20
FT61E145A- <u>ab</u>		
FT61E145- <u>Tab</u>		TSSOP20
FT61E145A- <u>Tab</u>		
FT61E145- <u>Nab</u>		QFN20
FT61E145A- <u>Nab</u>		

Where a = R; RoHS
 = G; Green
b = B; Tube
 = T; T&R



MCU Part Number Selections

Revision History

Date	Revision	Description
2022-08-25	1.00	Preliminary version

Table of contents

- 1. BLOCK DIAGRAM AND PINOUTS 8
 - 1.1. Pinouts 9
 - 1.2. Pin Description by Functions 13
- 2. I/O PORTS..... 16
 - 2.1. Summary of I/O PORT Related Registers 19
 - 2.2. Configuring the I/O 23
 - 2.3. Pin Out Priority 24
- 3. POWER-ON-RESET (POR) 26
 - 3.1. BOOT Sequence..... 26
- 4. SYSTEM-RESET 28
 - 4.1. Summary of SYSTEM-RESET Related Registers 29
 - 4.2. Brown-Out Reset (LVR / BOR) 29
 - 4.3. Illegal Instruction Reset..... 30
 - 4.4. Software Reset 30
 - 4.5. Stack Overflow/Underflow Reset 30
 - 4.6. EMC Reset..... 30
 - 4.7. Watch Dog Timer (WDT) Reset..... 30
 - 4.8. External I/O System-Reset /MCLR 31
 - 4.9. Detect the Type of Last Reset 31
- 5. LOW VOLTAGE DETECT / COMPARATOR (LVD)..... 33
 - 5.1. Summary of LVD Related Registers 34
- 6. OSCILLATORS and SYSCLK 35
 - 6.1. Summary of Oscillator Modules Related Registers 37
 - 6.2. Internal Clock Modes (HIRC and LIRC)..... 40
 - 6.3. External Clock Modes 42
 - 6.3.1. EC mode 42
 - 6.3.2. LP and XT modes 42
 - 6.4. HIRC, LIRC and EC inter-switching 43
- 7. TIMERS 45

7.1.	Watch Dog Timer (WDT)	45
7.1.1.	Summary of WDT Related Registers	46
7.1.2.	Configuration and using the WDT.....	47
7.2.	Advanced TIMER1	48
7.2.1.	Summary of Timer1 Related Registers	49
7.2.2.	Counting basic units	66
7.2.3.	Clock/Trigger Controller.....	71
7.2.4.	Capture/Compare Channels	78
7.3.	General-purpose TIMER2.....	92
7.3.1.	Summary of Timer2 Related Registers	93
7.3.2.	Counting basic units	101
7.3.3.	Capture / Compare Channel.....	104
7.4.	Basic TIMER4	107
7.4.1.	Summary of Timer4 Related Registers	108
8.	SLEEP (POWER-DOWN).....	110
8.1.	Enter SLEEP	110
8.2.	Wake Up from SLEEP	111
9.	INTERRUPTS.....	113
9.1.	Summary of Interrupt Related Registers	115
9.2.	External pin interrupt.....	121
10.	DATA EEPROM AND PROGRAM PROM	122
10.1.	Summary of DATA EEPROM and PROM Related Registers.....	123
10.2.	DATA EEPROM.....	124
10.2.1.	Writing DATA EEPROM	124
10.2.2.	Read DATA EEPROM.....	126
10.3.	Program PROM	126
10.3.1.	Erase Program PROM.....	127
10.3.2.	Writing Program PROM.....	128
10.3.3.	Reading Program PROM.....	130
10.4.	Read BOOT Register UCFGx.....	130

11. 12-bit ADC	131
11.1. Summary of ADC Related Registers	132
11.2. ADC Configuration	136
11.2.1. ADC Trigger and Configuration of Delay	137
11.2.2. ADC Aborts Conversion.....	139
11.2.3. Threshold Comparison	139
11.2.4. Interrupt.....	139
11.3. Sample-and-hold time	140
11.4. Minimum sampling time	140
11.5. Example of ADC Conversion Steps	141
12. USART INTERFACE	144
12.1. Summary of USART Interface Related Registers.....	146
12.2. USART function	152
12.2.1. Asynchronous Operating Mode	152
12.2.2. Synchronous Operating Mode	153
12.2.3. Infrared Operating Mode.....	154
12.2.4. Smart Card Mode	154
12.2.5. LIN Master Mode	155
12.2.6. Multiprocessor Communication Mode	156
12.2.7. Automatic baud rate detection	156
13. MEMORY READ / WRITE PROTECTON	158
14. SPECIAL FUNCTION REGISTERS (SFR)	159
14.1. Boot Level Registers	159
14.2. User Registers	161
14.3. STATUS Register	173
14.4. Stack	174
14.5. Indirect addressing.....	174
14.5.1. Conventional data memory	175
14.5.2. Linear data memory	176
14.5.3. Flash program memory.....	176

15. INSTRUCTION SET	178
15.1. Read-Modify-Write (RMW) Instructions	180
15.2. Instruction details	181
16. ELECTRICAL SPECIFICATIONS	191
16.1. Limit Parameters	191
16.2. Operation Characteristics	191
16.3. POR, LVR, LVD	192
16.4. I/O PORTS	193
16.5. Operating Current (I_{DD})	193
16.6. Internal Oscillators	194
16.7. ADC (12bit) and ADC VREF	194
16.8. Program and Data EEPROM	196
16.9. EMC characteristics	196
17. Characterization Graphs	197
18. PACKAGING INFORMATION	202
19. Appendix : Register Types	209
Contact Information	210

1. BLOCK DIAGRAM AND PINOUTS

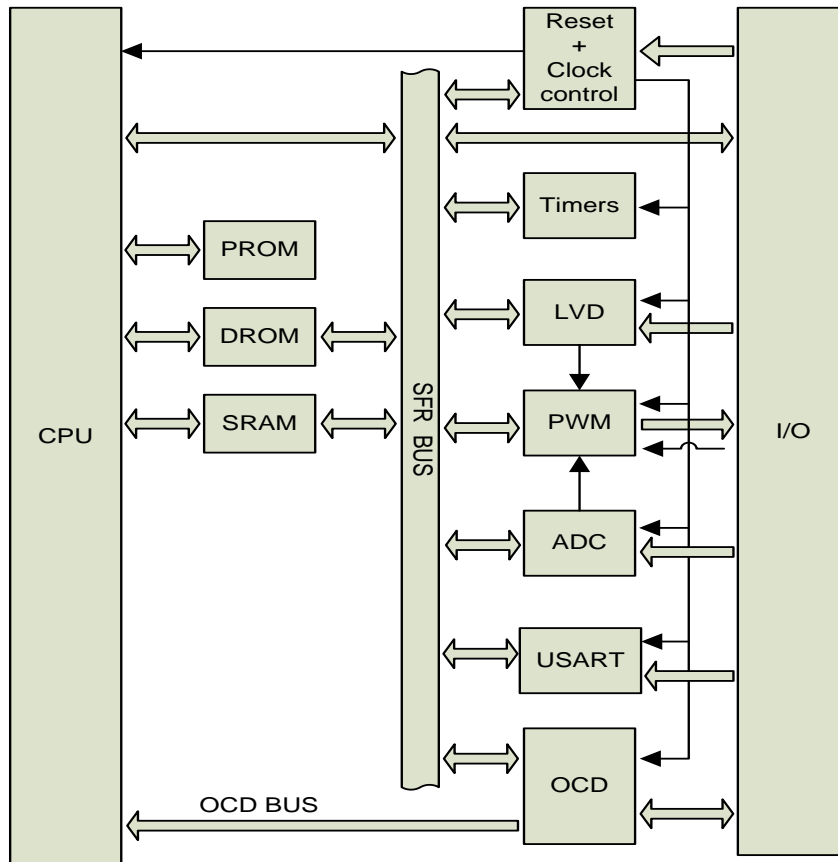


Figure 1-1 System Block Diagram

The list of standard abbreviations is as follows:

Abbreviation	Description
CPU	Central Processing Unit
SFR	Special Function Registers
SRAM	Static Random Access Memory
DROM	Data EEPROM
PROM	Program EEPROM
Timers	WDT, Timer1, Timer2, Timer4
PWM	Pulse Width Modulator
ADC	Analog to Digital Converter
LVD	Low Voltage Detect / comparator
USART	Universal Synchronous Asynchronous Receiver Transmitter
OCD	On Chip Debug
I/O	Input / Output

1.1. Pinouts

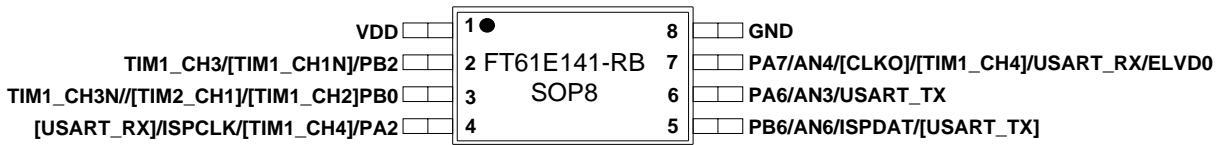


Figure 1-2 SOP8

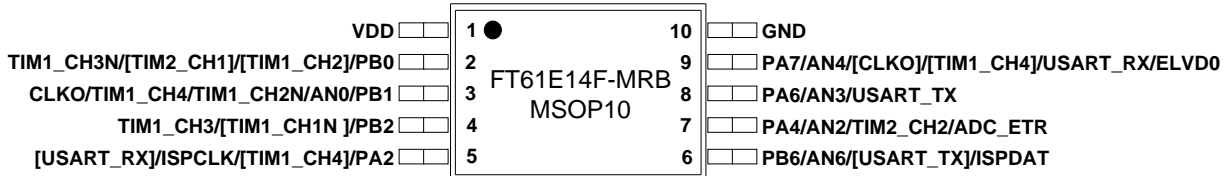


Figure 1-3 MSOP10

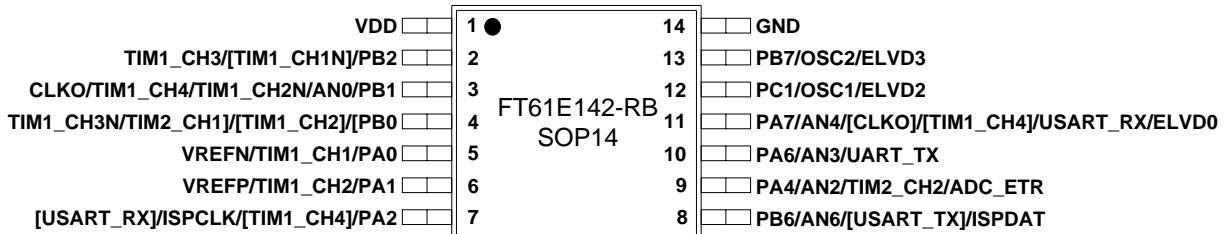


Figure 1-4 SOP14

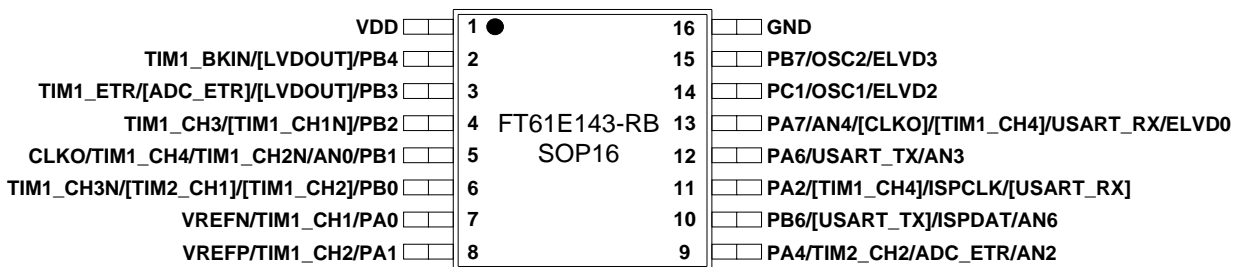


Figure 1-5 SOP16 (A)

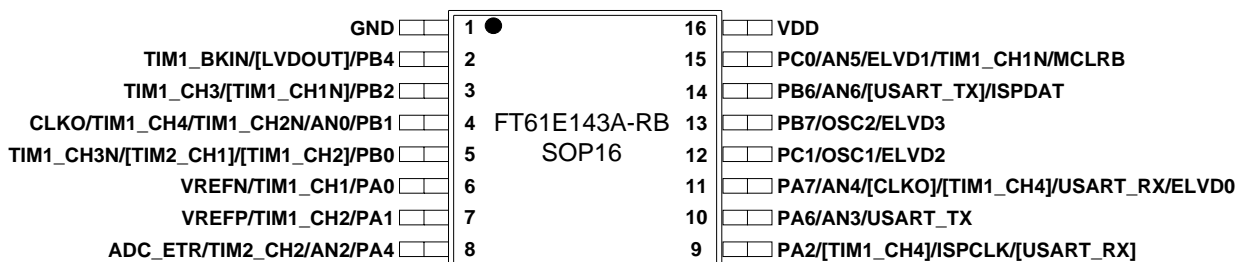


Figure 1-6 SOP16 (B)

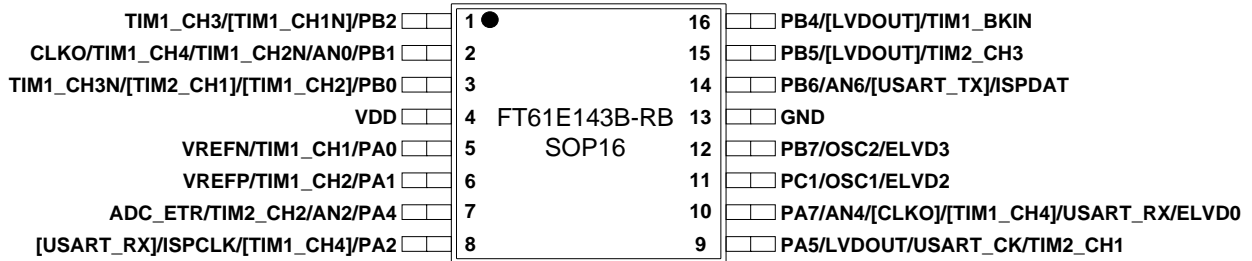


Figure 1-7 SOP16 (C)

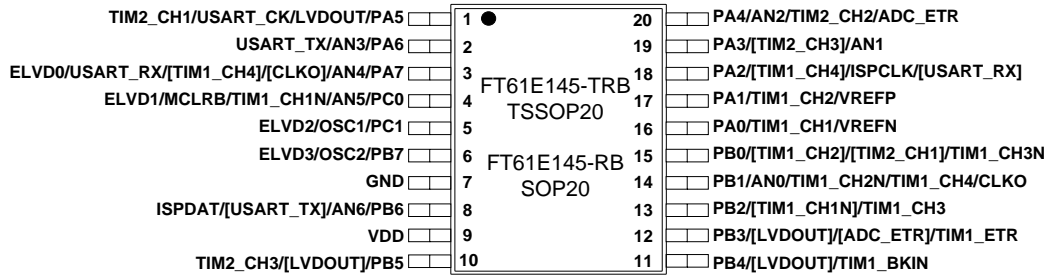


Figure 1-8 TSSOP20 / SOP20 (A)

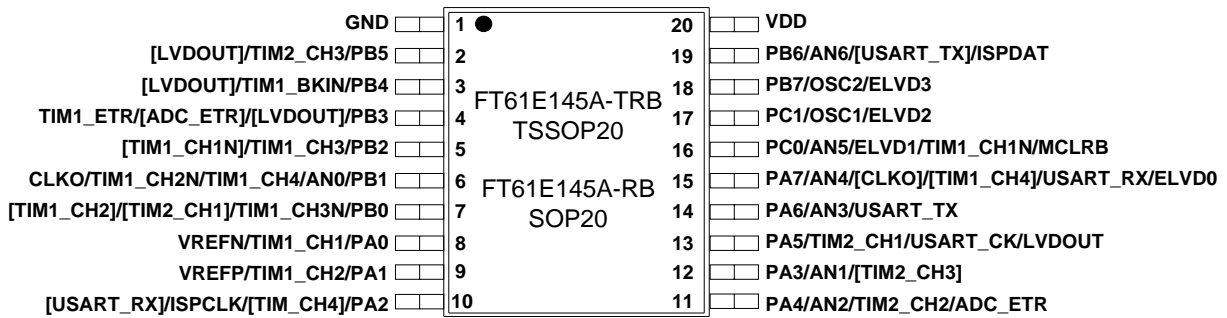


Figure 1-9 TSSOP20 / SOP20 (B)

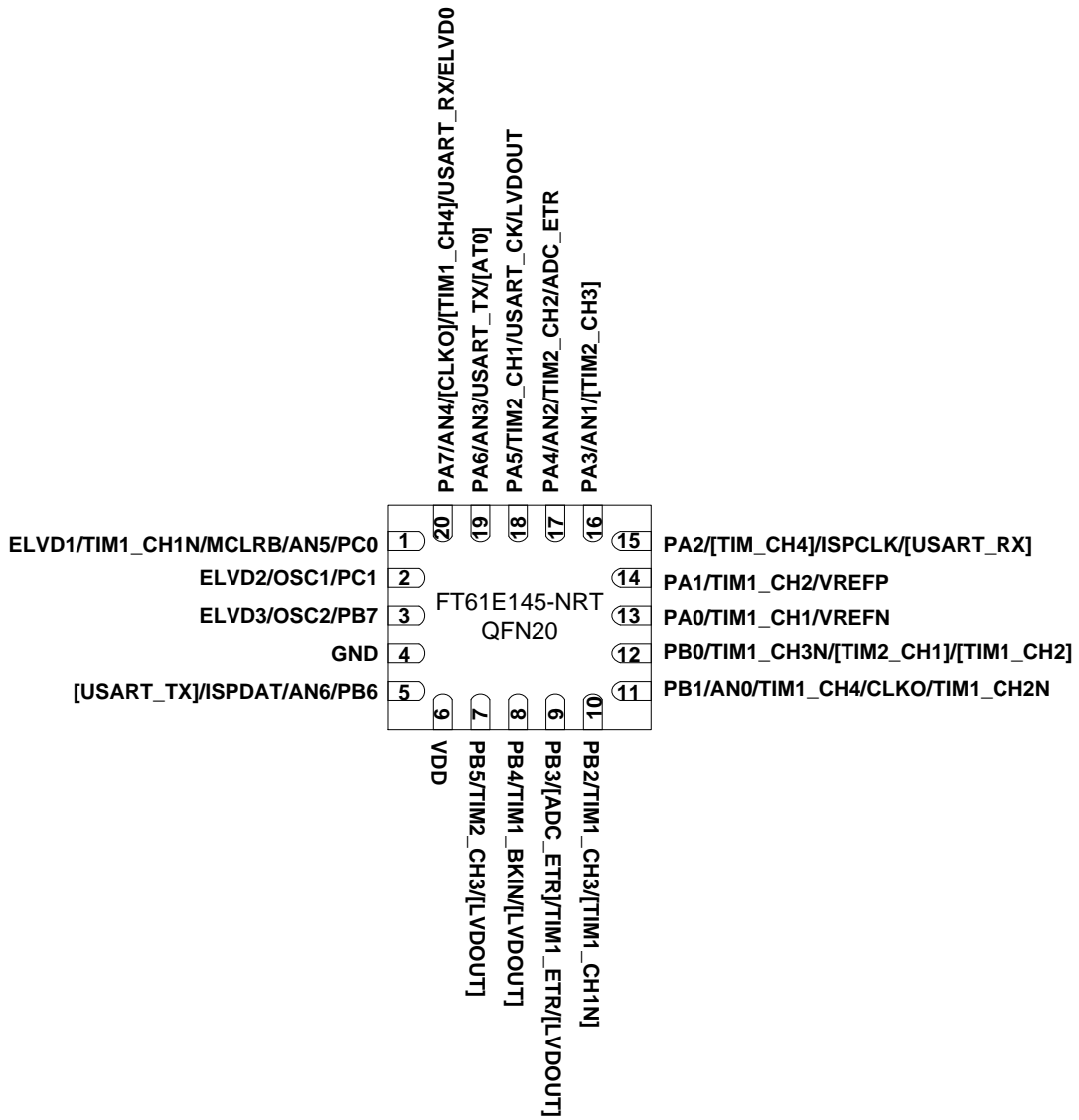


Figure 1-10 QFN20 (A) ¹

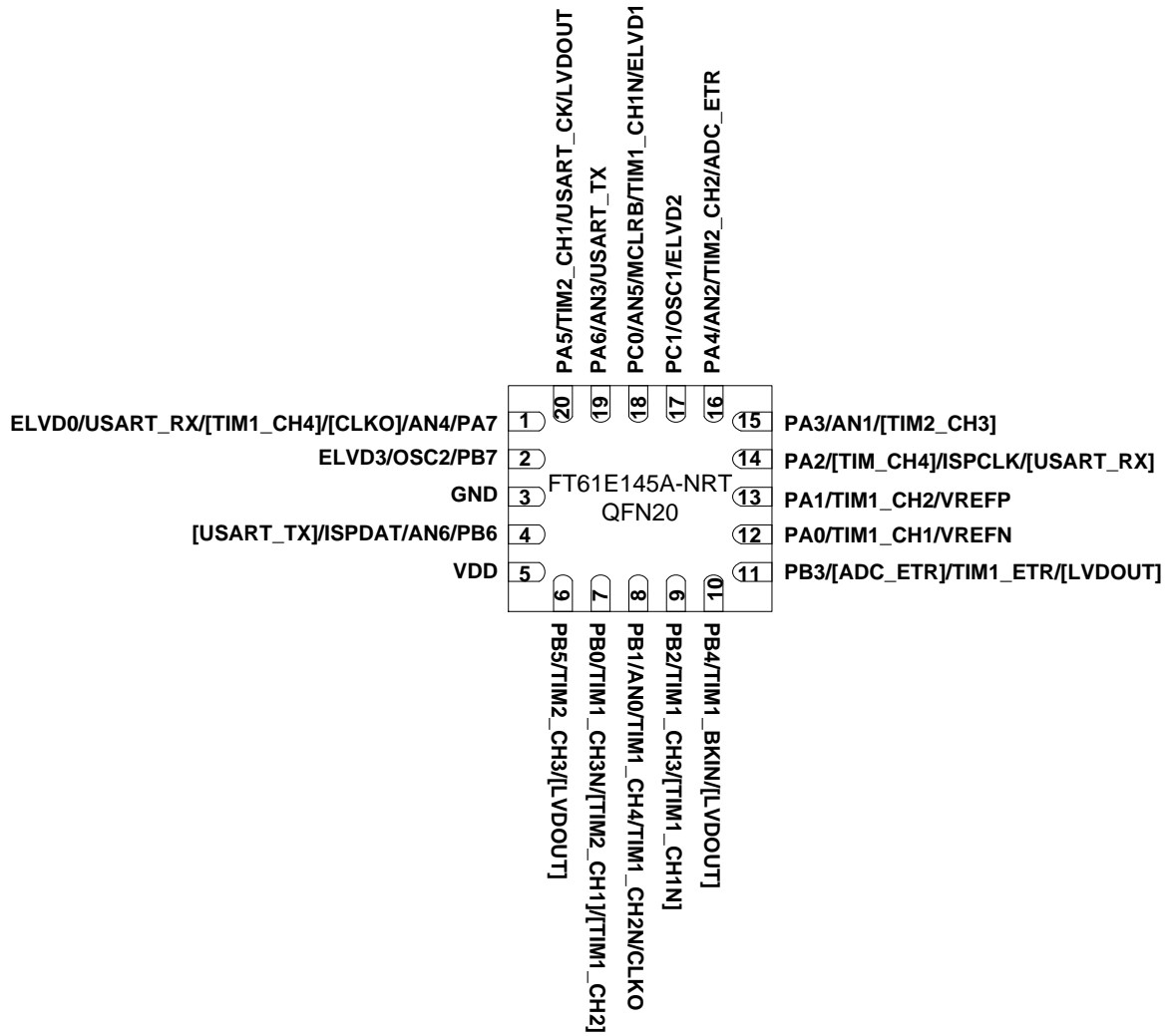


Figure 1-11 QFN20 (B) ¹

¹ For the QFN20 package, the exposed pad on the bottom is wired to GND.

1.2. Pin Description by Functions

Function	Description	Name	GPIO equiv.	8 pins	10 pins	14 pins	16(A) pins	16(B) pins	16(C) pins	20(A) pins	20(B) pins	QFN20 (A) pins	QFN20 (B) pins	
Power		VDD		1	1	1	1	16	4	9	20	6	5	
		GND		8	10	14	16	1	13	7	1	4	3	
GPIO	Pull-Up / Pull-Down, Digital Input, Digital Output	PC1				12	14	12	11	5	17	2	17	
		PC0						15		4	16	1	18	
		PB7				13	15	13	12	6	18	3	2	
		PB6		5	6	8	10	14	14	8	19	5	4	
		PB5							15	10	2	7	6	
		PB4						2	2	16	11	3	8	10
		PB3						3			12	4	9	11
		PB2		2	4	2	4	3	1	13	5	10	10	9
		PB1			3	3	5	4	2	14	6	11	11	8
		PB0		3	2	4	6	5	3	15	7	12	12	7
		PA7		7	9	11	13	11	10	3	15	20	20	1
		PA6		6	8	10	12	10		2	14	19	19	19
		PA5								9	1	13	18	20
		PA4			7	9	9	8	7	20	11	17	17	16
		PA3									19	12	16	15
		PA2		4	5	7	11	9	8	18	10	15	15	14
PA1					6	8	7	6	17	9	14	14	13	
PA0					5	7	6	5	16	8	13	13	12	
ISP Debugger	ISP-Data	ISPDAT	PB6	5	6	8	10	14	14	8	19	5	4	
	ISP-CLK	ISPCLK	PA2	4	5	7	11	9	8	18	10	15	14	
External reset	Pull-Up	/MCLR	PC0					15		4	16	1	18	
LVD	Input	ELVD0	PA7	7	9	11	13	11	10	3	15	20	1	
		ELVD1	PC0					15		4	16	1	18	
		ELVD2	PC1			12	14	12	11	5	17	2	17	
		ELVD3	PB7			13	15	13	12	6	18	3	2	
	Output	LVDO	PA5						9	1	13	18	20	
		[LVDO]	PB5						15	10	2	7	6	
[LVDO]		PB4				2	2	16	11	3	8	10		

Function	Description	Name	GPIO equiv.	8 pins	10 pins	14 pins	16(A) pins	16(B) pins	16(C) pins	20(A) pins	20(B) pins	QFN20 (A) pins	QFN20 (B) pins
		[LVDOOUT]	PB3				3			12	4	9	11
Clock	Output	CLKO	PB1		3	3	5	4	2	14	6	11	8
		[CLKO]	PA7	7	9	11	13	11	10	3	15	20	1
	OSC+	OSC1	PC1			12	14	12	11	5	17	2	17
	OSC -	OSC2	PB7			13	15	13	12	6	18	3	2
Timer1 (Deadband)	PWM1	TIM1_CH1	PA0			5	7	6	5	16	8	13	12
	/PWM1	TIM1_CH1N	PC0					15		4	16	1	18
		[TIM1_CH1N]	PB2	2	4	2	4	3	1	13	5	10	9
	PWM2	TIM1_CH2	PA1			6	8	7	6	17	9	14	13
		[TIM1_CH2]	PB0	3	2	4	6	5	3	15	7	12	7
	/PWM2	TIM1_CH2N	PB1		3	3	5	4	2	14	6	11	8
	PWM3	TIM1_CH3	PB2	2	4	2	4	3	1	13	5	10	9
	/PWM3	TIM1_CH3N	PB0	3	2	4	6	5	3	15	7	12	7
	PWM4	TIM1_CH4	PB1		3	3	5	4	2	14	6	11	8
		[TIM1_CH4]	PA7	7	9	11	13	11	10	3	15	20	1
PWM Fault-Break Input	TIM1_BKIN	PB4				2	2	16	11	3	8	10	
Trigger	TIM1_ETR	PB3				3			12	4	9	11	
Timer2	PWM5	TIM2_CH1	PA5						9	1	13	18	20
		[TIM2_CH1]	PB0	3	2	4	6	5	3	15	7	12	7
	PWM6	TIM2_CH2	PA4		7	9	9	8	7	20	11	17	16
	PWM7	TIM2_CH3	PB5						15	10	2	7	6
		[TIM2_CH3]	PA3							19	12	16	15
ADC	Input	AN6	PB6	5	6	8	10	14	14	8	19	5	4
		AN5	PC0					15		4	16	1	18
		AN4	PA7	7	9	11	13	11	10	3	15	20	1
		AN3	PA6	6	8	10	12	10		2	14	19	19
		AN2	PA4		7	9	9	8	7	20	11	17	16
		AN1	PA3							19	12	16	15
		AN0	PB1		3	3	5	4	2	14	6	11	8
	Trigger	ADC_ETR	PA4		7	9	9	8	7	20	11	17	16
		[ADC_ETR]	PB3				3			12	4	9	11

Function	Description	Name	GPIO equiv.	8 pins	10 pins	14 pins	16(A) pins	16(B) pins	16(C) pins	20(A) pins	20(B) pins	QFN20 (A) pins	QFN20 (B) pins
	V _{REF-}	VREFN	PA0			5	7	6	5	16	8	13	12
	V _{REF+}	VREFP	PA1			6	8	7	6	17	9	14	13
External pin interrupt	Low level, Rising edge, Falling edge, Double-edge	PC1				12	14	12	11	5	17	2	17
		PC0						15		4	16	1	18
		PB7				13	15	13	12	6	18	3	2
		PB6		5	6	8	10	14	14	8	19	5	4
		PB5							15	10	2	7	6
		PB4					2	2	16	11	3	8	10
		PB3					3			12	4	9	11
		PB2		2	4	2	4	3	1	13	5	10	9
		PB1			3	3	5	4	2	14	6	11	8
		PB0		3	2	4	6	5	3	15	7	12	7
		PA7		7	9	11	13	11	10	3	15	20	1
		PA6		6	8	10	12	10		2	14	19	19
		PA5							9	1	13	18	20
		PA4			7	9	9	8	7	20	11	17	16
		PA3								19	12	16	15
		PA2		4	5	7	11	9	8	18	10	15	14
PA1					6	8	7	6	17	9	14	13	
PA0					5	7	6	5	16	8	13	12	
USART	USART_CK	USART_CK	PA5						9	1	13	18	20
	USART_TX (Open-Drain)	USART_TX	PA6	6	8	10	12	10		2	14	19	19
		[USART_TX]	PB6	5	6	8	10	14	14	8	19	5	4
	USART_RX	USART_RX	PA7	7	9	11	13	11	10	3	15	20	1
		[USART_RX]	PA2	4	5	7	11	9	8	18	10	15	14

Table 1-1 Pin description by functions

2. I/O PORTS

Up to 18 I/O pins are available depending on the types of package. I/O ports are divided into 3 groups: PORTA (8), PORTB (8) and PORTC (2). [Table 2-1](#) lists the functions of all I/O pins.

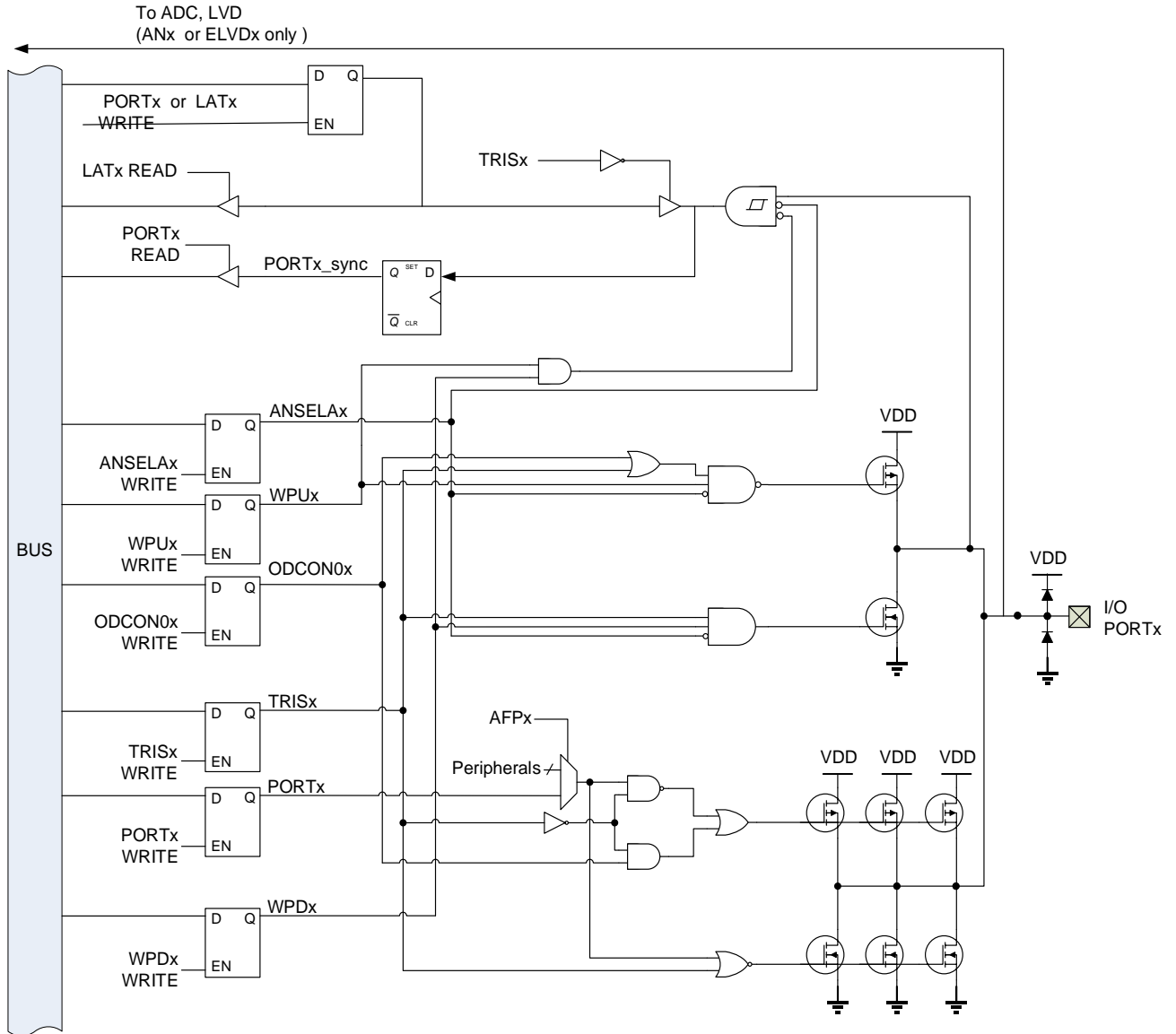


Figure 2-1 PORT Block Diagram

All I/O pins have the following functions ([Table 2-2](#) , [Table 2-3](#)):

- Digital Output
- Digital Input
- Open-Drain (USART corresponding PORTs)
- Weak Pull-Up
- Weak Pull-Down

In addition some I/O's have special functions assigned.

1. Burn debugger pins (ISP-Data, ISP-CLK) are hardware internal connection and require no set-up.

2. The Some special functions are configured at the IDE and loaded during BOOT ([Table 2-7](#)):

- External Clock/Crystal Oscillator IN (OSC1, OSC2)
- System-Reset (/MCLR)

3. All other functions are Instruction Level assigned to the various I/O's. They are divided into 4 categories:

a) Digital Output

- PWM
- Internal Clock Output
- LVD Output

b) Digital Input

- PWM Fault Break
- Timer1 trigger (TIM1_ETR)
- GPIO Interrupt-on-Change
- ADC trigger (ADC_ETR)

c) Analog Input

- LVD/BOR
- ADC
- V_{REF+}
- V_{REF-}

d) Communication Interface

- USART

Name	ISP Debugger	CLK	ADC	USART	Interrupt	LVD	PWM	Digital I/O Pull-Up / Pull-Down	Open-Drain	Source Current (mA)	Sink Current (mA)
PA0			(V _{REF-})		√		PWM1	√		4, 26	53, 62
PA1			(V _{REF+})		√		PWM2	√		4, 26	53, 62
PA2	CLK			[RX]	√			√		4, 26	53, 62
PA3			AN1		√		[PWM7]	√		4, 26	53, 62
PA4			AN2/ Trigger		√		PWM6	√		4, 26	53, 62
PA5				CLK	√	LVDOUT	PWM5	√		4, 26	53, 62
PA6			AN3	TX	√			√	√	4, 26	53, 62
PA7		Output	AN4	RX	√	ELVD0	[PWM4]	√		4, 26	53, 62
PB0					√		[PWM2]/ PWM3N/ [PWM5]	√		8,26	53, 62
PB1		Output	AN0		√		PWM4/ PWM2N	√		8,26	53, 62
PB2					√		PWM3/ [PWM1N]	√		8,26	53, 62
PB3			Trigger		√	[LVDOUT]	TIM1_ETR	√		8,26	53, 62
PB4					√	[LVDOUT]	BKIN	√		8,26	53, 62
PB5					√	[LVDOUT]	PWM7	√		8,26	53, 62
PB6	DATA		AN6	[TX]	√			√	√	8,26	53, 62
PB7		OSC-			√	ELVD3		√		8,26	53, 62
PC0			AN5		√	ELVD1	PWM1N	√		4, 8, 26	53, 62
PC1		OSC+			√	ELVD2		√		4, 8, 26	53, 62
Notes					/MCLR =PC0					V _{DD} =5, V _{DS} =0.5	

Table 2-1 I/O PORT functions

Note: PORTA and PORTB each has 2 configurable source current levels (see "PSRCAx" and "PSRCBx", [Table 2-3](#)), PORTC has 3 configurable source current levels (see "PSRCCx", [Table 2-3](#)), All IO each has 2 configurable sink current levels (see "PSINKx", [Table 2-3](#)).

2.1. Summary of I/O PORT Related Registers

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
ANSELA	0x197	-	ANSELA[6:0]								-000 0000
TRISA	0x8C	TRISA[7:0], PORTA Data Direction Register								1111 1111	
TRISB	0x8D	TRISB[7:0], PORTB Data Direction Register								1111 1111	
TRISC	0x8E	-	-	-	-	-	-	PORTC Data Direction Register		---- --11	
PORTA	0x0C	PORTA Output Register								xxxx xxxx	
PORTB	0x0D	PORTB Output Register								xxxx xxxx	
PORTC	0x0E	-	-	-	-	-	-	PORTC Output Register		---- --xx	
LATA	0x10C	PORTA Data Latch								xxxx xxxx	
LATB	0x10D	PORTB Data Latch								xxxx xxxx	
LATC	0x10E	-	-	-	-	-	-	PORTC Data Latch		---- --xx	
WPUA	0x18C	PORTA Weak Pull-Up								0000 0000	
WPUB	0x18D	PORTB Weak Pull-Up								0000 0000	
WPUC	0x18E	-	-	-	-	-	-	PORTC Weak Pull-Up		---- --00	
WPDA	0x20C	PORTA Weak Pull-Down								0000 0000	
WPDB	0x20D	PORTB Weak Pull-Down								0000 0000	
WPDC	0x20E	-	-	-	-	-	-	PORTC Weak Pull-Down		---- --00	
ODCON0	0x21F	-	-	-	-	-	-	-	UROD	---- --0	
PSRC0	0x11A	PORTA Source Current Setting								1111 1111	
PSRC1	0x11B	PORTB Source Current Setting								1111 1111	
PSRC2	0x11C	-	-	-	-	PORTC Source Current Setting			---- 1111		
PSINK0	0x19A	PORTA Sink Current Setting								0000 0000	
PSINK1	0x19B	PORTB Sink Current Setting								0000 0000	
PSINK2	0x19C	-	-	-	-	-	-	PORTC Sink Current Setting		---- --00	
ITYPE0	0x11E	PORTx[1:0] (x = A, B, C) and PORTy[3:2] (y = A, B) Ext. Pin Interrupt Type Setting								0000 0000	
ITYPE1	0x11F	PORTy[7:4] (y = A, B) Ext. Pin Interrupt Type Setting								0000 0000	
AFP0	0x19E	-	-	Pin Remapping Register 0				-		--00 000-	
AFP1	0x19F	-	-	Pin Remapping Register 1						--00 0000	
EPS0	0x118	External interrupt EINT3~0 pin selection								0000 0000	
EPS1	0x119	External interrupt EINT7~4 pin selection								0000 0000	
EPIE0	0x94	External pin interrupt enable								0000 0000	
EPIF0	0x14	External pin interrupt flag								0000 0000	

Table 2-2 Addresses and Reset Values of I/O related registers

Name	Status		Register	Addr.	Reset
TRISA	PORTA	<u>PORT Digital Output (Direction)</u> 1 = <u>Disable</u> 0 = Enable (Disable Pull-Up/Down)	TRISA[7:0]	0x8C	RW-1111 1111
TRISB	PORTB		TRISB[7:0]	0x8D	RW-1111 1111
TRISC	PORTC		TRISC[1:0]	0x8E	RW-11
ANSELA	1 = Disable Pull-Up /Down, and Digital Input (only for 7 ADC channels) 0 = (No action)		ANSELA[6:0]	0x197	RW-000 0000
WPUA	PORTA	<u>Weak Pull-Up</u> 1 = Enable 0 = <u>Disable</u>	WPUA[7:0]	0x18C	RW-0000 0000
WPUB	PORTB		WPUB[7:0]	0x18D	RW-0000 0000
WPUC	PORTC		WPUC[1:0]	0x18E	RW-00
WPDA	PORTA	<u>Weak Pull-Down</u> 1 = Enable 0 = <u>Disable</u>	WPDA[7:0]	0x20C	RW-0000 0000
WPDB	PORTB		WPDB[7:0]	0x20D	RW-0000 0000
WPDC	PORTC		WPDC[1:0]	0x20E	RW-00
PORTA	PORTA	<u>Data Output Register</u> Read: Returns V _{IO} Write: Write to the corresponding LATx register	PORTA[7:0]	0x0C	RW-xxxx xxxx
PORTB	PORTB		PORTB[7:0]	0x0D	RW-xxxx xxxx
PORTC	PORTC		PORTC[1:0]	0x0E	RW-xx
LATA	PORTA	Data Output latch	LATA[7:0]	0x10C	RW-xxxx xxxx
LATB	PORTB		LATB[7:0]	0x10D	RW-xxxx xxxx
LATC	PORTC		LATC[1:0]	0x10E	RW-xx
UROD	USART_TX Open-Drain	<u>Open-Drain</u> 1 = Enable 0 = <u>Disable</u>	ODCON0[0]	0x21F	RW-0
CLKOS ¹	CLKO	1 = <u>PB1</u> 0 = <u>PA7</u>	CKAUX[1]	0xF8D	RW-1
AFP0 ¹	TIM1_CH2	1 = <u>PB0</u> 0 = <u>PA1</u>	AFP0[5]	0x19E	RW-0
	TIM2_CH1	1 = <u>PB0</u> 0 = <u>PA5</u>	AFP0[4]		RW-0
	TIM2_CH3	1 = <u>PA3</u> 0 = <u>PB5</u>	AFP0[3]		RW-0
	TIM1_CH1N	1 = <u>PB2</u> 0 = <u>PC0</u>	AFP0[2]		RW-0
	ADC_ETR	1 = <u>PB3</u> 0 = <u>PA4</u>	AFP0[1]		RW-0
AFP1 ¹	<u>USART_TX</u>	00 = <u>PA6</u> 10 = <u>PA7</u> 01 = <u>PB6</u> 11 = <u>PA2</u>	AFP1[5:4]	0x19F	RW-00
	<u>USART_RX</u>	00 = <u>PA7</u> 10 = <u>PA6</u> 01 = <u>PA2</u> 11 = <u>PB6</u>	AFP1[3:2]		
	<u>TIM1_CH4</u>	00 = <u>PB1</u> 10 = <u>PA7</u> 01 = <u>PB1</u> 11 = <u>PA2</u>	AFP1[1:0]		

¹ Pin remapping selection.

Name	Status	Register	Addr.	Reset	
PSINK0	PA7-PA0	<u>Sink Current (mA)</u>	PSINK0[7:0]	0x19A	RW-0000 0000
PSINK1	PB7-PB0	1 = 62	PSINK1[7:0]	0x19B	RW-0000 0000
PSINK2	PC1-PC0	0 = 53	PSINK2[1:0]	0x19C	RW-00
PSRCA[7:0]	PA7-PA0	<u>Source Current (mA)</u>	PSRC0[7:0]	0x11A	RW-1111 1111
		1 = 26			
		0 = 4			
PSRCB[7:0]	PB7-PB0	<u>Source Current (mA)</u>	PSRC1[7:0]	0x11B	RW-1111 1111
		1 = 26			
		0 = 8			
PSRCC[3:2]	PC1	<u>Source Current (mA)</u>	PSRC2[3:0]	0x11C	RW-1111
		11 = 26			
PSRCC[1:0]	PC0	01/10 = 8			
		00 = 4			

Table 2-3 Instruction Level I/O related registers

Name	Status	Register	Addr.	Reset
ITYPE0[1:0]	PORTx.0	<u>External interrupt pin EINTx</u> trigger type	0x11E	RW-00
ITYPE0[3:2]	PORTx.1			RW-00
ITYPE0[5:4]	PORTy.2			RW-00
ITYPE0[7:6]	PORTy.3			RW-00
ITYPE1[1:0]	PORTy.4	0x11F	0x11F	RW-00
ITYPE1[3:2]	PORTy.5			RW-00
ITYPE1[5:4]	PORTy.6			RW-00
ITYPE1[7:6]	PORTy.7			RW-00

Table 2-4 External Pin Interrupt Trigger Type Register (x = A, B, C; y = A, B)

Name	Status	Register	Addr.	Reset
EINT0	00 = <u>PA0</u> 01 = PB0 10 = PC0 11 = Reserved	EPS0[1:0]	0x118	RW-00
EINT1	00 = <u>PA1</u> 01 = PB1 10 = PC1 11 = Reserved	EPS0[3:2]		RW-00
EINT2	00 = <u>PA2</u> 01 = PB2 1x = Reserved	EPS0[5:4]		RW-00
EINT3	00 = <u>PA3</u> 01 = PB3 1x = Reserved	EPS0[7:6]		RW-00
EINT4	00 = <u>PA4</u> 01 = PB4 1x = Reserved	EPS1[1:0]	0x119	RW-00
EINT5	00 = <u>PA5</u> 01 = PB5 1x = Reserved	EPS1[3:2]		RW-00
EINT6	00 = <u>PA6</u> 01 = PB6 1x = Reserved	EPS1[5:4]		RW-00
EINT7	00 = <u>PA7</u> 01 = PB7 1x = Reserved	EPS1[7:6]		RW-00

Table 2-5 External Interrupt Pin Selection Register

Name	Status	Register	Addr.	Reset
EPIE0x	<u>External pin interrupt</u> 1 = Enable 0 = <u>Disable</u>	EPIE0[7:0]	0x94	RW-00000000
EPIF0x ²	<u>External pin interrupt Flag</u> 1 = Yes (latched) 0 = <u>No</u>	EPIF0[7:0]	0x14	R_W1C-00000000

Table 2-6 External Pin Interrupt Enable and Flag Registers

Name	Function	default
MCLRE	External I/O reset	closure
FOSC	<ul style="list-style-type: none"> LP external oscillator across PC1 (+) and PB7 (-) XT external oscillator across PC1 (+) and PB7 (-) EC external oscillator at PC1 (+), PB7 as I/O <u>INTOSCIO</u> : PC1 and PB7 as I/O 	INTOSCIO

Table 2-7 BOOT Level I/O Related Configuration Registers

² Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to only use the STR and MOVWI instructions for write operations, rather than the BSR instructions .

2.2. Configuring the I/O

For each PORT, configures the following 5 modules according to their functions (Table 2-3):

- Digital Output
- Digital Input
- Open-Drain
- Weak Pull-Up
- Weak Pull-Down

• Function	Digital Input	Pull-Up / Pull-Down	Digital Output	Settings
ISP-DATA	On	Off	On	(Built in hardware, ignore instructions)
ISP-CLK	On	Off	Off	(Built in hardware, ignore instructions)
/MCLR _B	On	Pull-Up	Off	(initialize configuration, ignore instructions)
OSC+ (EC)	On	(optional)	Off	(initialize configuration, ignore instructions)
OSC+ / OSC-(LP, XT)	Off	Off	Off	(initialize configuration, ignore instructions)
ADC	Off	Off	Off	TRISx = 1; ANSELAx = 1
LVD	Off ⁽⁵⁾	Off	Off	TRISx = 1; ANSELAx = 1 (except PC1, PB7)
V _{REF+} / V _{REF-}	Off	Off	Off	TRISx = 1
ADC trigger	On	(optional)	Off	TRISx = 1
USART Input	On	(optional)	Off	TRISx = 1
External pin interrupt	On	(optional)	Off	TRISx = 1
BKIN	On	(optional)	Off	TRISx = 1
Digital Input	On	(optional)	Off	TRISx = 1
Clock Output	(ignore)	Off	On	TRISx = 0
PWM	On	Off	On	TRISx = 0
Digital Output	On	Off	On	TRISx = 0
USART Output	On	Off	On	TRISx = 0

Table 2-8 Instruction Level I/O Configuration Flags and Registers

Note:

1. TRISx = 0: "Digital Output" is enabled, "Pull-Up/Pull-Down" is automatically disabled (WPDx, WPUx are ignored).
2. TRISx = 1: "Digital Output" is disabled.
3. ANSELAx = 1: "Pull-Up", "Pull-Down", "Digital Input" are automatically disabled (WPDx, WPUx are ignored).
4. The only instruction that can disable the "Digital Input" is "ANSELAx = 1".
5. When a PORT is set as an LVD input, its "Digital Input", "Pull-Up" and "Pull-Down" functions are automatically disabled. When the LVD input needs to be switched between different channels, the "Digital Input" of the currently unselected channel can be disabled by setting "ANSELAx = 1", but PB7 and PC1 are not control by ANSELAx, and the "Digital Input" cannot be disabled, so it should not only be used as LVD input only part of the time.

6. /MCLR enabled: The Weak Pull-Up function of PC0 is automatically enabled (ignore WPUC[0]); read PORTC[0] as "0".
7. Write to the PORTx data output register or the LATx data latch, and the I/O PORT will output the corresponding logic level. Each group of up to 8 I/O data registers share the common address, and the write operation actually performs a "Read-Modify-Write" operation, that is, first read the PORTx latch value (output or input) or LATx of the group data latches, then modified, and finally written back to the PORTx/LATx data registers.
8. Digital Output and Digital Input functions can coexist, and some applications require both Digital Output and Digital Input to be enabled.
9. ODCON0x = 1: The mapped pins (see "AFP1") selected by "USART_TX function as open-drain output. The open-drain and internal Pull-Up functions can be turned on at the same time.
10. On a full reset or system reset, the PORTx registers will not be reset, but TRISx will be reset to '1', and turn off the output.

For the setting of external pin interrupt, please refer to [Section 9 "Interrupts"](#).

2.3. Pin Out Priority

Each I/O pin is multiplexed with multiple functions. When the corresponding module enables the output, the output priority from low to high is shown in [Table 2-9](#). Since the inputs are connected to individual function modules, there is no priority issue with the inputs.

Name	Priority 0	Priority 1	Priority 2	Priority 3
PA0	PA0	TIM1_CH1	-	-
PA1	PA1	TIM1_CH2	-	-
PA2	PA2	[TIM1_CH4]	ISPCLK	
PA3	PA3	[TIM1_CH3]	-	-
PA4	PA4	TIM2_CH2	-	-
PA5	PA5	LVDOUT	USART_CK	TIM2_CH1
PA6	PA6	USART_TX	-	-
PA7	PA7	[CLKO]	[TIM1_CH4]	-
PB0	PB0	[TIM1_CH2]	[TIM2_CH1]	TIM1_CH3N
PB1	PB1	TIM1_CH2N	TIM1_CH4	CLKO
PB2	PB2	[TIM1_CH1N]	TIM1_CH3	-
PB3	PB3	[LVDOUT]	-	-
PB4	PB4	[LVDOUT]	-	-
PB5	PB5	[LVDOUT]	TIM2_CH3	-
PB6	PB6	[USART_TX]	ISPDAT	-
PB7	PB7	OSC2	-	-
PC0	PC0	TIM1_CH1N	MCLR_B	-
PC1	PC1	OSC1	-	-

Table 2-9 PinOut Priority

For VerA chips, the precautions are as follows:

1. The mapping pin PB0 of TIM1_CH2 can only be used as PWM output and comparison output, rather than capture input;
2. When TIM1_CH2 output is enabled (T1CC2E=1), if AFP0[5] selects PB0, then PA1 is still occupied by TIM1_CH2 function and can be used as input rather than GPIO output;
3. When TIM2_CH1 output is enabled (T2CC1E=1), if AFP0[4] selects PA5, then PB0 is still occupied by TIM2_CH1 function and can be used as input rather than TIM1_CH2 output or GPIO output.

For chips \geq VerB, the above restrictions are not applicable.

3. POWER-ON-RESET (POR)

During Power-On, V_{DD} increases from below the Power-On-Reset Voltage (V_{POR}) to above V_{POR} . V_{DD} may not have completely discharged to 0V when the CPU is Power-On again.

1. The CPU is in a Full-Reset state when V_{DD} is below V_{POR} .
 - a. All calibrated configuration registers are not reset. Special Function Registers (SFR) are in Reset, except INDFx, Z, DC, C, FSRxL/H, BSREG, WREG, PORTx, LATx, OSCTUNE, EEDATL, EEDATH, EECON2 and SRAM (see [Section 14](#) "Special Function Registers"). Registers not reset, such as SRAM, will hold their values until V_{DD} drops below 0.6V (typical). Data of those registers with V_{DD} below 0.6V are undetermined.
 - b. Program Counter = 0x00, Instruction Register = "NOP", Stack Pointer = "TOS" (Top of Stack).
2. BOOT commences when V_{DD} raises above V_{POR} .
3. Instruction execution begins with Program Counter = 0x00 after BOOT completion.

V_{POR} is ~1.6V at 25°C (typical), increasing to ~1.9V at -40°C. For $V_{DD} \geq V_{POR}$, the CPU can function at a reduced speed of 8 MHz / 2T, which giving an automatically adjusted V_{DD} operating range according to the temperature change. This is important for battery-powered system as the CPU can function down even to ~1.6V at typical battery operating environments, greatly extending useful battery life.

Notes:

1. V_{POR} is not configurable.
2. The POR circuit is always on and will perform a Power-On-Reset any time when V_{DD} voltage is below V_{POR} , not just during Power-On.

3.1. BOOT Sequence

Name	Functions	default
PWRTEB	Power-Up-Timer, additional ~64ms delay after BOOT load	disabled

Table 3-1 BOOT configurations

The BOOT configuration is as above. Their values are set at the IDE, not by instructions. during BOOT:

1. CPU idles for ~4ms.
2. The BOOT Level registers are loaded from the non-volatile memory. It takes ~39us. These registers are pre-set at the IDE and not affected by instructions.
3. If Power-On-Timer (PWRT) is enabled, the CPU will idle for ~64ms.

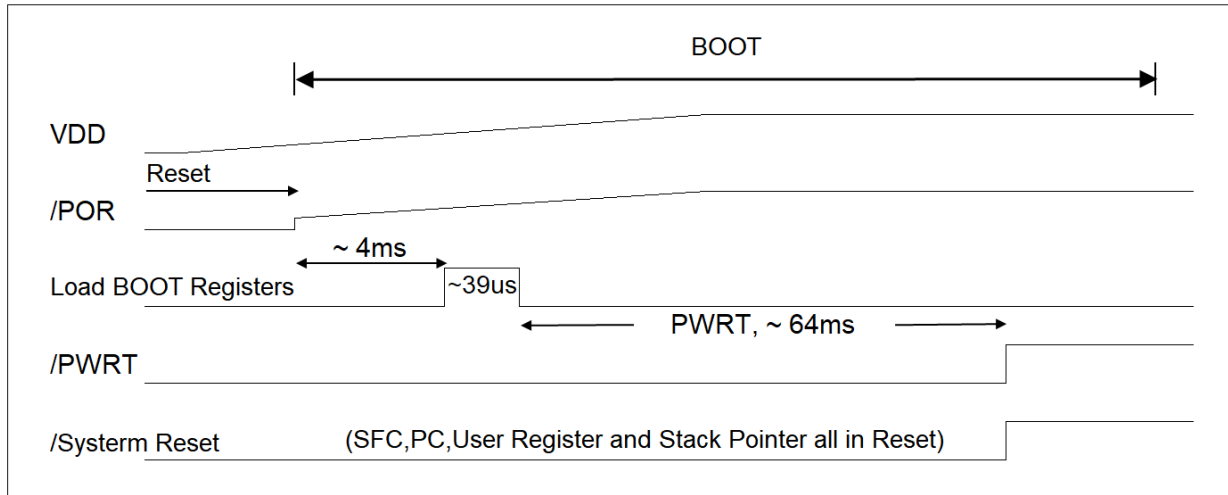


Figure 3-1 Power-On Sequence (PWRT enabled)

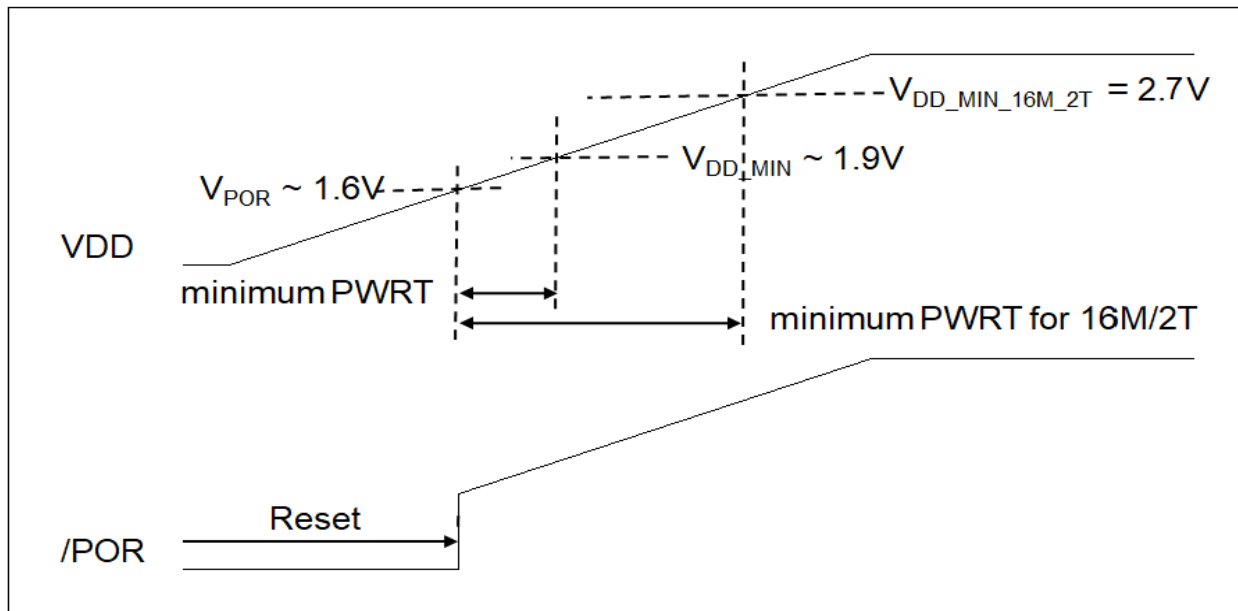


Figure 3-2 Minimum PWRT time required for power-on process

V_{DD} must be higher than 2.7V by the end of BOOT if the CPU is to run at 16MHz / 2T. The total BOOT time can increase from ~4ms to ~68ms by enabling the PWRT, giving more time for the power system to stabilize.

Enable LVR with V_{BOR} ≥ 2.7V for operation at 16MHz / 2T. In addition, the frequency of LVR enable can be controlled by instruction to monitor V_{DD} sporadically, instead of always on (see “LVREN”, “SLVREN”) to reduce power consumption.

Notes:

1. V_{DD} should not rise too slowly. C_{VDD} ≥ 22 µF is discouraged.
2. V_{DD} capacitor of 1 to 10µF is preferred. C_{VDD} < 1µF capacitor may be too small for EFT considerations.
3. If a delay in startup is acceptable, enables PWRT to improve CPU stability.

4. SYSTEM-RESET

System-Reset differs from POR in that it is not a Full-Reset. Depending on the trigger type and configurations, CPU may or may not BOOT. BOOT will wait ~4ms, reload the BOOT registers, and further delay system start by ~64ms if PWRT is enabled. In a System-Reset:

- Registers reset during POR will also be reset during system reset, except BOOT registers.
- Program Counter = 0x00, Instruction Register = "NOP", Stack Pointer = "TOS" (Top of Stack).

The following 7 events besides debugger OCD can be configured to trigger a System-Reset:

1. Brown-Out (BOR / LVR) – always BOOT.
2. Illegal Instructions Reset.
3. Watch-Dog Reset (WDT, CPU not in SLEEP).
4. EMC Reset – always BOOT.
5. Software Reset (execute instruction "RESET").
6. Stack Overflow/Underflow Reset.
7. External I/O (/MCLR) – BOOT if "MRBTE" is set. (≥ VerB chip) .

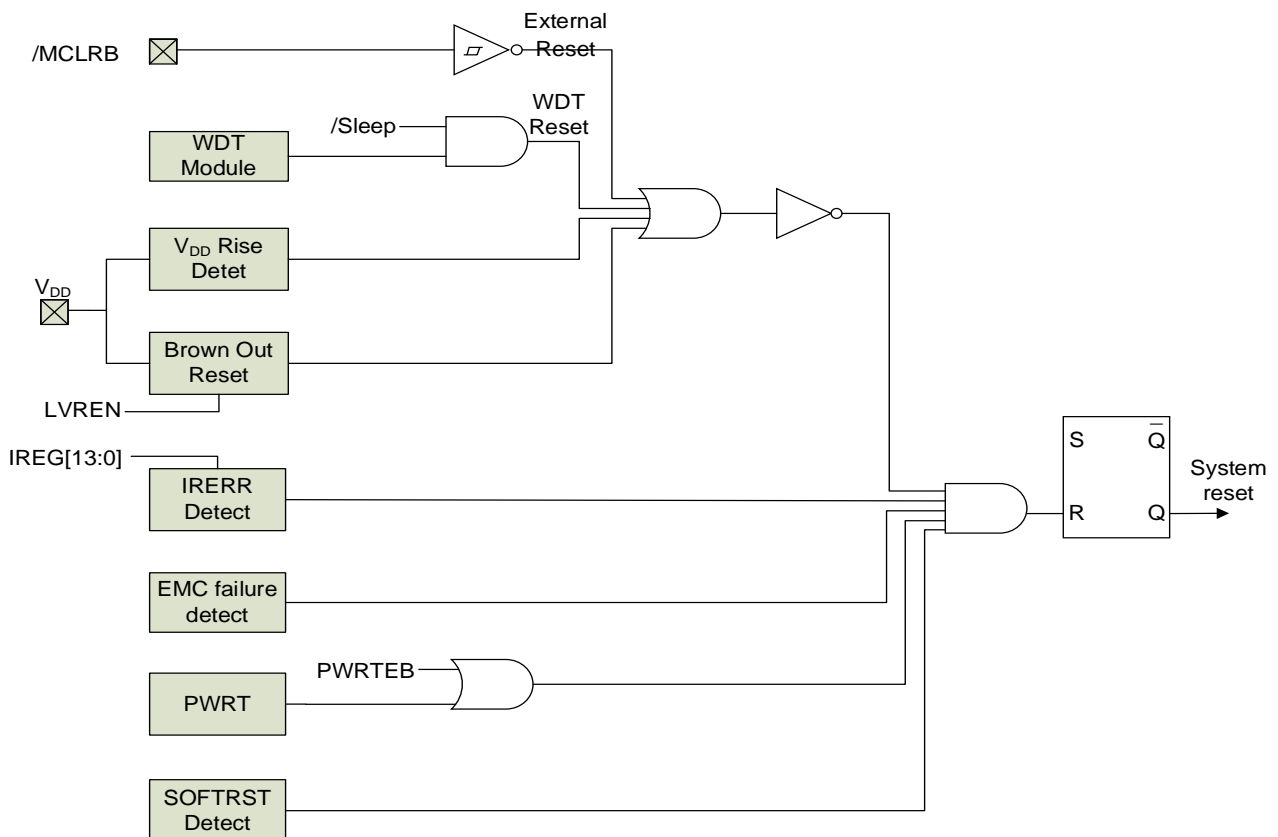


Figure 4-1 Reset circuit Block Diagram

4.1. Summary of SYSTEM-RESET Related Registers

Most settings for System-Reset are configured at the IDE, and cannot be changed by instructions.

Name	Function	default
STVREN	Stack Overflow/Underflow Reset. <ul style="list-style-type: none"> Enabled Disabled 	enabled
LVRS	<u>7 V_{BOR} Voltage levels (V):</u> 2.0 / 2.2 / 2.5 / 2.8 / 3.1 / 3.6 / 4.1	2.0
LVREN	<u>LVR</u> <ul style="list-style-type: none"> Enabled <u>Disabled</u> Enabled except in SLEEP Instruction controlled (SLVREN) 	disabled
WDTE	<u>WDT</u> <ul style="list-style-type: none"> Enabled (Instructions can not be disabled) <u>Instruction controlled (SWDTEN)</u> 	SWDTEN control
MCLRE	Reset by External I/O	disabled

Table 4-1 BOOT Level RESET related configurations

4.2. Brown-Out Reset (LVR / BOR)

Brown-Out occurs when V_{DD} falls below a pre-configured Brown-Out Voltage (V_{BOR}) for a time longer than T_{BOR}. T_{BOR} takes 3 to 4 LIRC clock cycles (~94 – 125µs, LIRC will turn on automatically if not already). CPU System-Reset as long as V_{DD} ≤ V_{BOR}. Once V_{DD} > V_{BOR} CPU will BOOT. The /BORF will be set to 0.

While V_{POR} is fixed, V_{BOR} can be set to 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1V (see “LVRS” in [Table 4-1](#)).

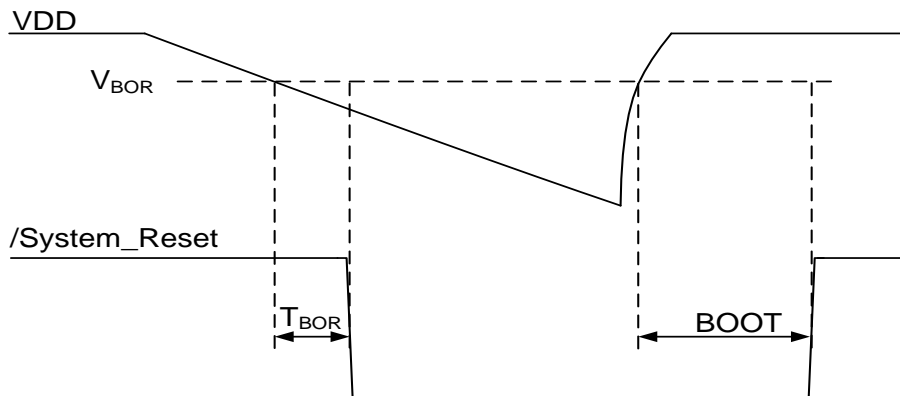


Figure 4-2 LVR BOOT Timing Diagram

LVR function can have four different settings configured (see “LVREN” in [Table 4-1](#)).

1. LVR enabled.

2. LVR disabled.
3. LVR enabled, except in SLEEP.
4. Let instructions enable or disable LVR (SLVREN, see [Table 4-2](#)).

Note: LVR can be instructions disabled in SLEEP to reduce power consumption. The CPU should wake up and enable LVR periodically to monitor V_{DD} if system V_{DD} is unstable.

Name	Status	Register	Addr.	Reset
SLVREN ¹	<p><u>Only applicable to LVREN configured to control LVR by the SLVREN</u></p> <p>1 = Enable LVR 0 = <u>Disable LVR</u></p>	LVDCON0[7]	0x199	RW-0

Table 4-2 Instruction Level LVR registers

4.3. Illegal Instruction Reset

There are many reasons for CPU fetch instruction errors, and the most common reasons are interference and V_{DD} instability.

Although there is no dedicated Reset instruction, any deliberate illegal instruction is equivalent to a Reset instruction. BOOT after an Illegal Instruction and the Flag IERRF will be set to 1 .

4.4. Software Reset

When the program executes Software Reset instruction "RESET", a system reset is generated and the flag /SRSTF will be set to 0.

4.5. Stack Overflow/Underflow Reset

The Stack Overflow or Underflow Reset (by configuring " STVREN") will trigger a System-Reset, and the Overflow Flag STKOVF or Underflow Flag STKUNF will be set to 1.

4.6. EMC Reset

The EMC detection module is always on. When some kind of EMC interference occurs, System-Reset and BOOT generate, and the Flag EMCF will be set to 1.

4.7. Watch Dog Timer (WDT) Reset

WDT overflows during SLEEP will result in a Wake-Up.

In normal mode (not SLEEP mode), a WDT overflow will trigger a System-Reset. And WDT reset can be used to reset a hung CPU. Clear WDT from time to time in the program to avoid false reset.

For details on WDT operation and setting see [Section 7.1](#) Watch Dog Timer (WDT).

¹This bit will not be cleared when a Brown-out Reset occurs. Other resets will clear this bit.

4.8. External I/O System-Reset /MCLR

The CPU can be reset by a low voltage applied to the /MCLR (PC0) pin if so configured by BOOT. The /MCLR pin is usually weak pullup to V_{DD} with a resistor instead of directly, as shown in Figure 4-3. The external RC network also provides glitches filtering and over-current protection.

For ≥ VerB chips, BOOT after a /MCLR System-Reset.

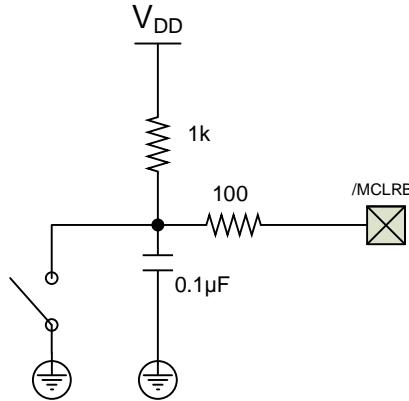


Figure 4-3 /MCLR reset circuit

4.9. Detect the Type of Last Reset

Eight status flags in the PCON register and the different combinations of Time Out (/TO) and Power Down (/PD) can trace the type of last System-Reset. /BORF should be set to 1 by instructions, and will be latches to “0” after the Reset.

Name	Status	Register	Addr.	Reset
STKOVF ²	Stack Overflows Flag	PCON[7]	0x96	RW0-0
STKUNF ²	Stack Underflows Flag	PCON[6]		RW0-0
EMCF ²	EMC Reset Flag	PCON[5]		RW0-0
IERRF ²	Illegal Instruction Flag	PCON[4]		RW0-0
/MCLR ³	External Reset Flag	PCON[3]		RW1-1
/SRSTF ³	Software Reset Flag	PCON[2]		RW1-1
/PORF ³	Power-On-Reset Flag	PCON[1]		RW1-0
/BORF ³	Low-voltage Reset Flag	PCON[0]		RW1-x

Table 4-3 Reset Flag Register

² Write '0' to clear, and writing '1' has no effect on the bit value.

³ Only '1' can be written, and writing '0' has no effect on the bit value..

Reset Source	STKOVF	STKUNF	EMCF	IERRR	/MCLRR	/SRSTF	/PORF	/BORF	/TO	/PD
	PCON[7]	PCON[6]	PCON[5]	PCON[4]	PCON[3]	PCON[2]	PCON[1]	PCON[0]	STATUS[4]	STATUS[3]
	0x96								Bank First address + 0x03	
POR	0	0	0	0	1	1	0	1	1	1
LVR	0	0	0	0	1	1	1	0	-	-
CLRWDT Instructions	-	-	-	-	-	-	-	-	1	1
SLEEP Instructions	-	-	-	-	-	-	-	-	1	0
WDT overflows while not in SLEEP (Reset)	-	-	-	-	-	-	-	-	0	-
WDT overflows while in SLEEP (Wake up)	-	-	-	-	-	-	-	-	0	0
Software Reset	-	-	-	-	-	0	-	-	-	-
MCLR Reset (\geq verB)	0	0	0	0	1	1	0	1	1	1
MCLR Reset ($<$ verB)	-	-	-	-	0	-	-	-	-	-
Illegal Instruction Reset	-	-	-	1	-	-	-	-	-	-
EMC Reset	-	-	1	-	-	-	-	-	-	-
Stack Underflow Reset	-	1	-	-	-	-	-	-	-	-
Stack Over flow Reset	1	-	-	-	-	-	-	-	-	-
On-Chip Debugger (OCD)	-	-	-	-	-	-	-	-	-	-

Table 4-4 Reset Related Status Flags ("-" no change)

5. LOW VOLTAGE DETECT / COMPARATOR (LVD)

LVD works similarly to a LVR except for the followings:

- None of the control and setting parameters are set by BOOT. They are set by instructions.
- I/O must be set appropriately: $TRISx = 1$; $ANSELAx = 1$ (Not applicable to PB7 and PC1, when PB7 and PC1 are configured as inputs but are not selected as LVD inputs and the port voltage is not VDD or GND, there may be leakage from the digital input module.)
- LVD will set LVDW instead of /BOR.
- It can be instructions configured to Interrupt. It will not trigger System-Reset.
- LVDDEB enables debouncing. Debouncing Time (T_{LVD}) is 3 – 4 LIRC cycles (LIRC turns on automatically if not already so).
- The input to the LVD module can be configured to V_{DD} or four other I/O. The latter allows the LVD to function as a single input comparator to one of the six LVDL levels ($V_{LVD-REF}$).
- The polarity of LVD can be set, such that the LVD can be a “High” or a “Low” comparator to $V_{LVD-REF}$.
- Six selectable LVD Voltage (LVDL), with ~2%/step tunable by instructions.
- LVDL can be output to pins (see "LVDOE" and "LVDOS").
- The External Reset MCLR of PC0 has higher priority than ELVD. When configured as an External Reset pin, the ELVD detection is inactive.

5.1. Summary of LVD Related Registers

Name	Status	Register	Addr.	Reset	
LVDM	<u>LVD Input</u> 1 = External pin (ELVDx) 0 = VDD	LVDCON0[6]	0x199	RW-0	
LVDEN	<u>LVD</u> 1 = Enable 0 = <u>Disable</u>	LVDCON0[4]		RW-0	
LVDW	<u>LVD triggreed Flag</u> 1 = Yes (no latch) 0 = <u>No</u>	LVDCON0[3]		RO-0	
LVDL	<u>V_{LVD-REF}</u> 000 = <u>Reserved</u> 100 = 2.8 001 = <u>Reserved</u> 101 = 3.0 010 = 2.0 110 = 3.6 011 = 2.4 111 = 4.0	LVDCON0[2:0]		RW-0 00	
LVDP	<u>LVDW Polarity</u> 1 = Detection voltage > V _{LVD-REF} 0 = <u>Detection voltage < V_{LVD-REF}</u>	LVDCON1[4]	0xF8E	RW-0	
LVDDDEB	<u>LVD debouncing</u> 1 = Enable 0 = <u>Disable</u>	LVDCON1[3]		RW-1	
LVDOE	<u>LVD Output</u> 1 = Enable 0 = <u>Disable</u>	LVDCON1[2]		RW-0	
LVDOS	<u>LVD Pinout</u> 00 = PA5 10 = PB4 01 = PB5 11 = PB3	LVDCON1[1:0]		RW-0 0	
LVDCAL	Each step adjust LVDL by ~2%		LVDTUNE[7:4]	0xF92	RW-1 000
ELVDS	<u>LVD External Input Pin Selection</u> 00 = <u>ELVD0</u> 10 = ELVD2 01 = ELVD1 11 = ELVD3	ADCON3[1:0]	0x41A	RW-0 0	
LV DIE	<u>LVD Interrupt</u> 1 = Enable 0 = <u>Disable</u>	INTCON[4]	0x0B	RW-0	
LV DIF ¹	<u>LVD Interrupt Flag</u> 1 = Yes 0 = <u>No, or cleared</u>	INTCON[1]		R_W1 C-0	

Table 5-1 Instruction Level LVD Settings and Flags

¹ Write 1 is cleared, write 0 is invalid. It is recommended that only STR and MOVWI instructions be used for write operations, not BSR or IOR instructions.

6. OSCILLATORS and SYSCLK

Instruction chooses whether SysClk is the internal oscillator HIRC, internal oscillator LIRC, or one of the three external oscillators (EC, LP, XT, see “SCS” in [Table 6-2](#)). If external oscillator is chosen, BOOT level “FOSC” ([Table 6-1](#)) will determine which one of the three external oscillators is used. Instructions also select the frequency step down divider for internal oscillator (see MCKCF in [Table 6-2](#)). SysClk is used to derive the Instruction Clock:

$$\text{Instruction Clock} = \text{SysClk} / N; N = 2 \text{ for } 2T, 4 \text{ for } 4T.$$

The pin assignments for external clock inputs are set by BOOT (see FOSC). Eight clock sources can be selected for output by instructions (see “CCOSEL” and “CCOEN”). When the clock output is enabled, the selected clock source is automatically turned on, the flag CCORDY is set to 1, and the pinout can be selected as PA7 or PB1 (see “CLKOS”, [Table 6-3](#)).

Peripheral Timers, ADC, and USARTx have independent SYSCLK selection (see “PCKEN”). The module clock needs to be enabled before the corresponding module can be enabled. When shutting down, turn off the module function before the module colck can be turned off. In addition, the count clock source of Timers and the conversion clock source of ADC have independent oscillators. When both the module system clock and the module function are enabled, the selected oscillator will turn on automatically and remain effective during the operation of the module. Therefore, multiple oscillators can operate simultaneously.

As instructions are halted in SLEEP, so will Instruction Clock by default, and the clock output is suspended. When SYSON=1, the instruction clock will keep active, so the corresponding peripherals of the enable module system clock will also keep active in SLEEP, and the clock output will continue.

Note:

1. When SYSON = 1 and TIMxEN = 1 in SLEEP, the count clock source selected by Timers will keep active.
2. When LIRC is selected as the ADC conversion clock source, LIRC will remain active after entering SLEEP, independent of SYSON.
3. It is recommended to turn off the clock modules that do not use peripherals to reduce power consumption.

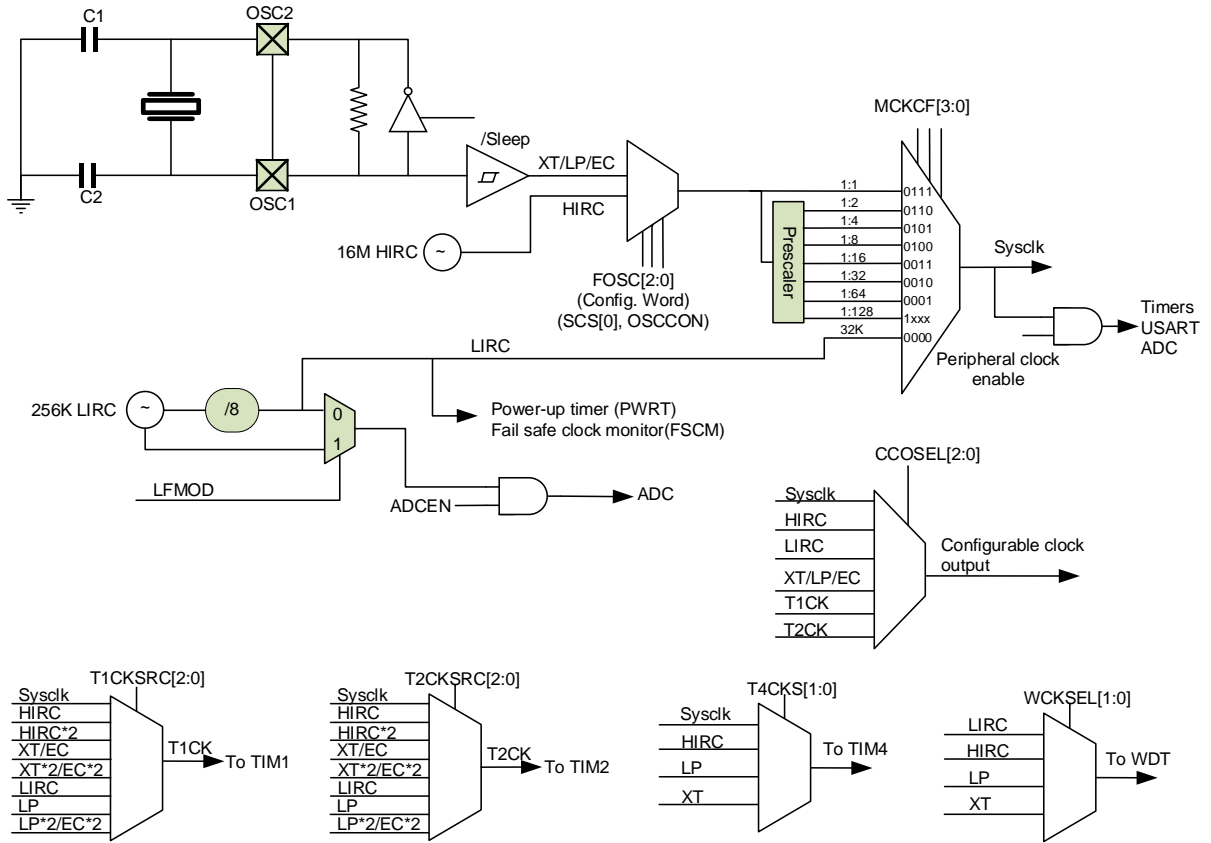


Figure 6-1 Clock source Block Diagram for SysClk

6.1. Summary of Oscillator Modules Related Registers

Name	Functions	default
FOSC	<ul style="list-style-type: none"> LP external low-speed oscillator across PC1 (+) and PB7 (-) XT external high-speed oscillator across PC1 (+) and PB7 (-) EC external oscillator at PC1 (+), PB7 as I/O <u>INTOSCIO</u> : PC1 and PB7 as I/O 	INTOSCIO
IESO	<u>Two-speed Startup for XT and LP</u>	<ul style="list-style-type: none"> Enable
FSCMEN	<u>Fail-Safe Clock Monitor</u>	<ul style="list-style-type: none"> Disable
TSEL	<u>Correspondence between system clock and instruction clock (1T, 2T or 4T)</u> <ul style="list-style-type: none"> 1 (Instruction Clock = SysClk) <u>2</u> (Instruction Clock = SysClk/2) 4 (Instruction Clock = SysClk/4) 	2
OSTPER	OST Timer Period Selection (XT / LP apply)	<ul style="list-style-type: none"> 512 <u>1024</u> 2048 4096 (32768 in LP mode)

Table 6-1 BOOT Level FOSC and 2-speed Start-Up configurations

SysClk Source		Configuration		
		SCS	LFMOD	OST
		OSCCON[0]	TCKSRC[7]	(Optional, see OSTPER)
		0x99	0x31F	
		RW-0	RW-0	
External	EC	0	-	-
	XT	0	-	1,024 (default)
	LP	0	-	1,024 (default)
Internal	HIRC	16 MHz	1	-
	LIRC	256 kHz ¹	1	1
		32 kHz ²	1	0

Name	Status	Register	Addr.	Reset		
MCKCF	SysClk divider (EC/XT/LP/HIRC)			OSCCON[7:4]	0x99	RW-0011
	0111 = 1	0100 = 8	0001 = 64			
	0110 = 2	0011 = <u>16</u>	1xxx = 128			
	0101 = 4	0010 = 32	0000 = LIRC			

Table 6-2 Instruction Level SysClk source setup

¹ 256 kHz LIRC is used only for ADC only (see ADCS and LFMOD, [Table 11-3](#)).

² Sysclk source (MCKCF = 0000), PWRT, LIRC and HIRC cross-calibration, FSCM, WDT (WCKSRC = 00), Timer1 (T1CKSRC = 101), Timer2 (T2CKSRC = 101), and clock output (CCOSEL = 010) use the 8-frequency division of LIRC ,i.e.32 kHz , regardless of the value of LFMOD.

Name	Status	Register	Addr.	Reset
OSTS	<u>Oscillator Start-Up Time-out (latched) Status</u> 1 = Running from the external clock (start-up successful) 0 = Running from the internal oscillator	OSCCON[3]	0x99	RO-0
HTS	<u>HIRC ready (latched) Flag</u> 1 = Yes 0 = <u>No</u>	OSCCON[2]		RO-0
LTS	<u>LIRC ready (latched) Flag</u> 1 = Yes 0 = <u>No</u>	OSCCON[1]		RO-0
SYSON	<u>In SLEEP mode, the Sysclk controlled</u> 1 = Keep active 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
CCORDY	<u>Clock Output Flag</u> 1 = Yes 0 = <u>No</u>	CKOCON[6]		RO-0
DTYSEL	<u>TIM1/TIM2 Multiplier Clock Duty Cycle Adjustment Bit</u> 00 = 2ns delay 10 = <u>4ns delay</u> 01 = 3ns delay 11 = 7ns delay	CKOCON[5:4]		RW-10
CCOSEL	<u>Clock Output Selection</u> 000 = <u>Sysclk</u> 100 = T1CK 001 = HIRC 101 = T2CK 010 = LIRC 110 = LP ^(*) 011 = XT ^(*) 111 = EC ^(*) ^(*) FOSC should be configured to LP/XT/EC mode, otherwise the clock output may be incorrect or no output;	CKOCON[3:1]		RW-000
CCOEN	<u>Clock Output</u> 1 = Enable 0 = <u>Disable</u>	CKOCON[0]		RW-0
CLKOS ³	<u>Clock Output Pin</u> 1 = <u>CLKO map to PB1</u> 0 = CLKO map to PA7	CKAUX[1]	0xF8D	RW-1
CKMAVG	<u>4x averaging for LIRC and HIRC Cross Calibration</u> 1 = Enable 0 = <u>Disable</u>	MSCKCON[1]	0x41D	RW-0

³ Before modifying CLKOS, the EECON1.CFGS needs to be set to 1. After write operation, EECON1.CFGS need to be cleared.

Name	Status	Register	Addr.	Reset
CKCNT1	<u>Start the LIRC and HIRC Cross calibration function Calibration</u> 1 = Start 0 = <u>Finished (auto-cleared)</u>	MSCKCON [0]		RW-0
SOSCPR	<u>LIRC Period Calibrated by number of HIRC clocks</u>	SOSCPR[11:0]	0x41F[3:0] 0x41E[7:0]	RW-FFF
TUN	Internal HIRC frequency tunable register	OSCTUNE[7:0]	0x98	RW-xxxx xxxx
UARTEN	USART Clock module	PCKEN[5]	0x9A	RW-0
TIM4EN	Timer4 Clock module	PCKEN[3]		RW-0
TIM2EN	Timer2 Clock module	PCKEN[2]		RW-0
TIM1EN	Timer1 Clock module	PCKEN[1]		RW-0
ADCEN	ADC Clock module	PCKEN[0]		RW-0

Table 6-3 Oscillators Control/Status

Name	Status	Register	Addr.	Reset
GIE	<u>Global Interrupt</u> 1 = Enable (PEIE, OSFIE, CKMIE apply) 0 = <u>Global Shutdown</u> (Wake-Up not affected)	INTCON[7]	Bank First address +0x0B	RW-0
PEIE	<u>Peripheral Interrupt Enable</u> 1 = Enable (OSFIE, CKMIE apply) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0
OSFIE	External Oscillator Failed Interrupt 1 = Enable 0 = <u>Disable</u> (no Wake-Up)	INTCON[3]		RW-0
OSFIF ⁵	External Oscillator Failed Interrupt Flag 1 = Yes (latched) 0 = <u>No</u>	INTCON[0]		R_W1C-0
CKMIE	LIRC and HIRC Cross Calibration Completion Interrupt 1 = Enable 0 = <u>Disable</u> (no Wake-Up)	PIE1[1]	0x91	RW-0
CKMIF ⁴	LIRC and HIRC Cross Calibration Completion Flag 1 = Yes (latched) 0 = <u>No</u>	PIR1[1]	0x11	R_W1C-0

Table 6-4 Oscillators Interrupt Enable and Status Bits

⁴ Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended that only STR and MOVWI instructions be used for write operations, not BSR or IOR instructions.

6.2. Internal Clock Modes (HIRC and LIRC)

Internal high frequency clock (HIRC) is factory calibrated to 16 MHz @ 2.5V/25°C. Typical value of frequency change between chips < ±1.5% at 2.5 – 5.5V, 25°C. The typical temperature variation from -40 – +85 °C is ±2.0%.

HIRC accuracy is calibrated at the wafer level. Packaging may cause the HIRC frequency to drift. There is an option at the downloader to re-calibrate the HIRC. The HIRC frequency trimmed value is stored in the “OSCTUNE” register. Users can change HIRC from the default 16 MHz (tuning). Trimming steps are non-linear (~40 kHz). A rough estimation is as follows:

$$OSCTUNE[7:0] \pm N \approx 16000 \pm N * 40 \text{ (kHz)}$$

Internal low frequency clock (LIRC) is factory calibrated to 32 kHz. Typical die to die variations is <±9.5% at 2.5 – 5.5V, 25°C. The temperature variation from -40 – +85 °C is < ±3.0%.

LIRC and HIRC can be used to cross calibrate each other – A build in hardware uses Timer2 to measure the number of Instruction Clocks (set SysClk to HIRC at 16MHz) in one LIRC period (32 kHz).

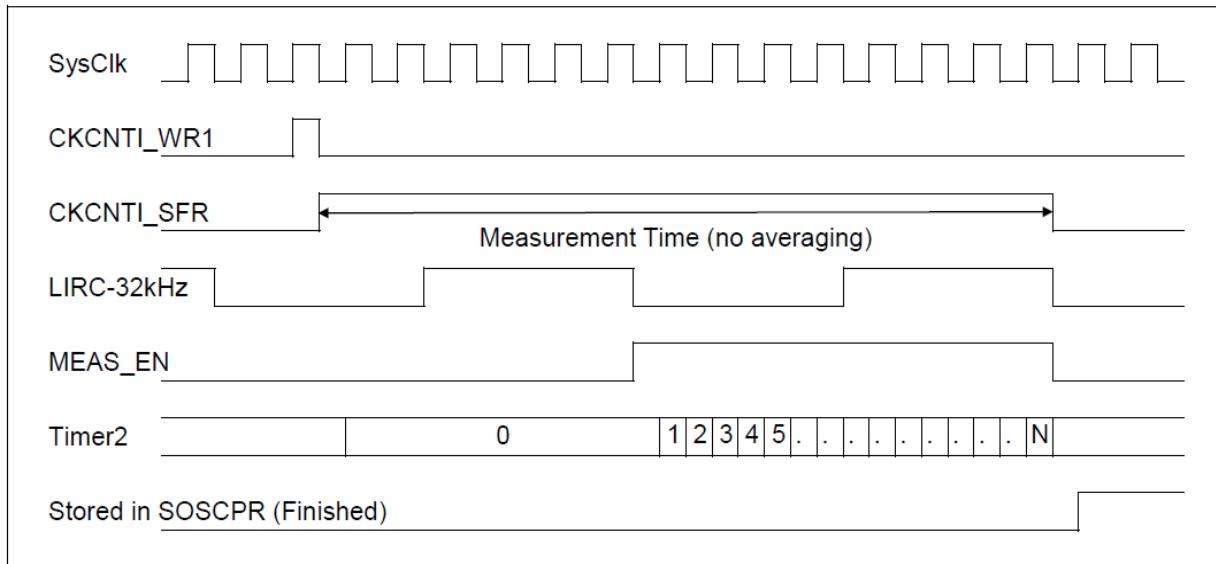


Figure 6-2 Single measurement Timing Diagram

To enable LIRC and HIRC Cross Calibration:

1. Set MCKCF = 111, SCS = 1 ; select SysClk at 16MHz HIRC (other settings will have a lower accuracy).
2. Set CKMAVG = 1 ; 4 times averaging, choose 0 for no averaging.
3. Set TIM2EN = 1, T2CEN = 1 ; enable Timer2.
4. Set CKCNTI = 1 ; start calibration, automatically Timer2 prescaler = 1, postscalar = 1, T2CKSRC = HIRC
5. At the end of the calibration “CKCNTI =0”, “CKMIF = 1” automatically.
6. Measured value is stored at SOS CPR;
7. LIRC is 32kHz and CPU is running at 16MHz / 2T, the ideal matching number is 500.

Notes:

- Do not write SOSCPRH/L during LIRC and HIRC Cross Calibration.
- Timer2 cannot be used by other peripherals during LIRC and HIRC Cross Calibration.
- LIRC and HIRC Cross Calibration is incompatible with Single Step Debugger mode.
- When CKCNTI = 1, LIRC is automatically turned on and keeps running in SLEEP mode, and only when SYSON = 1 for calibration to run in SLEEP mode.
- After power on, LIRC and HIRC Cross Calibration will turn on automatically. At this time, CKCNTI=1, CKMAVG=0, no need to set T2CEN. After the automatic cross calibration is completed, the CKMIF flag will not be set, and the CKCNTI will be reset automatically before TIM2 can be configured or used by other peripherals.

6.3. External Clock Modes

6.3.1. EC mode

External digital signal connected to OSC1 is the clock source (OSC2 is available for I/O). There is no set up or transition time delay when EC is used for SysClk after a POR or a wake-up from sleep.

6.3.2. LP and XT modes

A quartz crystal resonator or ceramic resonator is connected between OSC1 and OSC2 in LP or XT modes.

LP Oscillator mode has the lowest gain setting and current consumption of the three modes (EC, LP and XT). This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the highest gain setting of the internal inverter-amplifier.

After a BOOT or a Wake-Up from Sleep, CPU program execution is suspended during OST counting if the clock source is XT or LP mode. This allows the XT or LP clock to stabilize. OST counts OSC1 (+ve terminal of the crystal input) in XT and LP mode. The number of counts is determined by the initialization configuration register OSTPER. For a 32.768 kHz tuning-fork type crystals the OST time is at least 1 second when OSTPER=32.768.

Notes:

- WDT is held in cleared until OST finished counting.
- Do not write WDTCON / OPTION during OST counting, otherwise unexpected behavior will occur.

Two-Speed Clock Start-up (see “IESO” in [Table 6-1](#)) allows instructions execution while OST counts, using the internal oscillator INTOSC as SysClk. It removes the external oscillator start-up time from the time spent awake and can reduce the overall power consumption, especially in cases of frequent SLEEP mode usage. The CPU wakes up from Sleep, performs a few instructions using the INTOSC as SysClk and return to Sleep without having to wait for the primary oscillator to become stable.

Note: Two-Speed Start-up is disabled for EC mode, as the oscillator does not require stabilization time.

Two Speed Start-up sequence

1. After a BOOT or Wake-up from Sleep.
2. INTOSC is used as SysClk for Instructions execution until OST time out.
3. SysClk is held low from the falling edge of INTOSC until the falling edge of the new clock (LP or XT mode).
4. SysClk switches to the external clock source.

The Oscillator Start-up Time-out Status (OSTS) indicates whether the SysClk is running from the external clock source or from the internal clock source. This is an indirect way to find out if the Oscillator Start-up Timer (OST) has timed out for the LP or XT mode when the Two-Speed Clock Start-up mode is on.

Executing a SLEEP instruction will abort the OST, and OSTS will remain “0”.

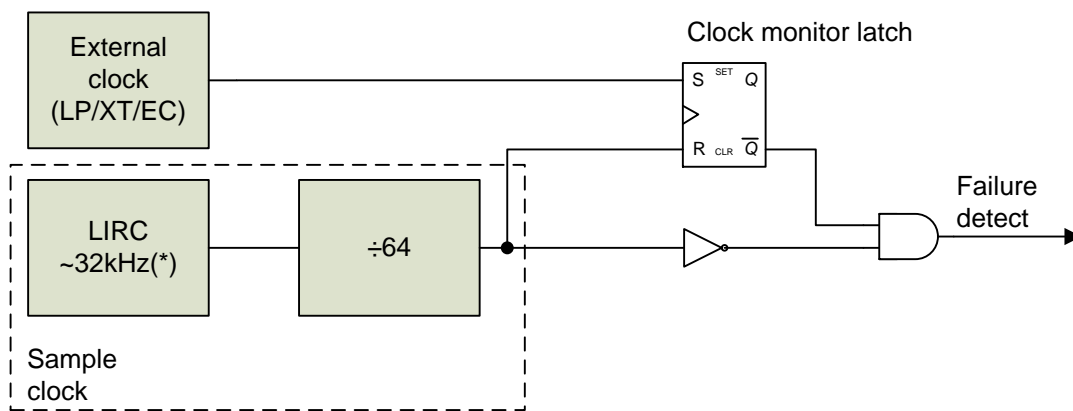
Fail-Safe Clock Monitor (FSCM, enabled by “FSCMEN”, see [Table 6-1](#)) allows the device to continue operating should the external oscillator fails. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is applicable to all external oscillator modes (EC, LP

and XT). It is recommended that FSCM be enabled if an external oscillator is used.

An external oscillator is considered fail if it oscillates at ~1 kHz or below. A sample clock is generated by dividing the LIRC by 64. The external clock sets a latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is when an entire half-cycle of the sample clock elapses without the primary clock goes low.

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets OSFIF. Setting OSFIF to 1 will generate an interrupt if OSFIE is enabled. The device hardware can then take steps to mitigate the problems that may arise from a failed clock. The SysClk will continue to be sourced from the internal clock source until the device hardware successfully restarts the external oscillator.

The internal clock source chosen by “FSCM” is determined by “MCKCF”. This allows the internal oscillator to be configured before a failure occurs.



Note: LFMOD does not affect the sample clock.

Figure 6-3 FSCM Block Diagram

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or toggling the SCS. When SCS is toggled, OST is restarted. While OST is running, CPU selects INTOSC modes as Sysclk to continue executing instructions. When OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be resolved before the OSFIF flag is cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, will not update SCS. The program can monitor OSTs to determine the current SysClk source.

6.4. HIRC, LIRC and EC inter-switching

Figure 6-4 shows the timing during inter-switching. If either HIRC or LIRC is shutdown prior to switching (to save power) there is an extra oscillator setup delay time, HTS and LTS indicate the status of the corresponding oscillator respectively.

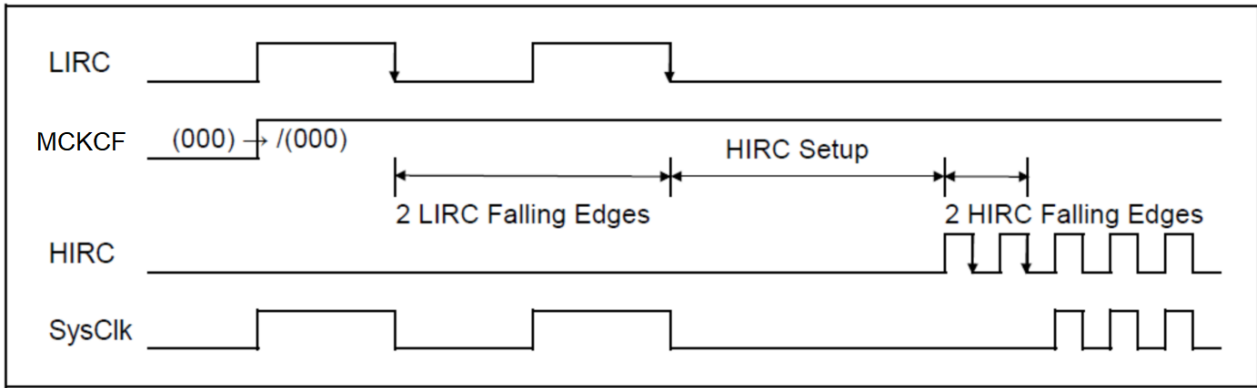


Figure 6-4 Switching from LIRC to HIRC (same principle applies switching among EC, LIRC, HIRC)

7. TIMERS

There are 4 Timers including the Watch Dog Timer (WDT).

	WDT	Timer1	Timer2	Timer4
Prescaler (bit)	3	16	4 (1x, 4x, 16x)	3
Counter (bit)	16	16	16	8
Postscaler (bit)	–	–	–	–
Clock Sources	<ul style="list-style-type: none"> • LP • XT • HIRC • <u>LIRC</u> 	<ul style="list-style-type: none"> • EC, LP or XT • HIRC • <u>Sysclk</u> • LIRC • 2x HIRC • 2x (EC, LP or XT) 	<ul style="list-style-type: none"> • EC, LP or XT • HIRC • <u>Sysclk</u> • LIRC • 2x HIRC • 2x (EC, LP or XT) 	<ul style="list-style-type: none"> • LP • XT • HIRC • <u>Sysclk</u>

Table 7-1 Timers' Resources

Notes: If a Timer's clock source is not the system Clock, set "TxCEN = 0" before changing TMRx.

Any Timer enabled will turn on its clock source automatically. System Clock is disabled at SLEEP so it cannot be used for WDT. When LP / XT / EC oscillator is selected as Timers' clock source, FOSC must be configured correspondingly, otherwise the oscillator is off and no counting will occur.

In a POR or System-Reset, all Timers' counter and prescaler are reset. The followings will also reset a Timer's counter and scaler(s):

	WDT	Timer1	Timer2	Timer4
Prescaler	<ul style="list-style-type: none"> • WDT disabled 	<ul style="list-style-type: none"> • Reset mode 	<ul style="list-style-type: none"> • T2CEN = 0 	<ul style="list-style-type: none"> • T4CEN = 0
Counter	<ul style="list-style-type: none"> • WDT, OST overflow • Enters/Exits SLEEP • CLRWDT • WDTCON write • WCKSEL write 	<ul style="list-style-type: none"> • T1CNT = T1ARR 	<ul style="list-style-type: none"> • T1CNT=T2ARR 	<ul style="list-style-type: none"> • T4CNT = T4ARR

Table 7-2 Events resetting a Timers' Counter and Scaler(s)

7.1. Watch Dog Timer (WDT)

WDT is used to "Wake-Up from SLEEP" or "System-Reset if the CPU suspend". WDT counts the number of clock cycles to a pre-set number until overflow.

- In SLEEP mode, a WDT overflow will trigger a Wake-up. The CPU will resume operation from where it is before SLEEP. This is not an Interrupt nor System-Reset event.
- In non-SLEEP mode, a WDT overflow will trigger a System-Reset and BOOT (see [Section 4](#) System-Reset).

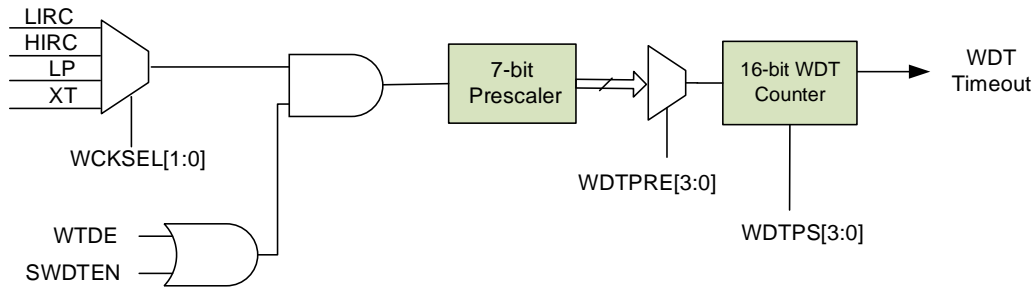


Figure 7-1 Block Diagram of WDT

The WDT will overflow after a WatchDog-Time: WDT-Period x WDT-Prescaler / WDT Clock Frequency.

For a given Clock Source, WatchDog-Time step is a continuous multiple due to the binary nature of the WDT Prescaler. Using LIRC as clock source, the maximum settable time before WDT overflows is

$$2^{16} \times 2^7 / 32\text{kHz} = \sim 262 \text{ seconds}$$

7.1.1. Summary of WDT Related Registers

Name	Functions	Default
WDTE	<u>WDT</u> <ul style="list-style-type: none"> Enabled (Instructions can not be disabled) <u>Instruction controlled (SWDTEN)</u> 	SWDTEN control

Table 7-3 BOOT Level WDT Selectors

Name	Status	Register	Addr.	Reset
WCKSEL	<u>WDT Clock Sources</u>		0x11C	RW-00
	00 = LIRC 01 = HIRC 10 = LP (only FOSC in LP or INTOSCIO mode*) 11 = XT (only FOSC in XT or INTOSCIO mode*) *Otherwise misconfigured, no WDT Clock Source	MISC0[1:0]		
WDTPRE	<u>WDT Prescaler</u>		0x97	RW-111
	000 = 1 001 = 2 010 = 4 011 = 8	100 = 16 101 = 32 110 = 64 111 = <u>128 (default)</u>		
WDTPS	<u>WDT Period</u>		0x97	RW-0100
	0000 = 32 0001 = 64 0010 = 128 0011 = 256 0100 = <u>512 (default)</u> 0101 = 1,024 0110 = 2,048	0111 = 4,096 1000 = 8,192 1001 = 16,384 1010 = 32,768 1011 = 65,536 11xx = 65,536		
SWDTEN	1 = WDT Enables 0 = <u>WDT Disables</u> (if WDTE choosed SWDTEN control)	WDTCON[0]		RW-0

Table 7-4 Instruction Level WDT Related Registers

7.1.2. Configuration and using the WDT

WDTE (BOOT Level) and/or SWDTEN (Instruction Level) enable the WDT. After a WDT triggered Reset, it will also BOOT.

The WDT prescaler is set by WDTPRE, and the clock source is selected by WCKSEL (default at 32kHz if the LIRC is selected, regardless of the value of LFMOD). When the WDT enabled, the selected clock source is automatically turned on and will remain active in SLEEP mode.

To stop a WDT overflow, the WDT must be cleared before time expires. Refer to [Table 7-2](#) for events that will clear the WDT. Counting continues after WDT is cleared.

7.2. Advanced TIMER1

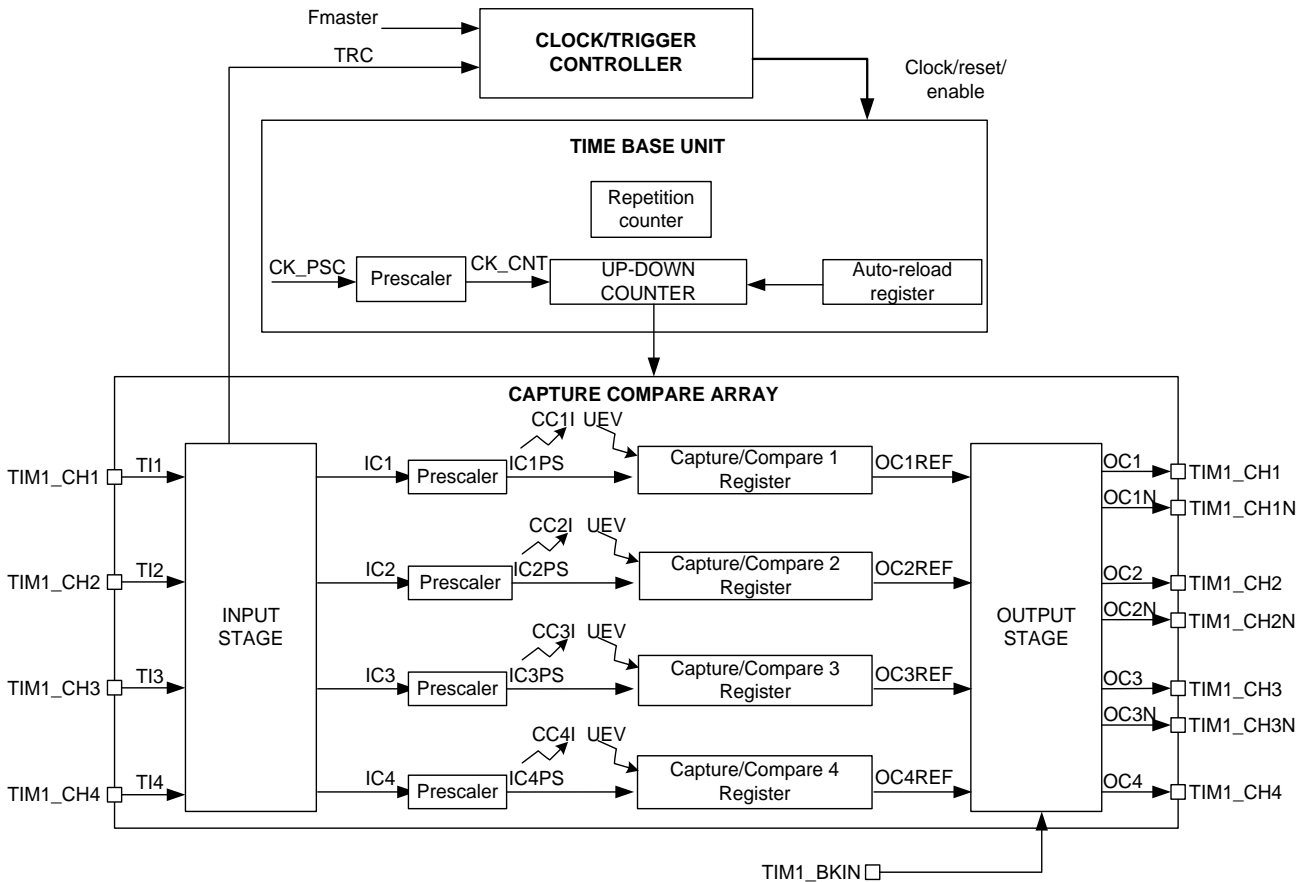


Figure 7-2 Block Diagram of TIM1

TIM1 Features:

- 16 bit up, down, up/down counting, supporting auto-reload
- Repeat Count
- 16 bit programmable prescaler
- Counting control mode:
 - ✓ Internal clock mode, encoder mode 1/2/3, reset mode, gating mode, trigger mode, external clock mode 1/2
- 4-way polarity optional channel support:
 - ✓ Input capture
 - ✓ Output compare
 - ✓ PWM channels with the same cycle and independent duty cycle (edge or center alignment), 3 channels supporting complementary output and programmable deadband
 - ✓ One-pulse output
 - ✓ 6-step PWM, synchronous mode, group mode

- ✓ Fault-break function (optional auto-restart)
- TIM1/TIM2 synchronous trigger mode
- Interruption event: update event, input trigger, commutation event, input capture, output comparison, fault-break input
- Support 3 level of register write protection lock setting (T1LOCK)

7.2.1. Summary of Timer1 Related Registers

Name	Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset
PCKEN	0x9A	—	—	UARTEN	—	TIM4EN	TIM2EN	TIM1EN	ADCEN	0000 0000
CKOCON	0x95	SYSON	CCORDY	DTYSEL[1:0]		CCOSEL[2:0]			CCOEN	0010 0000
TIM1CR1	0x211	T1ARPE	T1CMS[1:0]		T1DIR	T1OPM	T1URS	T1UDIS	T1CEN	0000 0000
TIM1CR2	0x212	T1ENCTRL	—	—	—	—	T1COMS	—	T1CCPC	0--- -0-0
TIM1SMCR	0x213	—	T1TS[2:0]			—	T1SMS[2:0]			-000 -000
TIM1ETR	0x214	T1ETP	T1ECE	T1ETPS[1:0]		T1EFT[3:0]				0000 0000
TIM1IER	0x215	T1BIE	T1TIE	T1COMIE	T1CC4IE	T1CC3IE	T1CC2IE	T1CC1IE	T1UIE	0000 0000
TIM1SR1	0x216	T1BIF	T1TIF	T1COMIF	T1CC4IF	T1CC3IF	T1CC2IF	T1CC1IF	T1UIF	0000 0000
TIM1SR2	0x217	—	—	—	T1CC4OF	T1CC3OF	T1CC2OF	T1CC1OF	—	---0 000-
TIM1EGR	0x218	T1BG	T1TG	T1COMG	T1CC4G	T1CC3G	T1CC2G	T1CC1G	T1UG	0000 0000
TIM1CCMR1 (output mode)	0x219	T1OC1CE	T1OC1M[2:0]			T1OC1PE	T1OC1FE	T1CC1S[1:0]		0000 0000
TIM1CCMR1 (input mode)		T1IC1F[3:0]				T1IC1PSC[1:0]		T1CC1S[1:0]		0000 0000
TIM1CCMR2 (output mode)	0x21A	T1OC2CE	T1OC2M[2:0]			T1OC2PE	T1OC2FE	T1CC2S[1:0]		0000 0000
TIM1CCMR2 (input mode)		T1IC2F[3:0]				T1IC2PSC[1:0]		T1CC2S[1:0]		0000 0000
TIM1CCMR3 (output mode)	0x21B	OC3CE	T1OC3M[2:0]			OC3PE	OC3FE	T1CC3S[1:0]		0000 0000
TIM1CCMR3 (input mode)		T1IC3F[3:0]				T1IC3PSC[1:0]		T1CC3S[1:0]		0000 0000
TIM1CCMR4 (output mode)	0x21C	OC4CE	T1OC4M[2:0]			OC4PE	OC4FE	T1CC4S[1:0]		0000 0000
TIM1CCMR4 (input mode)		T1IC4F[3:0]				T1IC4PSC[1:0]		T1CC4S[1:0]		0000 0000
TIM1CCER1	0x21D	T1CC2NP	T1CC2NE	T1CC2P	T1CC2E	T1CC1NP	T1CC1NE	T1CC1P	T1CC1E	0000 0000
TIM1CCER2	0x21E	T1GP	T1SMOD	T1CC4P	T1CC4E	T1CC3NP	T1CC3NE	T1CC3P	T1CC3E	0000 0000
TIM1CNTRH	0x28C	T1CNT[15:8]								0000 0000
TIM1CNTRL	0x28D	T1CNT[7:0]								0000 0000
TIM1PSCRH	0x28E	T1PSC[15:8]								0000 0000
TIM1PSCRL	0x28F	T1PSC[7:0]								0000 0000
TIM1ARRH	0x290	T1ARR[15:8]								1111 1111
TIM1ARRL	0x291	T1ARR[7:0]								1111 1111
TIM1RCR	0x292	T1REP[7:0]								0000 0000
TIM1CCR1H	0x293	T1CCR1[15:8]								0000 0000
TIM1CCR1L	0x294	T1CCR1[7:0]								0000 0000
TIM1CCR2H	0x295	T1CCR2[15:8]								0000 0000
TIM1CCR2L	0x296	T1CCR2[7:0]								0000 0000
TIM1CCR3H	0x297	T1CCR3[15:8]								0000 0000

Name	Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset
TIM1CCR3L	0x298	T1CCR3[7:0]								0000 0000
TIM1CCR4H	0x299	T1CCR4[15:8]								0000 0000
TIM1CCR4L	0x29A	T1CCR4[7:0]								0000 0000
TIM1BKR	0x29B	T1MOE	T1AOE	T1BKP	T1BKE	T1OSSR	T1OSSI	T1LOCK[1:0]		0000 0000
TIM1DTR	0x29C	T1DTG[7:0]								0000 0000
TIM1OISR	0x29D	—	T1OIS4	T1OIS3N	T1OIS3	T1OIS2N	T1OIS2	T1OIS1N	T1OIS1	-000 0000
LEBCON	0x41C	LEBEN	LEBCH[1:0]		—	EDGS	BKS[2:0]		000- 0000	

Table 7-5 Summary of Timer1 Related Registers (reserved bit must keep as reset, and cannot be changed)

Name	Status	Register	Addr.	Reset	
T1CNT	TIM1 Count value	MSB	TIM1CNTRH[7:0]	0x28C	RW-0000 0000
		LSB	TIM1CNTRL[7:0]	0x28D	RW-0000 0000
T1PSC	TIM1Prescaler	MSB	TIM1PSCRH[7:0]	0x28E	RW-0000 0000
		LSB	TIM1PSCRL[7:0]	0x28F	RW-0000 0000
T1ARR	Auto-reload register for counting cycle (preload value) Note: When this value is 0, the counter does not work;	MSB	TIM1ARRH[7:0]	0x290	RW-1111 1111
		LSB	TIM1ARRL[7:0]	0x291	RW-1111 1111
T1REP	Repeat Count Down	TIM1RCR[7:0]	0x292	RW-0000 0000	
T1CCR1	Input capture mode: Last capture event (IC1) Captured count value	MSB	TIM1CCR1H[7:0]	0x293	RO-0000 0000
		LSB	TIM1CCR1L[7:0]	0x294	RO-0000 0000
	Output compare mode: Output compare value of TIM1_CH1 (Preload value)	MSB	TIM1CCR1H[7:0]	0x293	RW-0000 0000
		LSB	TIM1CCR1L[7:0]	0x294	RW-0000 0000
T1CCR2	Input capture mode: Last capture event (IC2) Captured count value	MSB	TIM1CCR2H[7:0]	0x295	RO-0000 0000
		LSB	TIM1CCR2L[7:0]	0x296	RO-0000 0000
	Output compare mode: Output compare value of TIM1_CH2	MSB	TIM1CCR2H[7:0]	0x295	RW-0000 0000

Name	Status		Register	Addr.	Reset
	(Preload value)	LSB	TIM1CCR2L[7:0]	0x296	RW-0000 0000
T1CCR3	Input capture mode: Last capture event (IC3) Captured count value	MSB	TIM1CCR3H[7:0]	0x297	RO-0000 0000
		LSB	TIM1CCR3L[7:0]	0x298	RO-0000 0000
	Output compare mode: Output compare value of TIM1_CH3 (Preload value)	MSB	TIM1CCR3H[7:0]	0x297	RW-0000 0000
		LSB	TIM1CCR3L[7:0]	0x298	RW-0000 0000
T1CCR4	Input capture mode: Last capture event (IC4) Captured count value	MSB	TIM1CCR4H[7:0]	0x299	RO-0000 0000
		LSB	TIM1CCR4L[7:0]	0x29A	RO-0000 0000
	Output compare mode: Output compare value of TIM1_CH4 (Preload value)	MSB	TIM1CCR4H[7:0]	0x299	RW-0000 0000
		LSB	TIM1CCR4L[7:0]	0x29A	RW-0000 0000

Table 7-6 Timer1 Period Related Register

Name	Status		Register	Addr.	Reset
TIM1EN	<u>TIM1 Clock module</u>	1 = Enable 0 = <u>Disable</u>	PCKEN[1]	0x9A	RW-0
SYSON	<u>In SLEEP mode, the Sysclk controls</u>	1 = Enable 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
T1CKSRC	<u>TIM1 Clock Sources (Fmaster)</u> 000 = <u>Sysclk</u> 100 = 2 x (XT or EC) (*) 001 = HIRC 101 = LIRC 010 = XT or EC (*) 110 = LP or EC (*) 011 = 2 x HIRC 111 = 2 x (LP or EC) (*) (*)FOSC should be configured accordingly or in LP/XT/EC mode, otherwise oscillator will not run.		TCKSRC[2:0]	0x31F	RW-000
DTYSEL	<u>TIM1/TIM2 Multiplier Clock Duty Cycle Adjustment</u> <u>Bit</u> 00 = 2ns delay 10 = 4ns delay 01 = 3ns delay 11 = 7ns delay		CKOCON[5:4]	0x95	RW-10

Name	Status	Register	Addr.	Reset
T1ARPE	<u>Automatic pre-loading of counting cycles</u> 1 = Enable (T1ARR preload value is loaded when the update event arrives) 0 = <u>Disable</u> (T1ARR loaded immediately)	TIM1CR1[7]	0x211	RW-0
T1CMS	<u>Counter alignment modes</u> 00 = <u>Edge-aligned mode</u> (Counting direction is determined by T1DIR) 01 = Center-aligned mode1 (T1CCxIF set to 1 when counting down) 10 = Center-aligned mode2 (T1CCxIF set to 1 when counting up) 11 = Center-aligned mode3 (T1CCxIF is set to 1 for both upward and downward counting) Notes. 1. Center-aligned mode means that the counter counts up and down alternately. 2. Mode switching is allowed only when the counter is disabled (T1CEN=0).	TIM1CR1[6:5]		RW-00
T1DIR	<u>Count direction (in center-aligned/encoder mode, this bit is read-only)</u> 1 = Up 0 = <u>Down</u>	TIM1CR1[4]		RW-0
T1OPM	<u>One-pulse mode</u> 1 = Enable (When the next update event comes, T1CEN will be reset automatically and the counter will stop) 0 = <u>Disable</u> (The counter does not stop when an update event occurs)	TIM1CR1[3]		RW-0
T1URS	<u>Update event source when T1UDIS=0</u> 1 =Counter overflow/underflow 0 =Counter overflow/underflow, <u>Software setting T1UG bit, or Reset Trigger Event</u>	TIM1CR1[2]		RW-0
T1UDIS	<u>Generate update event control</u> 1 = Disable 0 = Enable	TIM1CR1[1]		RW-0
T1CEN	<u>TIM1 Counter</u>	TIM1CR1[0]		RW-0

Name	Status	Register	Addr.	Reset
	1 = Enable 0 = <u>Disable</u>			
T1ENCTRL	<u>TIM1/TIM2 trigger control synchronously</u> 1 = TIM1/TIM2 is enabled by T1CEN simultaneously 0 = <u>TIM2 is enabled by T2CEN</u>	TIM1CR2[7]	0x212	RW-0
T1COMS	<u>When T1CCPC=1, commutation event source</u> 1 = T1COMG is set to 1 by software, or trigger event is generated 0 = <u>T1COMG is set to 1 by software</u> Note: Only valid for channels with complementary outputs;	TIM1CR2[2]		RW-0
T1CCPC	<u>Automatic preload of capture/compare control bits (control bits:T1SMOD, T1GP, T1CCxE, T1CCxNE, T1CCxP, T1CCxNP, T1OCxM)</u> 1 = Enable (The preload value of the control bit is loaded when the commutation event comes) 0 = <u>Disable</u> (controls loaded immediately) Note: Only valid for channels with complementary outputs;	TIM1CR2[0]		RW-0
T1TS	<u>Trigger input source of synchronization counter (TRGI)</u> 0xx = Reserved 100 = Edge detector of channel 1 input T11 (T11F_ED) 101 =Channel 1 input after filtering(T11FP1) 110 =Channel 2 input after filtering(T12FP2) 111 = External trigger input (ETRF) Note: 1. The trigger input source can only be changed when T1SMS=000; 2. See T1CC1P/T1CC2P or T1ETP for polarity of effective edge/active level of trigger input;	TIM1SMCR[6:4]	0x213	RW-000
T1SMS	<u>Trigger mode</u> 000 = <u>Internal clock</u> 001 = Encoder mode 1	TIM1SMCR[2:0]		RW-000

Name	Status	Register	Addr.	Reset
	<p>(According to TI1FP1 level, the counter counts up/down on the effective edge of TI2FP2)</p> <p>010 = Encoder mode 2 (According to TI2FP2 level, the counter counts up/down on the effective edge of TI1FP1)</p> <p>011 = Encoder mode 3 (According to TI1FP1/TI2FP2 level, the counter counts up/down on the effective edge of TI2FP2/TI1FP1)</p> <p>100 = Reset mode (When the active edge of the input is triggered, the counter is cleared and counted again from 0)</p> <p>101 = Gating mode (Counter counts during triggering input effective level, and stops counting when inactive level is reached, but does not reset)</p> <p>110 = Trigger mode (Counter counts and does not reset when triggering the effective edge of input)</p> <p>111 = External clock mode 1 (Counter counts on the active edge of the trigger input)</p> <p>Note: The trigger input of Gating mode cannot select TI1F_ ED;</p>			
T1ETP	<p><u>External trigger polarity</u></p> <p>1 = ETR inverted, active at low or falling edge</p> <p>0 = <u>ETR is not inverted, active at high or rising edge</u></p>	TIM1ETR[7]		RW-0
T1ECE	<p><u>External clock mode 2</u></p> <p>1 = Enable (Counter counts on the active edge of the external trigger input ETR)</p> <p>0 = <u>Disable</u></p> <p>Note:</p> <ol style="list-style-type: none"> The same function as external clock mode 2 when external trigger input ETR is selected for external clock mode 1. 	TIM1ETR[6]	0x214	RW-0

Name	Status	Register	Addr.	Reset
	T1CCR1, and the original configuration T1CCR2 / T1CCR3 is disabled.) 0 = <u>Disable</u>			
T1SMOD	<u>PWM synchronous mode</u> 1 = Enable (The signals of channel CH1N/2N/3N and CH1/2/3 are identical, and there is no deadband) 0 = <u>Disable</u>	TIM1CCER2[6]		RW-0

Table 7-7 Instruction Level Timer1 Related Control Registers

Name	Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	Bit0	Reset
TIM1CCMR1	0x219	T1IC1F[3:0]			T1IC1PSC[1:0]		T1CC1S[1:0]			RW-0000 0000
TIM1CCMR2	0x21A	T1IC2F[3:0]			T1IC2PSC[1:0]		T1CC2S[1:0]			RW-0000 0000
TIM1CCMR3	0x21B	T1IC3F[3:0]			T1IC3PSC[1:0]		T1CC3S[1:0]			RW-0000 0000
TIM1CCMR4	0x21C	T1IC4F[3:0]			T1IC4PSC[1:0]		T1CC4S[1:0]			RW-0000 0000

Name	Status			Register	Addr.	Reset
T1ICxF	<u>Sampling frequency and digital filter length of channel x input capture</u>			TIM1CCMRx[7:4] x = 1, 2, 3, 4	0x219/ 0x21A/ 0x21B/ 0x21C	RW-00 00
	Value	Sampling frequency(f_{SAMPLI}/N)	Digital filter length N			
	0000	<u>Fmaster</u>	<u>0</u>			
	0001	Fmaster	2			
	0010	Fmaster	4			
	0011	Fmaster	8			
	0100	Fmaster / 2	6			
	0101	Fmaster / 2	8			
	0110	Fmaster / 4	6			
	0111	Fmaster / 4	8			
	1000	Fmaster / 8	6			
	1001	Fmaster / 8	8			
	1010	Fmaster / 16	5			
1011	Fmaster / 16	6				

	1100	Fmaster / 16	8			
	1101	Fmaster / 32	5			
	1110	Fmaster / 32	6			
	1111	Fmaster / 32	8			
T1CCxPSC	<u>Channel x input capture prescaler (several events trigger a capture)</u> 00 = 1 prescaler 10 = 4 prescaler 01 = 2 prescaler 11 = 8 prescaler Note: When T1CCxE=0, the prescaler is reset to 00			TIM1CCMRx[3:2]		RW-00
T1CC1S ¹	<u>Channel 1 Mode selection</u>	00 = <u>Output</u> 01 = Input, input pin is mapped to T11FP1 10 = Input, input pin is mapped to T12FP1 11 = Input, input pin is mapped to TRC		TIM1CCMR1[1:0]	0x219	RW-00
T1CC2S ²	<u>Channel 2 Mode selection</u>	00 = <u>Output</u> 01 = Input, input pin is mapped to T12FP2 10 = Input, input pin is mapped to T11FP2 11 = Input, input pin is mapped to TRC		TIM1CCMR2[1:0]	0x21A	RW-00
T1CC3S ²	<u>Channel 3 Mode selection</u>	00 = <u>Output</u> 01 = Input, input pin is mapped to T13FP3 10 = Input, input pin is mapped to T14FP3 11 = Reserved		TIM1CCMR3[1:0]	0x21B	RW-00
T1CC4S ²	<u>Channel 4 Mode selection</u>	00 = <u>Output</u> 01 = Input, input pin is mapped to T13FP4 10 = Input, input pin is mapped to T14FP4 11 = Reserved		TIM1CCMR4[1:0]	0x21C	RW-00

Table 7-8 TIM1CCMRx as Input Configuration Register

¹ Can be written only when channel x disables (T1CCxE=0 and T1CCxNE=0).

² Can be written only when channel x disables (T1CCxE=0 and T1CCxNE=0).

Name	Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	Bit0	Reset
TIM1CCMR1	0x219	T1OC1CE	T1OC1M[2:0]		T1OC1PE	T1OC1FE	T1CC1S[1:0]			RW-0000 0000
TIM1CCMR2	0x21A	T1OC2CE	T1OC2M[2:0]		T1OC2PE	T1OC2FE	T1CC2S[1:0]			RW-0000 0000
TIM1CCMR3	0x21B	T1OC3CE	T1OC3M[2:0]		T1OC3PE	T1OC3FE	T1CC3S[1:0]			RW-0000 0000
TIM1CCMR4	0x21C	T1OC4CE	T1OC4M[2:0]		T1OC4PE	T1OC4FE	T1CC4S[1:0]			RW-0000 0000

T1OCxM	Channel x Output compare mode		Level of reference signal OCxREF
000	Frozen (no compare)		<u>Remain unchanged</u>
001	When T1CNT = CCRx_SHAD		1
010	When T1CNT = CCRx_SHAD		0
011	When T1CNT = CCRx_SHAD		Level reversal
100	Forced inactive		0
101	Forced active		1
110	PWM1 mode	T1CNT < CCRx_SHAD	1
		T1CNT > CCRx_SHAD	0
111	PWM2 mode	T1CNT < CCRx_SHAD	0
		T1CNT > CCRx_SHAD	1

Note: The output reference signal OCxREF is active at high level, which together with the polarity selection T1CCxP determines the actual output value of pin OCx;

Table 7-9 T1OCxM Configured as Output Compare Mode

Name	Status	Register	Addr.	Reset
T1OCxCE	<u>Channel x output reference signal OCxREF is controlled by ETR reset</u> 1 = Enable (When ETR is at effective level, OCxREF resume) 0 = Disable (OCxREF is not affected by ETR input)	TIM1CCMRx[7] x = 1, 2, 3, 4	0x219 / 0x21A	RW-0
T1OCxPE	<u>Automatic preloading of channel x output compare values</u> 1 = Enable (T1CCRx preload values are loaded when the update event arrives) 0 = <u>Disable</u> (T1CCRx loaded immediately) Note: It must be enabled under PWM mode, and single	TIM1CCMRx[3] x = 1, 2, 3, 4	0x21B / 0x21C	RW-0

Name	Status	Register	Addr.	Reset
	pulse mode is optional			
T1OCxFE	<p><u>Channel x output signal enables quickly</u></p> <p>1 = <u>Enable</u> (Delay from input triggering effective edge to channel x output $\geq 3 \cdot T_{Fmaster}$, and the output of channel x is a fixed value, the value=T1CEN (PWM1 mode) / !T1CEN(PWM2 mode))</p> <p>0 = <u>Disable</u> (Delay from input triggering effective edge to channel x output $\geq 5 \cdot T_{Fmaster}$)</p> <p>Note: This bit only works when Channel 1 is configured as PWM1/PWM2 mode</p>	TIM1CCMRx[2] x = 1, 2, 3, 4		RW-0
T1CC1S ³	<p><u>Channel 1</u> <u>Mode selection</u></p> <p>00 = <u>Output</u></p> <p>01 = Input, input pin is mapped to TI1FP1</p> <p>10 = Input, input pin is mapped to TI2FP1</p> <p>11 = Input, input pin is mapped to TRC</p>	TIM1CCMR1[1:0]	0x219	RW-00
T1CC2S ³	<p><u>Channel 2</u> <u>Mode selection</u></p> <p>00 = <u>Output</u></p> <p>01 = Input, input pin is mapped to TI2FP2</p> <p>10 = Input, input pin is mapped to TI1FP2</p> <p>11 = Input, input pin is mapped to TRC</p>	TIM1CCMR2[1:0]	0x21A	RW-00
T1CC3S ³	<p><u>Channel 3</u> <u>Mode selection</u></p> <p>00 = <u>Output</u></p> <p>01 = Input, input pin is mapped to TI3FP3</p> <p>10 = Input, input pin is mapped to TI4FP3</p> <p>11 = Reserved</p>	TIM1CCMR3[1:0]	0x21B	RW-00
T1CC4S ³	<p><u>Channel 4</u> <u>Mode selection</u></p> <p>00 = <u>Output</u></p> <p>01 = Input, input pin is mapped to TI3FP4</p> <p>10 = Input, input pin is mapped to TI4FP4</p> <p>11 = Reserved</p>	TIM1CCMR4[1:0]	0x21C	RW-00

Table 7-10 TIM1CCMRx as Output Configuration Register

³ Can be written only when channel x is disabled (T1CCxE=0 and T1CCxNE=0)

Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Addr	Reset
TIM1CCER1	T1CC2NP	T1CC2NE	T1CC2P	T1CC2E	T1CC1NP	T1CC1NE	T1CC1P	T1CC1E	0x21D	RW-0000 0000
TIM1CCER2	T1GP	T1SMOD	T1CC4P	T1CC4E	T1CC3NP	T1CC3NE	T1CC3P	T1CC3E	0x21E	RW-0000 0000

Name	Functions	Input Capture/Trigger mode (T1CCxS ≠ 00)	Output compare mode (T1CCxS = 00)
T1CCxP	Channel x Input/output polarity selection	1 = Capture/trigger occurs at the falling edge or low level of T1xF 0 = <u>Capture/trigger occurs at the rising edge or high level of T1xF</u> Note: Only channel 1 and 2 can be selected as input trigger source	1 = OCx active at low level 0 = <u>OCx active at high level</u>
T1CCxE	Channel x I/O pin function	1 = Enable input capture/trigger function of the pin 0 = <u>Disable</u>	1 = Enable the OCx output function of the pin 0 = <u>Disable</u>
T1CCxNP	Channel x complementary output polarity selection	-	1 = OCxN active at low level 0 = <u>OCxN active at high level</u>
T1CCxNE	Channel x complementary pinout function	-	1 = Enable the OCxN output function of the pin 0 = <u>Disable</u>

Note: The channel output level is jointly determined by the values of T1MOE, T1OSSI, T1OSSR, T1OISx, T1OISxN, T1CCxE and T1CCxNE bits. See [Table 7-14](#).

Table 7-11 Timer1 Channel Output and Polarity Selection

Name	Status	Register	Addr.	Reset
TIM1_CH1N	<u>Channel 1 Complementary Pin Remapping</u> 1 = PB2 0 = <u>PC0</u>	AFP0[2]	0x19E	RW-0
	<u>Channel 2 Pin Remapping</u> 1 = PB0 0 = <u>PA1</u>	AFP0[5]		RW-0
TIM1_CH4	<u>Channel 4 Pin Remapping</u> 0x = <u>PB1</u> 10 = PA7 11 = PA2	AFP1[1:0]	0x19F	RW-00

Table 7-12 Timer1 Pin Function Remapping Register

Name	Status	Register	Addr.	Reset
BKS	<u>Fault-Break Source for TIM1</u> 000 = <u>Disable</u> 001 = BKIN pin 010 = LVD detection 100 = ADC threshold comparison	LEBCON[2:0]	0x41C	RW-0 00
T1MOE ⁴	<u>Main output control</u> (Valid only for channels configured as outputs) 1 = Enable (If T1CCxE/T1CCxNE = 1, enable OCx and OCxN outputs) 0 = <u>Disable</u> (Disable OCx and OCxN output or force to idle state)	TIM1BKR[7]	0x29B	RW-0
T1AOE	<u>Main output auto-control</u> 1 = T1MOE is automatically set to 1 when the next update event arrives (when the break input is inactive) or set to 1 by software 0 = <u>T1MOE can only be set to 1 by software</u>	TIM1BKR[6]		RW-0
T1BKP	<u>Fault source break input TIM1 BKIN polarity</u> 1 = active at high level 0 = <u>active at low level</u>	TIM1BKR[5]		RW-0
T1BKE	<u>Break input (BRK)</u> 1 = Enable 0 = <u>Disable</u>	TIM1BKR[4]		RW-0
T1OSSR	<u>Output "off state" selection in operating mode (when T1MOE = 1)</u> For details, see Table 7-14 Timer1 Output Control and Status	TIM1BKR[3]		RW-0
T1OSSI	<u>Output "off state" selection in idle mode (when T1MOE=0)</u> For details, see Table 7-14 Timer1 Output Control and Status	TIM1BKR[2]		RW-0
T1LOCK ⁵	<u>Lock settings</u> (Write protect, prevent software errors)			
	00	01	10	11
	<u>Disable</u>	Locking level 1	Locking level 2	Locking level 3
	No write protection for registers	T1BKE, T1BKP, T1AOE, T1OISx, T1OISxN, T1DTG	Includes level 1, T1CCxP, T1CCxNP, T1OSSR, T1OSSI	Includes level 2, T1OCxM, T1OCxPE
		TIM1BKR[1:0]		RW-0 0

Table 7-13 Timer1 Main Output Enable, Braking and Locking Level Registers

⁴ When the break input is valid, this bit will be cleared by hardware asynchronously.

⁵ The LOCK bit can only be written once after system reset, and once it is written, its content will be remain unchanged until reset.

Controls					Output Status	
T1MOE	T1OSSI	T1OSSR	T1CCxE	T1CCxNE	OCx Output Status	OCxN Output Status
1	x	0	0	0	OCx = 0 (Output disabled)	OCxN = 0 (Output disabled)
		0	0	1	OCx = 0 (Output disabled)	OCxN = OCxREF ^ T1CCxNP
		0	1	0	OCx = OCxREF ^ T1CCxP	OCxN = 0 (Output disabled)
		0	1	1	OCx = OCxREF ^ T1CCxP + Deadband	OCxN = Complementary signals for OCxREF ^ T1CCxNP + Deadband
		1	0	0	OCx = T1CCxP (Output disabled)	OCxN = T1CCxNP (Output disabled)
		1	0	1	OCx = T1CCxP	OCxN = OCxREF ^ T1CCxNP
		1	1	0	OCx = OCxREF ^ T1CCxP	OCxN = T1CCxNP
		1	1	1	OCx = OCxREF ^ T1CCxP + Deadband	OCxN = Complementary signals for OCxREF ^ T1CCxNP + Deadband
0	x	0	0	0	OCx = T1CCxP (Output disabled)	OCxN = T1CCxNP (Output disabled)
		0	0	1	In deadband: OCx = T1CCxP, OCxN = T1CCxNP (Output disabled)	
		0	1	0	After deadband: OCx = T1OISx, OCxN = T1OISxN (Output disabled)	
		0	1	1	After deadband: OCx = T1OISx, OCxN = T1OISxN (Output disabled)	
		1	0	0	OCx = T1CCxP (Output disabled)	OCxN = T1CCxNP (Output disabled)
		1	0	1	In deadband: OCx = T1CCxP, OCxN = T1CCxNP (Output inactive values)	
		1	1	0	After deadband: OCx = T1OISx, OCxN = T1OISxN	
		1	1	1	After deadband: OCx = T1OISx, OCxN = T1OISxN	

Table 7-14 Timer1 Output Control and Status

Name	Status			Register	Addr.	Reset
T1DTG	<u>Setting of Deadband generator</u>			TIM1DTR[7:0]	0x29C	RW-0000 0000
	T1DTG[7:0]	DT(Deadband Duration Time)	t_{DTG}			
	0xxxxxxx	$T1DTG[7:0] \times t_{DTG}$	$T_{Fmaster}$ (f1)			
	10xxxxxx	$(64+T1DTG[5:0]) \times t_{DTG}$	$2 \times T_{Fmaster}$ (f2)			
	110xxxxx	$(32+T1DTG[4:0]) \times t_{DTG}$	$8 \times T_{Fmaster}$ (f3)			
	111xxxxx	$(32+T1DTG[4:0]) \times t_{DTG}$	$16 \times T_{Fmaster}$ (f4)			
	* Fmaster is the clock source of TIM1 eg. When $T_{Fmaster} = 125 \text{ ns}$ (8 MHz), Dead-Time is as follows:					
	T1DTG[7:0]	Dead-Time (μs)	Step Time			
0 ~ 7Fh	0 ~ 15.875	125 ns (f1)				
80h ~ BFh	16 ~ 31.75	250 ns (f2)				
C0h ~ DFh	32 ~ 63	1 μs (f3)				
E0h ~ FFh	64 ~ 126	2 μs (f4)				

Table 7-15 Timer1 Complementary Output Deadband Configuration

Name	Status	Register	Addr.	Reset
T1OIS4	<u>When T1MOE=0, Channel 4(OC4) output in idle state</u> 1 = OC4 output 1 0 = OC4 output 0	TIM1OISR[6]	0x29D	RW-0
T1OIS3	<u>When T1MOE=0, Channel 3/2/1(OCx) output in idle state</u>	TIM1OISR[4]		RW-0
T1OIS2	1 = After Dead-Time, OCx output 1	TIM1OISR[2]		RW-0
T1OIS1	0 = <u>After Dead-Time, OCx output 0</u>	TIM1OISR[0]		RW-0
T1OIS3N	<u>When T1MOE=0, complementary Channel 3/2/1(OCxN) output in idle state</u>	TIM1OISR[5]		RW-0
T1OIS2N	1 = After Dead-Time, OCxN output 1	TIM1OISR[3]		RW-0
T1OIS1N	0 = <u>After Dead-Time, OCxN output 0</u>	TIM1OISR[1]		RW-0

Table 7-16 Timer1 Channel Output Register in Idle Status

Name	Status	Register	Addr.	Reset
GIE	<u>Global Interrupt</u> 1 = Enable (PEIE, T1BIE, T1BG, T1TIE, T1TG, T1COMIE, T1COMG, T1CCxIE, T1CCxG, T1UIE apply) 0 = <u>Global Shutdown</u> (Wake-Up not affected)	INTCON[7]	Bank First address+0x0B	RW-0
PEIE	<u>Peripheral Interrupt Enable</u> 1 = Enable (T1BIE, T1BG, T1TIE, T1TG, T1COMIE, T1COMG, T1CCxIE, T1CCxG, T1UIE apply) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0
T1BIE	<u>Break Interrupt</u> 1 = Enable 0 = <u>Disable</u>	TIM1IER[7]	0x215	RW-0
T1BG ⁶	<u>Break Software Interrupt</u> 0 = <u>Disable</u>	TIM1EGR[7]	0x218	WO-0
T1BIF ⁷	<u>Break Interrupt Flag</u> 1 = Effective level detected on break input 0 = <u>No break event</u>	TIM1SR1[7]	0x216	R_W1C-0
T1TIE	<u>Trigger Interrupt</u> 1 = Enable 0 = <u>Disable</u>	TIM1IER[6]	0x215	RW-0
T1TG ⁶	<u>Trigger Software Interrupt</u> 0 = <u>Disable</u>	TIM1EGR[6]	0x218	WO-0
T1TIF ⁷	<u>Trigger Interrupt Flag</u> 1 = Triggered 0 = <u>No Trigger event</u>	TIM1SR1[6]	0x216	R_W1C-0
T1COMIE	<u>Commutation Interrupt</u> 1 = Enable 0 = <u>Disable</u>	TIM1IER[5]	0x215	RW-0
T1COMG ⁶	<u>Commutation Software Interrupt</u> 0 = <u>Disable</u>	TIM1EGR[5]	0x218	WO-0
T1COMIF ⁷	<u>Commutation Interrupt Flag</u> 1 = Commutated 0 = <u>No Commutation event</u>	TIM1SR1[5]	0x216	R_W1C-0
T1CC4IE	Channel 4 Capture/Compare Interrupt	TIM1IER[4]		RW-0
T1CC3IE	Channel 3 Capture/Compare Interrupt	TIM1IER[3]	0x215	RW-0
T1CC2IE	Channel 2 Capture/Compare Interrupt	TIM1IER[2]		RW-0

⁶ The software is set to 1, and the hardware is automatically cleared to 0.

⁷ Write '1' to clear, and writing '0' has no effect on the bit value.. It is recommended that only STR and MOVWI instructions be used for write operations, not BSR or IOR instructions.

Name	Status	Register	Addr.	Reset
T1CC1IE	Channel 1 Capture/Compare Interrupt	TIM1IER[1]	0x218	RW-0
T1CC4G ⁶	Channel 4 Capture/Compare Software Interrupt	TIM1EGR[4]		WO-0
T1CC3G ⁶	Channel 3 Capture/Compare Software Interrupt	TIM1EGR[3]		WO-0
T1CC2G ⁶	Channel 2 Capture/Compare Software Interrupt	TIM1EGR[2]		WO-0
T1CC1G ⁶	Channel 1 Capture/Compare Software Interrupt	TIM1EGR[1]		WO-0
T1CC4IF ⁷	<u>Channel x Capture/Compare Interrupt Flag</u> <ul style="list-style-type: none"> Output mode: 1 = T1CNT matches T1CCRx value 0 = <u>Mismatches</u> Note: If T1CCRx>T1ARR, T1CCxIF is set to 1 when CNT counts to T1ARR value. <ul style="list-style-type: none"> Input mode: 1 = Count value captured to T1CCRx (auto clear when reading T1CCRx) 0 = <u>No Capture event</u> 	TIM1SR1[4]	0x216	R_W1C-0
T1CC3IF ⁷		TIM1SR1[3]		R_W1C-0
T1CC2IF ⁷		TIM1SR1[2]		R_W1C-0
T1CC1IF ⁷		TIM1SR1[1]		R_W1C-0
T1CC4OF ⁷	<u>Channel x Repeat Capture Interrupt Flag</u> 1 = Repeated capture occurs (when the count value is captured to the T1CCRx register, T1CCxIF has been set to 1) 0 = <u>No repeated capture</u>	TIM1SR2[4]	0x217	R_W1C-0
T1CC3OF ⁷		TIM1SR2[3]		R_W1C-0
T1CC2OF ⁷		TIM1SR2[2]		R_W1C-0
T1CC1OF ⁷		TIM1SR2[1]		R_W1C-0
T1UIE	Allow Update Interrupt	TIM1IER[0]	0x215	RW-0
T1UG ⁶	Allow Update Software Interrupt	TIM1EGR[0]	0x218	WO-0
T1UIF ⁷	Update event Interrupt Flag	TIM1SR1[0]	0x216	R_W1C-0

Table 7-17 Timer1 interrupt enable and status bits

7.2.2. Counting basic units

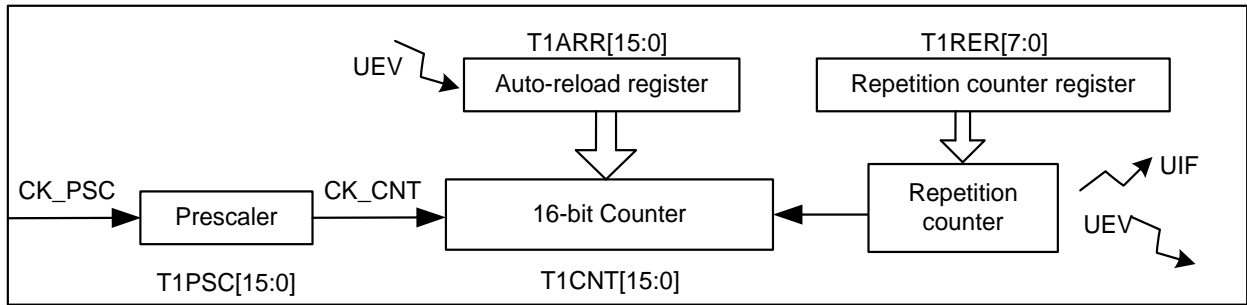


Figure 7-3 Counting basic units

TIM1 base units:

- 16-bit up, down or up/down counter
- 16-bit prescaler
- Repeated counter
- 16-bit auto-reload register

The prescaler, repetition counter, output comparison and the auto reload register consist of the preload register and the shadow register, respectively.

	Prescaler	Repetition Counter	Output Compare value	Auto reload register
Pre-loaded enables	Enabled by default when T1CEN = 1		T1OCxPE	T1ARPE
Pre-loaded Registers	T1PSC[15:0]	T1REP[7:0]	T1CCRx[15:0]	T1ARR[15:0]

Table 7-18 Update event related preload registers

The prescaled clock (CK_PSC) source is available as follows (see [Section 7.2.3](#) Clock/Trigger Controller).

- Internal clock source (Fmaster)
- External clock source (ETR)
- Filtered external channel trigger input (TI1FP1, TI2FP2)

Note: Due to the need for clock synchronization, the clock cycle of the external asynchronous clock source (ETR) must be two times longer than the cycle of the internal clock source (Fmaster).

The 16-bit prescaler divides the prescaler clock (CK_PSC) by 1 ~ 65536 to generate the counter clock (CK_CNT).

Frequency division Equation: $f_{CK_CNT} = f_{CK_PSC} / (PSCR[15:0] + 1)$; (PSCR is the value of prescaler shadow register)

When T1UDIS=0, update events are allowed to occur. The update event source (see "T1URS") are as follows:

- Counter overflow or underflow (when T1REP=0, please refer to [Section 7.2.2.2](#) Repetition Counter)
- Software setting T1UG bit
- Trigger event is generated in reset mode

When an update event is generated, the update event flag bit T1UIF is set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE and T1UIE).

In addition, depending on the configuration, update events can trigger the following conditions:

1. Related to prescaler, repetition counter, output compare value and auto reload register:
 - (1) When the counter is enabled (T1CEN = 1) and its corresponding preload is enabled (T1OCxPE / T1ARPE = 1, as in [Table 7-18](#)), its shadow register will be updated to the preload value when an update event is generated, as in [Figure 7-4](#).
 - (2) When the counter is disabled (T1CEN = 0), or its corresponding preload is disabled (T1OCxPE / T1ARPE = 0), its shadow register will be updated directly to the preload value.
2. In one-pulse mode, when an update event is generated, the counter is automatically turned off (T1CEN = 0) and the counter stops counting.
3. When the fault-break and the auto output (T1AOE = 1) are enabled, the PWM will resume normal output after an update event is generated when the fault event is withdrawn.

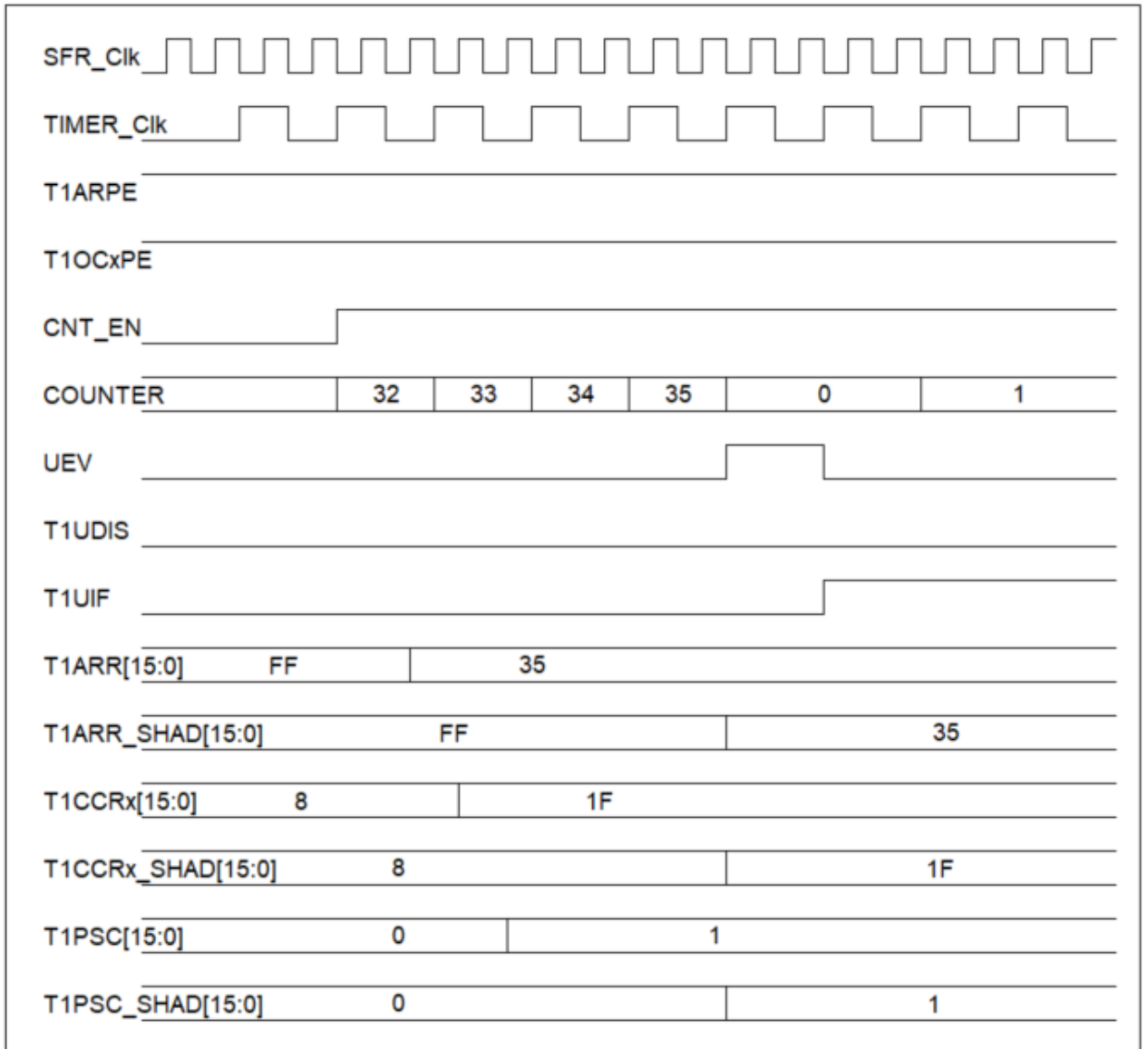


Figure 7-4 Update timing diagram of the preload register under update event

7.2.2.1. Count mode

- **Up count mode** (T1CMS = 00 and T1DIR = 0): Counter counts upward from 0. When T1CNT = T1ARR, an overflow event is generated, and then the count starts from 0 again.

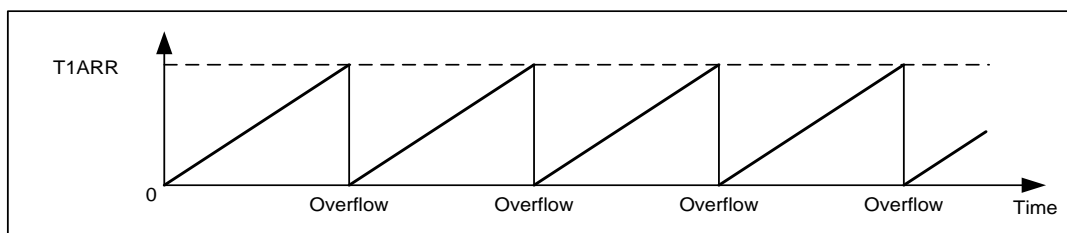


Figure 7-5 Up count mode

- **Down count mode** ($T1CMS = 00$ and $T1DIR = 1$): The counter starts counting down from the value of $T1ARR$, generates an underflow event when $T1CNT = 0$, and then starts counting again from the value of $T1ARR$.

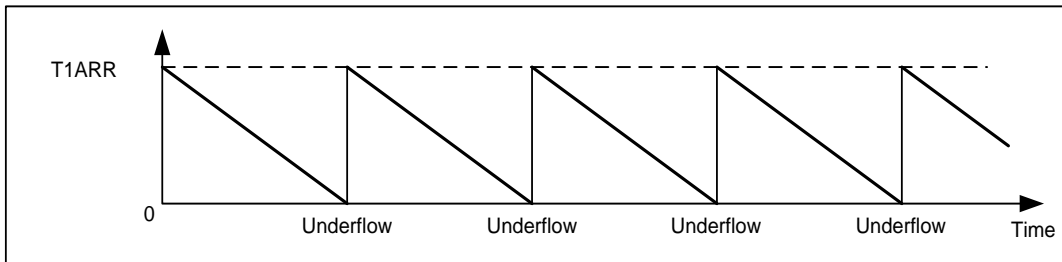


Figure 7-6 Down count mode

Center-aligned mode (Upward/downward counting, $T1CMS \neq 00$): The initial direction of counting depends on the $T1DIR$ register value (as shown in [Figure 7-7](#) and [Figure 7-8](#)), and the initial value of counting is $T1CNT$. If $T1DIR$ is initialized to 0, the counter starts counting up from $T1CNT$ and generates an overflow event when $T1CNT = T1ARR$; then the counter starts counting down from the value of $T1ARR$ and generates a downflow event when $T1CNT = 0$. And then the counter starts counting up from 0 and keeps repeating the above process.

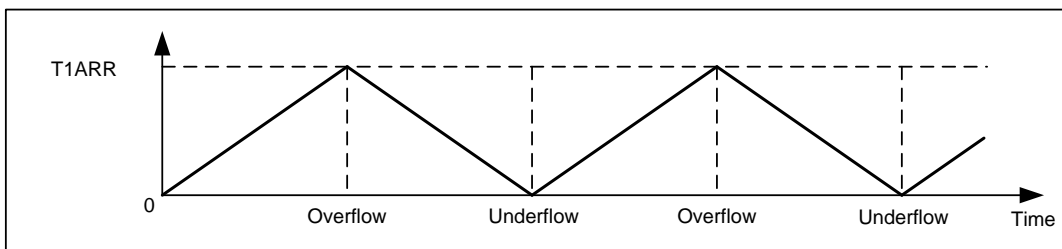


Figure 7-7 Center-aligned mode ($T1DIR$ initialized to 0)

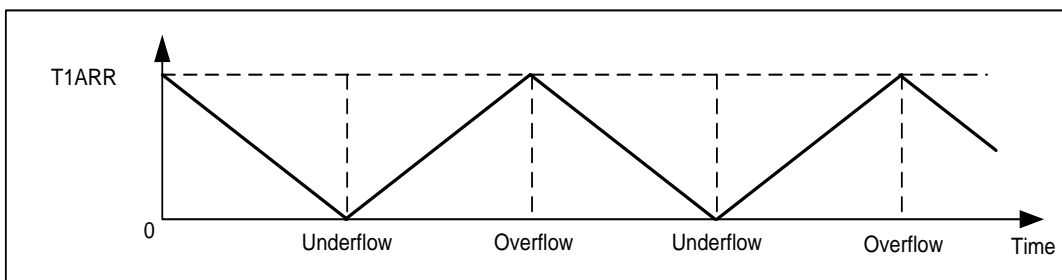


Figure 7-8 center-aligned mode ($T1DIR$ initialized to 1)

Example of configuration steps:

1. Enable the TIM1 module clock ($TIM1EN = 1$), and select the TIM1 clock source ($T1CKSRC$);
2. If necessary, enable the counting cycle preload function ($T1ARPE=1$);
3. Configure the value of counting cycle ($T1ARR$);
4. Configure the counting direction as up or down ($T1DIR$);
5. Configure the count mode as edge-aligned mode or center-aligned mode ($T1CMS$);

6. Configure prescaler (T1PSC);
7. Enable the counter (T1CEN = 1).

Note:

1. It is recommended to read and write the value of counter T1CNT[15:0] when the counter is stopped (T1CEN = 0) to avoid errors.
2. Software cannot rewrite the T1CMS and T1DIR bits at the same time; when T1CMS = 00, T1DIR is a readable and writable register; when T1CMS ≠ 00, T1DIR is a read-only register, and the counting direction is automatically set by hardware after counting is started.
3. In center-aligned mode, it needs to set the initial count value $T1CNT \leq T1ARR$.
4. It is necessary to configure the cycle, output compare value, count mode and other registers first, and configure the prescaler register before enabling the counter (T1CEN = 1) .

7.2.2.2. Repetition Counter

When the shadow register (RCR) of the 8-bit repetition counter is not 0, it will be automatically decremented by 1 when the following events occur:

- Up count mode, per count overflow event;
- Down count mode, per count underflow event;
- Center-aligned mode, per count overflow or underflow event.

The update event (UEV) is generated only when the repetition counter is decremented to 0, i.e., the frequency of the update event can be set by the repetition counter. In addition, the counting cycle T1ARR, duty cycle T1CCR_x and other configurations can be changed in the update event interrupt handler, which is useful when generating a specific number of PWM signals (see [Section 7.2.4.2 PWM Mode](#)).

When an update event occurs, its shadow register (RCR) will be automatically updated to the preloaded T1REP value.

Note: When T1REP is configured and its value is not 0, it is recommended to turn on the Update Event Interrupt after the first update event, and its shadow register (RCR) will be reloaded to the T1REP value only when the next update event (UEV) occurs.

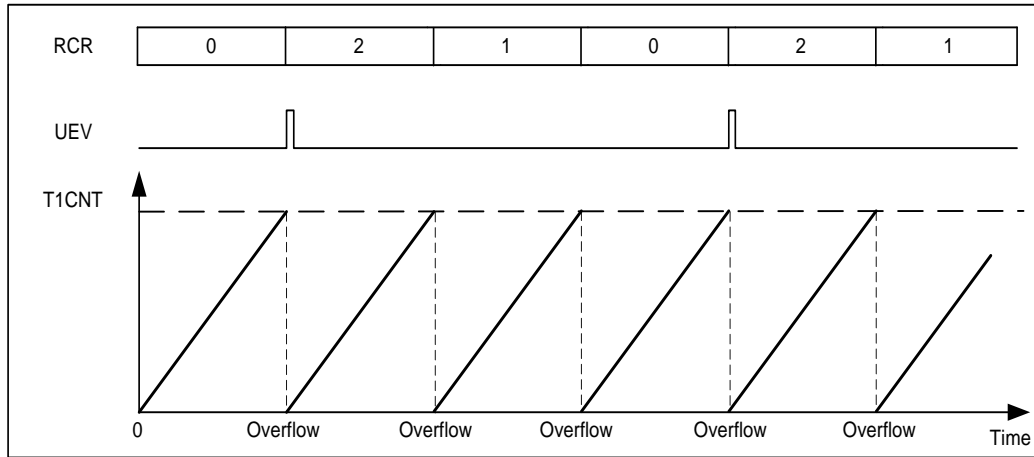


Figure 7-9 Repetition counter timing diagram (when T1REP = 2)

7.2.3. Clock/Trigger Controller

The clock/trigger controller includes the counter's clock source, trigger source, and mode control.

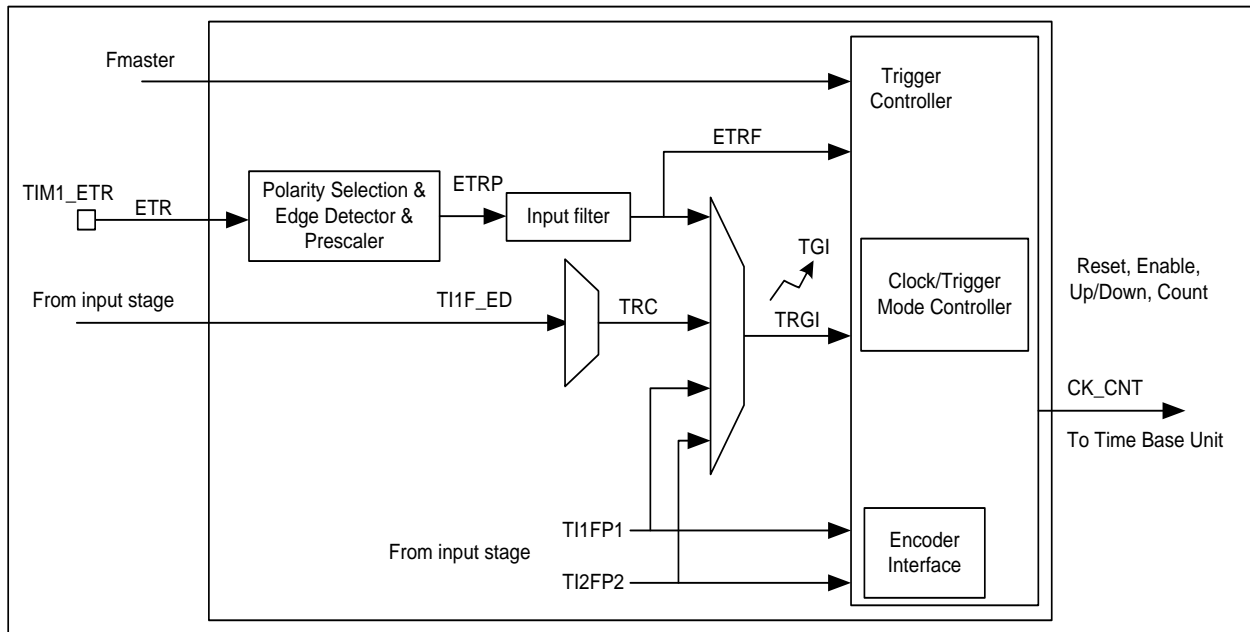


Figure 7-10 Clock/trigger controller Block Diagram

7.2.3.1. Counter Clock Source (Fmaster)

When T1SMS = 000, the counter is driven by the internal clock with the following optional 6 clock sources (see T1CKSRC):

- Sysclk
- 1x or 2x HIRC
- LIRC

- 1x or 2x external clock (Valid only if FOSC is configured to LP, XT or EC mode accordingly.)

7.2.3.2. Counter trigger source

When T1SMS ≠ 000 (Slave mode), the counter is driven by the trigger source (TRGI), and its optional 4 trigger event sources (see T1TS) are as follows:

- Channel 1 Input Edge Detector for TI1 (TI1F_ED)
- Filtered Channel 1 Input (TI1FP1)
- Filtered Channel 2 Input (TI2FP2)
- External Trigger Input (ETRF)

Note:

1. See T1CC1P/T1CC2P or T1ETP for the polarity of the active edge/active level of the trigger input;
2. When a trigger event occurs, the trigger interrupt flag T1TIF is set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE and T1TIE).

7.2.3.3. Counting control mode

The TIM1 counting control mode (see T1SMS and T1ECE) can select encoder mode 1/2/3, reset mode, gating mode, trigger mode and external clock mode 1/2 in addition to internal clock mode.

- **Internal Clock Mode** (T1SMS = 000):
The counter is driven by the internal clock (Fmaster).
- **Encoder mode :**
 - ✓ Encoder mode 1 (T1SMS = 001): the counter counts up/down on the active edge of TI2FP2 according to the TI1FP1 level.
 - ✓ Encoder mode 2 (T1SMS = 010): the counter counts up/down on the active edge of TI1FP1 according to the TI2FP2 level.
 - ✓ Encoder mode 3 (T1SMS = 011): the counter counts up/down on the active edge of TI2FP2/TI1FP1 according to the TI1FP1/TI2FP2 level.

Encoder Mode	Active counting edge	TI2FP2 Level	TI1FP1 Active Edge		TI1FP1 Level	TI2FP2 Active Edge	
			Rising	Falling		Rising	Falling
1	TI2FP2	-	-	-	High	Up	Down
		-	-	-	Low	Down	Up
2	TI1FP1	High	Down	Up	-	-	-
		Low	Up	Down	-	-	-
3	TI1FP1 or TI2FP2	High	Down	Up	High	Up	Down
		Low	Up	Down	Low	Down	Up

Table 7-19 Encoder modes (count direction vs. decode signal, T1CCxP = 0)

Encoder mode is mainly used in motor applications. The counting direction changes continuously with the combination of T11FP1 and T12FP2 signals.

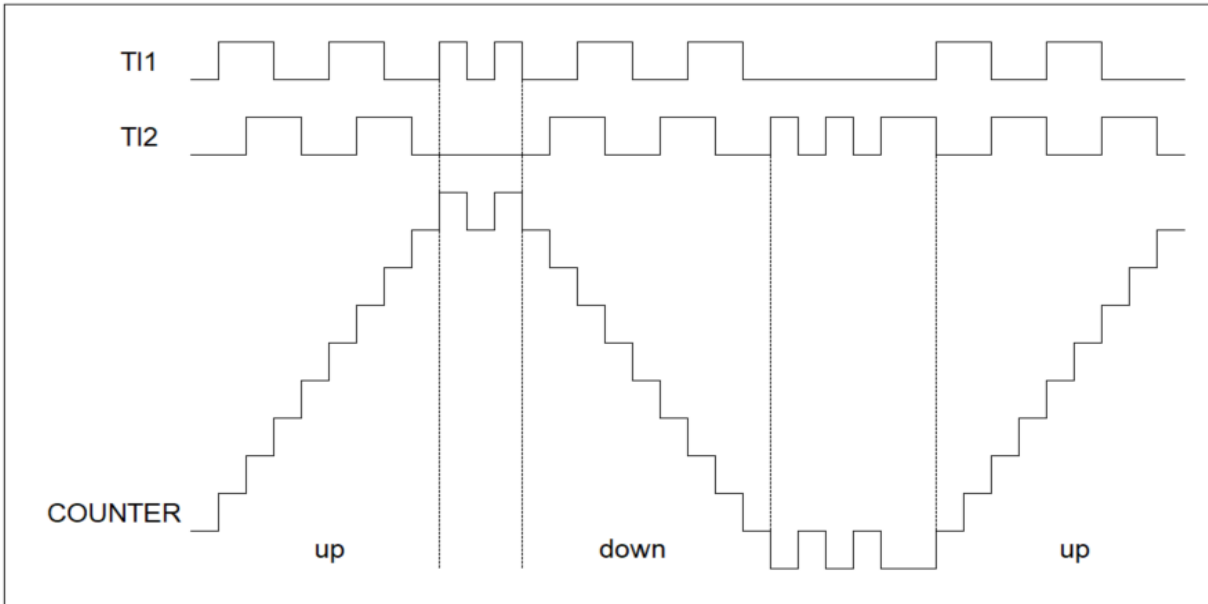


Figure 7-11 Encoder mode 3, counter timing diagram

The notes in encoder mode are as follows.

1. The input capture and output compare functions of Timer1 can work normally.
 2. The prescaler (T1PSC) function is disabled.
 3. It cannot be used simultaneously with external clock mode 2.
- **Reset Mode** (T1SMS = 100):

The counter starts to count normally driven by the internal clock until a active edge occurs on the trigger input (TRGI), at which t point the counter is cleared and starts counting again from 0. At the same time, the trigger flag T1TIF is set. In addition, when T1UDIS = 0 and T1URS = 0, an update event will be generated.

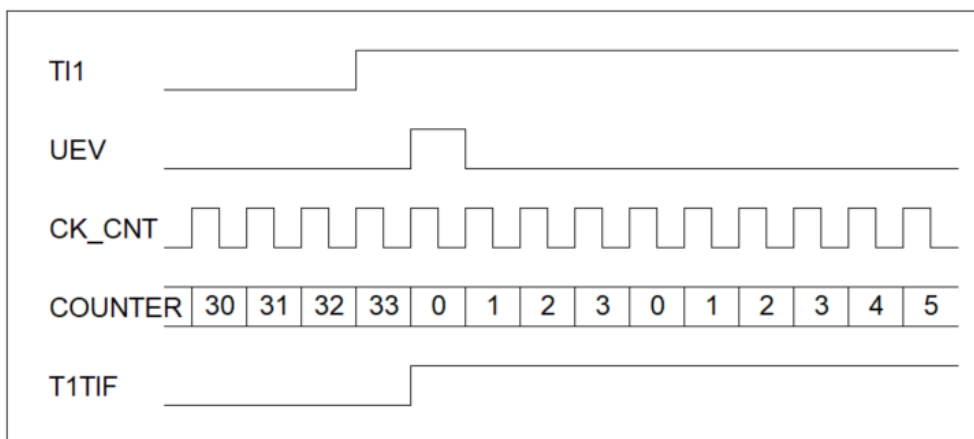


Figure 7-12 Reset mode, counter timing diagram (channel T11 is selected and the active edge of the trigger input is the rising edge)

- **Gating Mode** (T1SMS = 101):

The counter is driven to count by the internal clock during the active level of the trigger input (TRGI), and stops counting during the inactive level, but does not reset. Trigger flag T1TIF is set when the counter starts or stops.

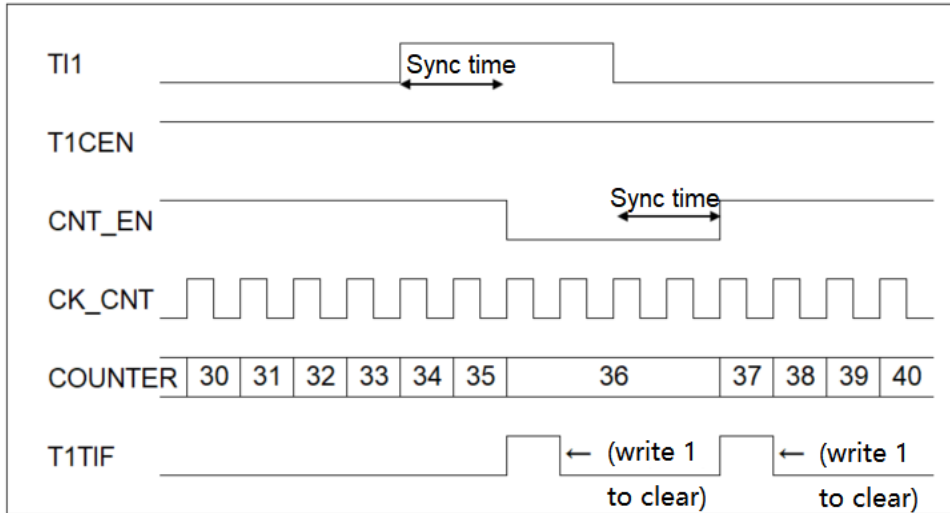


Figure 7-13 Gating mode, counter timing diagram (select Channel T11 and trigger input active level is low)

- **Trigger Mode** (T1SMS = 110):

The counter is driven by the internal clock on the active edge of the trigger input (TRGI) and is not reset. At the same time, the trigger flag T1TIF is set.

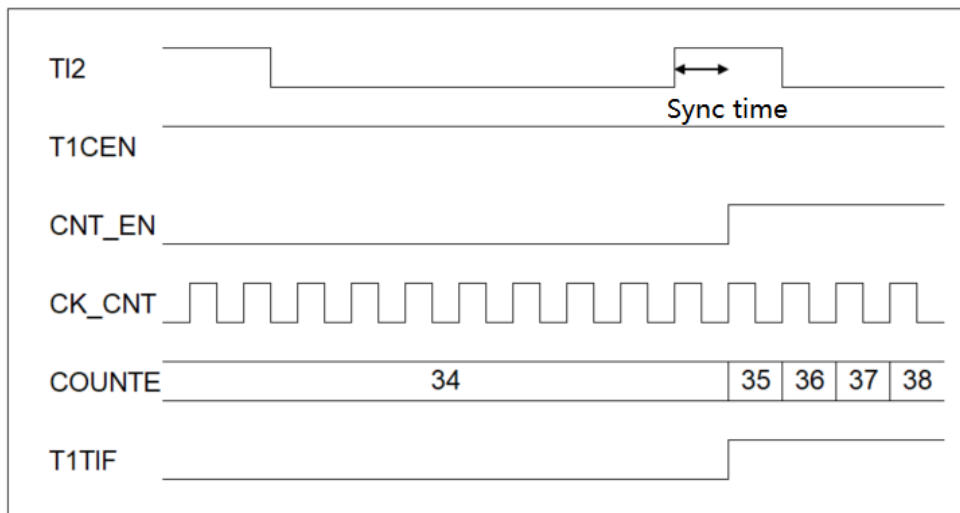


Figure 7-14 Trigger mode, counter timing diagram (select Channel T12 and the active edge of the trigger input is the rising edge)

- **External Clock Mode 1** (T1SMS = 111):

The counter counts on the active edge of the trigger input (TRGI). At the same time, the trigger flag T1TIF is set.

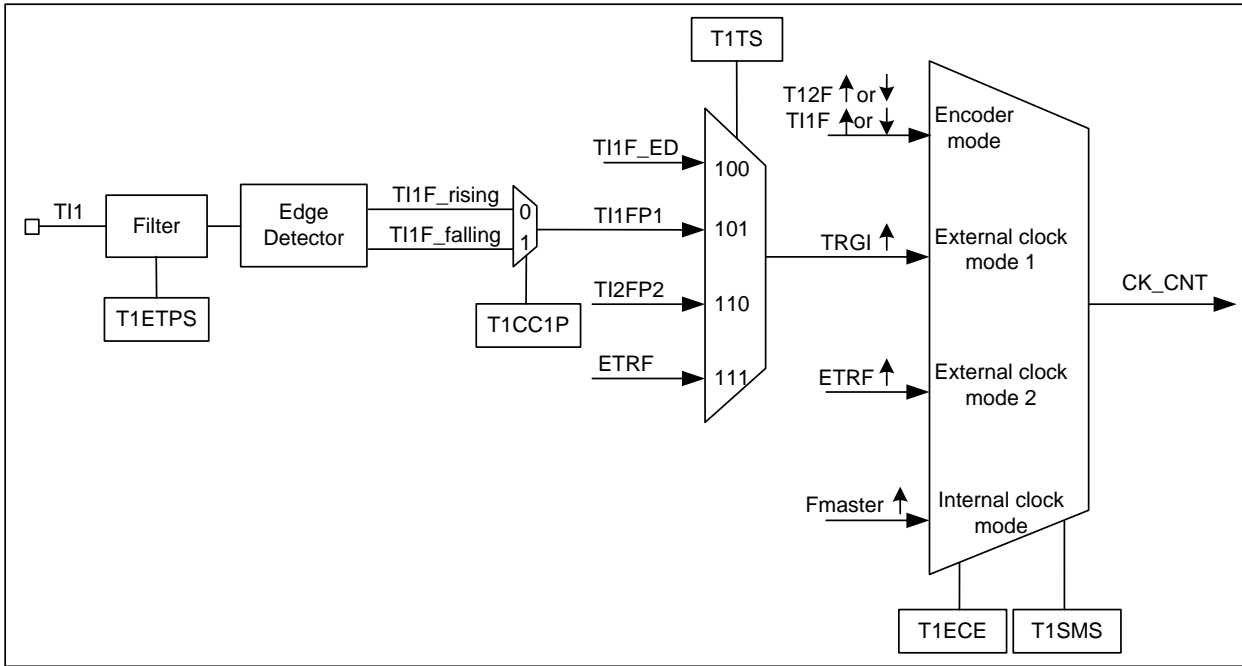


Figure 7-15 Block Diagram of external clock mode 1 (with T11 as the count clock source)

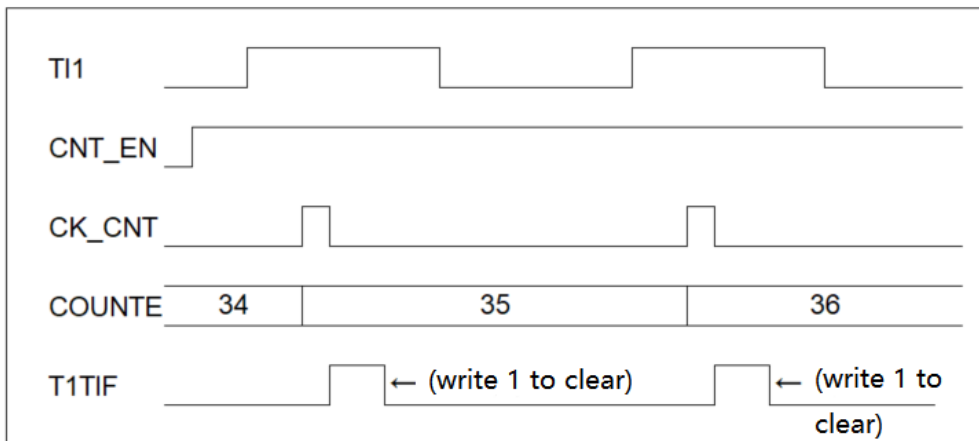


Figure 7-16 External clock mode 1, counter timing diagram (select channel T11 and trigger input active edge is rising edge)

- **External Clock Mode 2 (T1ECE = 1):**

The counter counts on the active edge of the trigger input (ETRF).

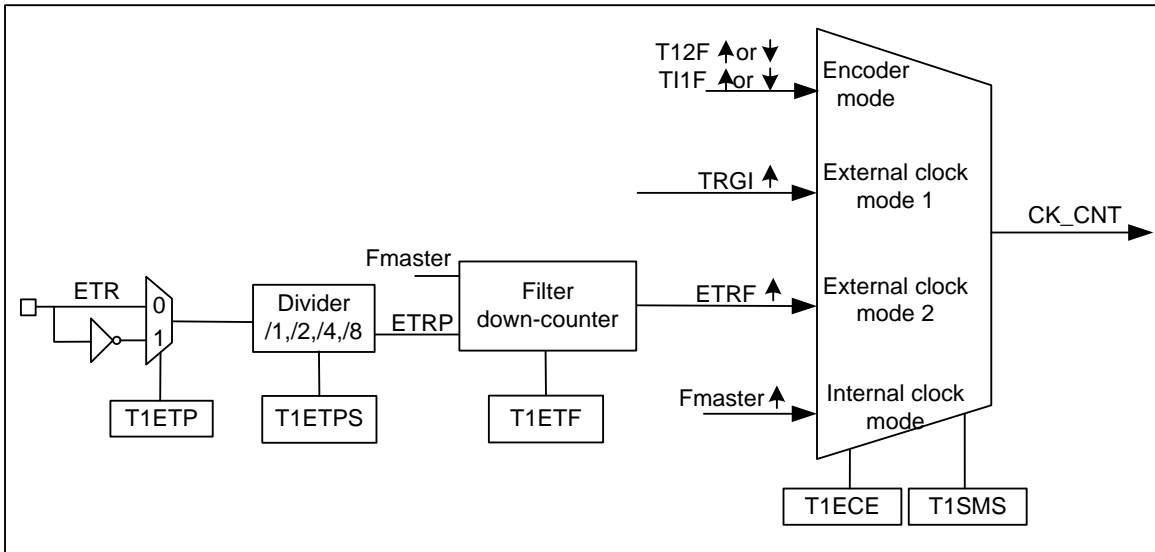


Figure 7-17 External clock mode 2 Block Diagram

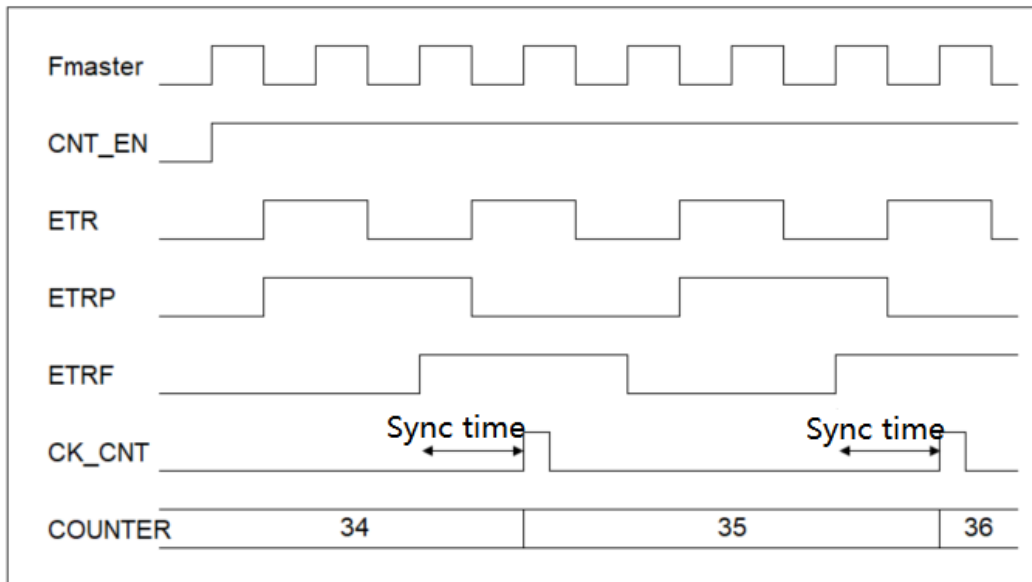


Figure 7-18 External Clock Mode 2, Counter Timing Diagram

Example of configuration steps for control modes (except external clock mode 2):

1. Enable the TIM1 module clock (TIM1EN = 1), and select the TIM1 clock source (T1CKSRC).
2. Configure the selected channel port as the input (TRISx = 1);
3. Configure input capture sampling frequency and filter length for Channel x (T1ICxF);
4. Configure input capture prescaler for Channel x (T1ICxPSC);
5. Select the input capture channel (T1CC1S/T1CC2S) as needed;
6. Configure the active edge or active level of the trigger input (T1CC1P/T1CC2P);
7. Select the counting control mode as reset mode, gating mode or trigger mode (T1SMS), and select the trigger input source (T1TS);

8. Enable the counter (T1CEN = 1);

Program Example 1 (Take encoder mode 3 as an example, please see the timing diagram shown in [Figure 7-11](#)):

```

BANKSEL PCKEN
BSR PCKEN,0           ; Enable TIM1 module clock
BANKSEL TCKSRC
LDWI 01H
STR TCKSRC           ; Select TIM1 clock source as HIRC
BANKSEL TRISA
LDWI 03H
STR TRISA           ; Configure Channel1 PORT PA0 and Channel2 PORT PA1 as input
BANKSEL TIM1CCMR1
LDWI 01H
STR TIM1CCMR1       ; Configure Channel1 input capture filter length, prescaler, and the input
pin is mapped on TI1FP1
LDWI 01H
STR TIM1CCMR2       ; Configure Channel2 input capture filter length, prescaler, and the input
pin is mapped on TI2FP2
LDWI 53H
STR TIM1SMCR        ; Configure TIM1 for encoder mode 3
LDWI 11H
STR TIM1CCER1       ; Enable channels 1 and 2 to be input, and the active level of the trigger
input is low

BANKSEL TIM1CR1
BSR TIM1CR1,0       ; Enable the counter

```

Program Example 2 (take the Gating mode as an example, see the timing diagram shown in [Figure 7-13](#)):

```

BANKSEL PCKEN
BSR PCKEN,0           ; Enable TIM1 module clock
BANKSEL TCKSRC
LDWI 01H
STR TCKSRC           ; Select TIM1 clock source as HIRC
BANKSEL TRISA
LDWI 01H
STR TRISA           ; Configure Channel1 PORT PA0 as input
BANKSEL TIM1CCMR1
LDWI 01H
STR TIM1CCMR1       ; Configure Channel1 input capture filter length, prescaler, and the input
pin is mapped on TI1FP1

LDWI 55H
STR TIM1SMCR        ; Configure TIM1 as gating control mode, trigger source is TI1FP1
LDWI 03H
STR TIM1CCER1       ; Enable Channel1 as input, and trigger input active level is low level
BANKSEL TIM1CR1

```

```
BSR TIM1CR1,0          ; Enable the counter
BTSS TIM1SR1,6         ; Determine whether the trigger interrupt flag is high
LJUMP $-1
BCR TIM1SR1,6          ; Clear the trigger interrupt flag bit
```

Example of configuration steps for external clock mode 2:

1. Enable the TIM1 module clock (TIM1EN = 1), and select the TIM1 clock source (T1CKSRC);
2. Configure the selected ETR external channel port as an input (TRISx = 1);
3. Configure external trigger prescaler (T1ETPS), and external trigger sampling frequency and filter length (T1ETF);
4. Configure the active edge or active level (T1ETP) of the external trigger input;
5. Select the counting control mode as external clock mode 2 (T1ECE);
6. Enable the counter (T1CEN = 1);

Program Example (see timing diagram [Figure 7-18](#)):

```
BANKSEL PCKEN
BSR PCKEN,0           ; Enable TIM1 module clock
BANKSEL TCKSRC
LDWI 01H
STR TCKSRC            ; Select TIM1 clock source as HIRC
BANKSEL TRISB
LDWI 08H
STR TRISB             ; Configure ETR external channel PB3 as input
BANKSEL TIM1ETR
LDWI 50H
STR TIM1ETR           ; Configure external trigger prescaler, filter, polarity, and enable external
clock mode 2
BANKSEL TIM1CR1
BSR TIM1CR1,0        ; Enable the counter
```

7.2.4. Capture/Compare Channels

The CH1~4 PORTS of TIM1 can be configured as Input Capture or Output Compare function (see the T1CCxS bit of the multiplexing register TIM1CCMRx).

updated directly to the preload value.

	PWM Sync Mode	PWM Group Mode	Channel x Pin Function	Complementary Channel x Pin Function	Channel x Polarity	Complementary Channel x Polarity	Channel x Output Compare Mode
Preload Register	T1SMOD	T1GP	T1CCxE	T1CCxNE	T1CCxP	T1CCxNP	T1OCxM
Preload enable	T1CCPC						

Table 7-20 Preload registers related to commutation events

7.2.4.1. Input capture mode

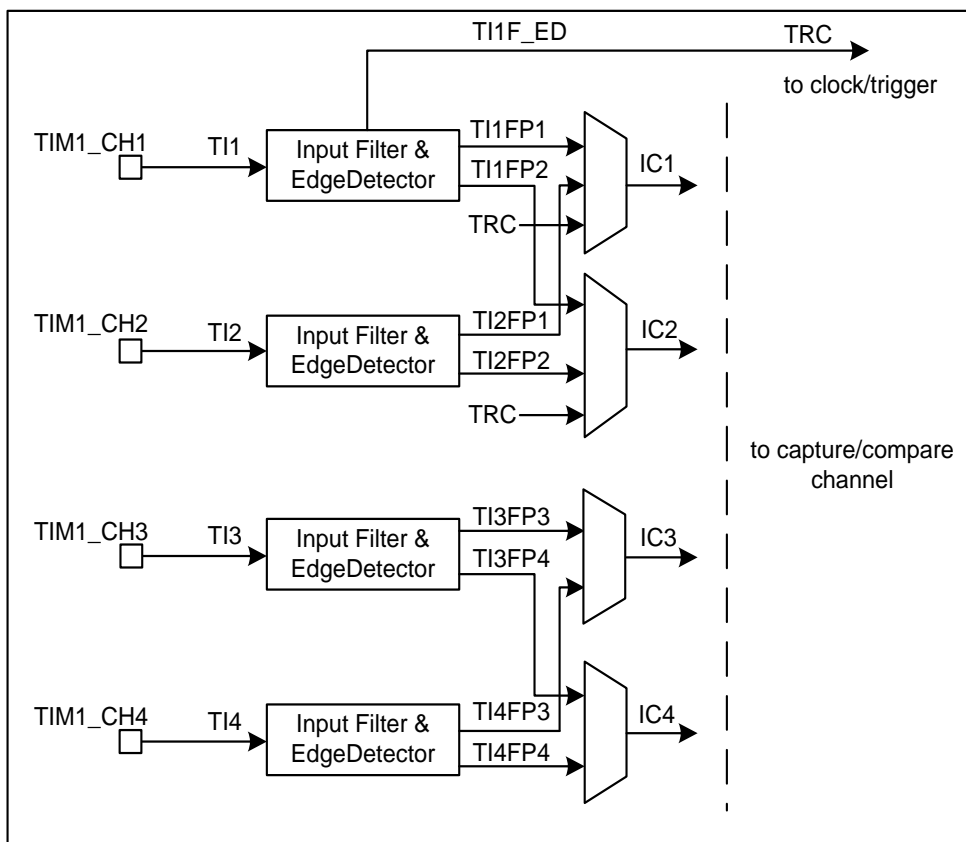


Figure 7-20 Input capture channel Block Diagram

In input capture mode, when an input capture event occurs in channel x, the current count value will be captured into the T1CCRx[15:0] register, and the input capture flag T1CCxIF will be set. If an input capture event occurs again while T1CCxIF remains 1, the repeat capture flag bit T1CCxOF will be set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE and T1CCxIE). In addition, the input capture software interrupt bit T1CCxG can be enabled to trigger an interrupt.

The input capture sources for each channel of TIM1 (see T1CCxS) are as follows:

T1CCxS	Channel1	Channel2	Channel3	Channel4
01	TI1FP1	TI2FP2	TI3FP3	TI4FP4
10	TI2FP1	TI1FP2	TI4FP3	TI3FP4
11	TRC	TRC	-	-

Table 7-21 Input capture sources for each channel

Note: When the capture source of channel x (x = 1/2/3/4) is selected as the input capture signal of the corresponding I/O of other channels, the other channels need to be set as inputs. For example, if channel 1 selects TI2FP1 (T1CC1S = 10), channel 2 must be set as input (T1CC2S = 01 or 10); channel 3 and channel 4 as above.

Signal Name	Detailed description
TIM1_CH1/2/3/4	I/O input corresponding to Channel1/2/3/4
IC1/2/3/4	Capture source via selected channel
TI1FP1	Channel1 corresponds to the input capture signal of the I/O, as one of the capture sources of Channel1
TI1FP2	Channel1 corresponds to the input capture signal of I/O, as one of the capture sources of Channel2
TI2FP2	Channel2 corresponds to the input capture signal of the I/O as one of the capture sources of Channel2
TI2FP1	Channel2 corresponds to the input capture signal of I/O, as one of the capture sources of Channel1
TI3FP3	Channel3 corresponds to the input capture signal of the I/O as one of the capture sources of Channel3
TI3FP4	Channel3 corresponds to the input capture signal of I/O, as one of the capture sources of channel4
TI4FP4	Channel4 corresponds to the input capture signal of I/O, as one of the capture sources of channel4
TI4FP3	Channel4 corresponds to the input capture signal of I/O, as one of the capture sources of Channel3
TRC	Channel1 corresponds to the input double-edge capture signal of I/O, as one of the capture sources of channels 1 and 2

Table 7-22 Input Capture Signal Description

Example of configuration steps for an input capture channel:

1. Enable the TIM1 module clock (TIM1EN = 1), and select the TIM1 clock source (T1CKSRC).
2. Configure the selected channel PORT as the input (TRISx = 1).
3. Select input capture source (T1CCxS).
4. Configure the polarity of the capture source (T1CCxP).

5. Configure the capture sampling frequency and filter length of channel x (T1ICxF[3:0]) and capture prescaler (T1IC1PSC[1:0]).
6. Input capture interrupts (GIE, PEIE, T1CCxE) can be enabled as needed.
7. Enable capture channel (T1CCxE = 1).
8. Enable the counter (T1CEN = 1).

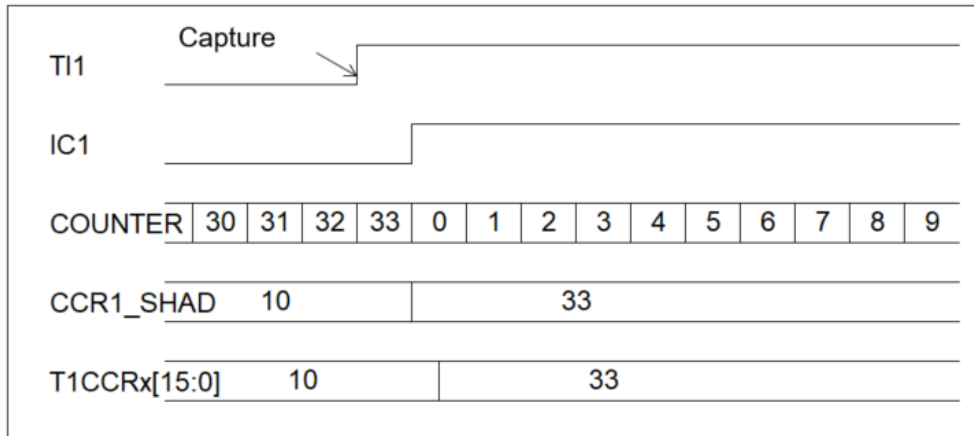


Figure 7-21 Input Capture Timing Diagram

PWM signal measurement application: the cycle and duty cycle of PWM signal can be measured by using input capture mode and reset mode, and selecting the input capture source of two channels as the PWM signal input of the same channel.

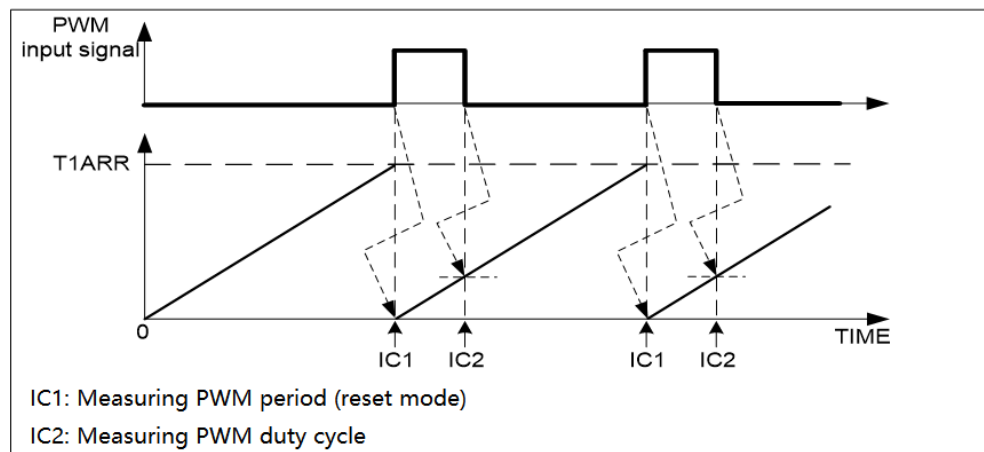


Figure 7-22 Schematic Diagram of Measuring PWM Signal

Example of configuration steps to measure PWM:

1. Enable the TIM1 module clock (TIM1EN = 1), and select the TIM1 clock source (T1CKSRC);
2. Configure the PORT corresponding to Channel1/2 as input (TRISx = 1);
3. Select the input capture source (T1CCxS), map IC1 of Channel1 to T11FP1, and map IC2 of Channel2 to T12FP1;

4. Configure the polarity of the capture source, configure Channel1 as rising edge (T1CC1P = 0) and Channel2 as falling edge (T1CC2P = 1);
5. Configure capture sampling frequency and filter length (T1ICxF[3:0] = 0000), capture prescaler (T1IC1PSC[1:0] = 00);
6. Configure the counting control mode as reset mode (T1SMS = 101), and the counting trigger source as TI1FP1 (T1TS = 101);
7. Enable the input capture function of Channel1 and Channel2 (T1CC1E=1 and T1CC2E=1);
8. Enable the counter (T1CEN = 1);

Note: Since the capture edge precedes the reset trigger source by two count clock cycles, in order to obtain an accurate measurement value, the software needs to do the following:

- When Prescaler = 0, PWM period = T1CCR1H/L+2, Duty Cycle = T1CCR2H/L+2.
- When Prescaler = 1, PWM period = T1CCR1H/L+1, Duty Cycle = T1CCR2H/L+1.
- When Prescaler ≥ 1, PWM period = T1CCR1H/L, Duty Cycle = T1CCR2H/L.

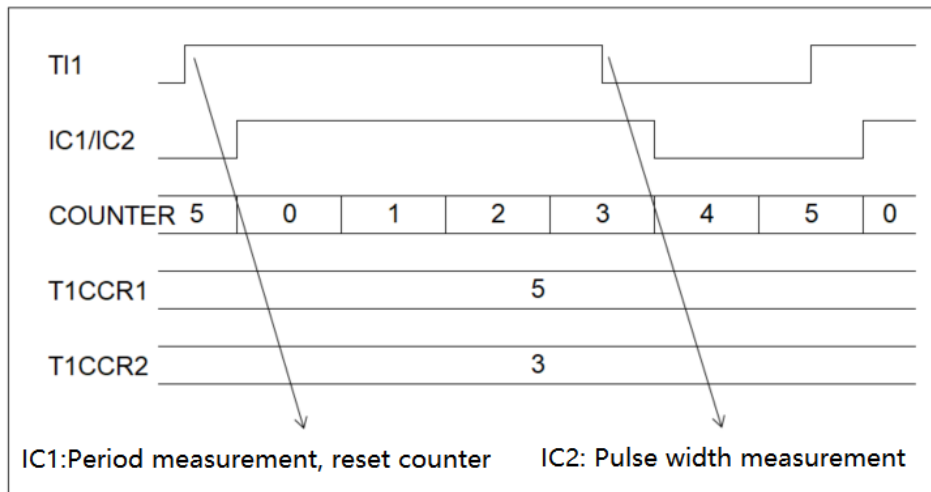


Figure 7-23 Timing Diagram for Measuring PWM Signal

7.2.4.2. Output compare mode

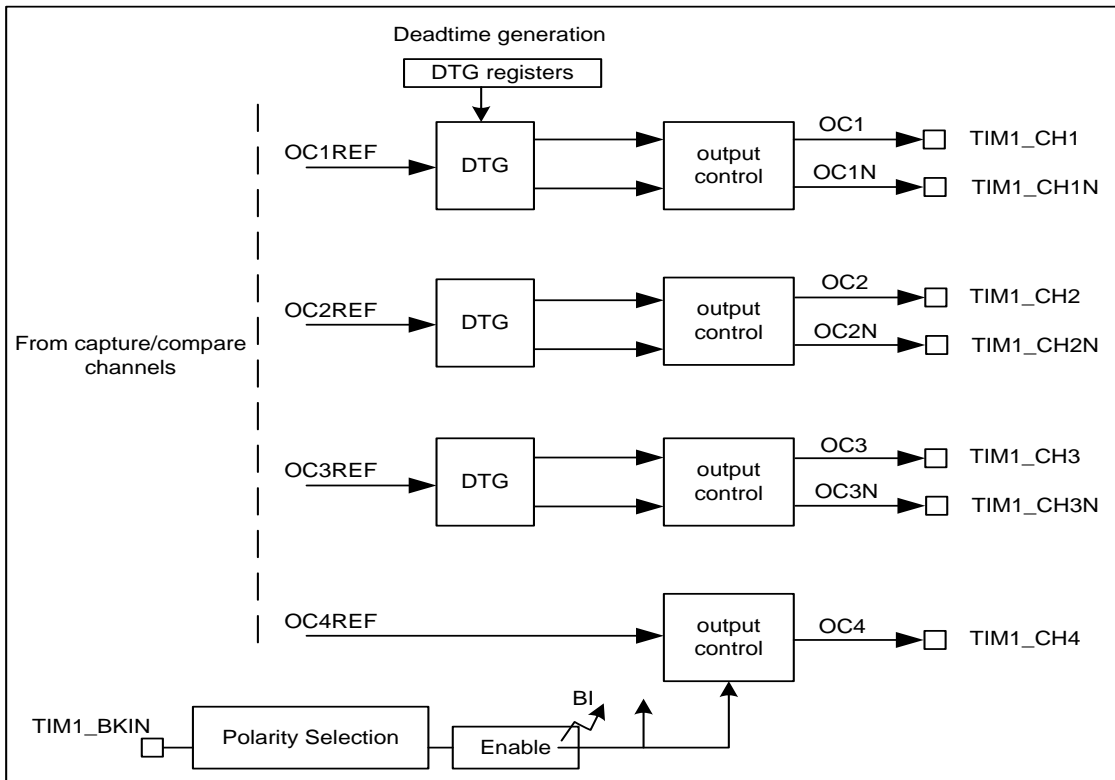


Figure 7-24 Block Diagram of Output Compare Channel

The output compare module compares the count value (T1CNT) with the comparison value (shadow register CCRx_SHAD), first generates the output reference signal OCxREF (active high), and then sends it to the Deadband generation module or break module, and then outputs the waveform to the port (see Table 7-14) through polarity selection and other output controls (see T1MOE, T1OSSI, T1OSSR, T1CCxE and T1CCxNE).

The reference signal OCxREF can be configured to 8 output modes through T1OCxM[2:0] (see Table 7-9):

1. Frozen mode (T1OCxM = 000): OCxREF value remains unchanged.
2. Active level on match (T1OCxM = 001): OCxREF = 1 when T1CNT = CCRx_SHAD.
3. Inactive level on match (T1OCxM = 010): OCxREF = 0 when T1CNT = CCRx_SHAD.
4. Toggle on match (T1OCxM = 011): When T1CNT = CCRx_SHAD, the OCxREF value is reversed.
5. Forced inactive (T1OCxM = 100): OCxREF is always 0.
6. Forced active (T1OCxM = 101): OCxREF is always 1.
7. PWM1 mode (T1OCxM = 110).

When T1CNT < CCRx_SHAD, OCxREF = 1; when T1CNT > CCRx_SHAD, OCxREF = 0.

8. PWM2 mode (T1OCxM = 111).

When T1CNT < CCRx_SHAD, OCxREF = 0; when T1CNT > CCRx_SHAD, OCxREF = 1.

When T1CNT matches CCRx_SHAD, the output compare flag T1CCxIF is set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE, T1CCxIE). In addition, the output compare software Interrupt T1CCxG, can be enabled to trigger an interrupt.

Configuration steps for the output compare channel:

1. Enable the TIM1 module clock (TIM1EN = 1), and select the TIM1 clock source (T1CKSRC).
2. Configure the PORT corresponding to the channel as an output (TRISx = 0).
3. Configure the cycle (T1ARR) and comparison value (T1CCRx) of the output waveform.
4. Configure output compare mode (T1OCxM) and output polarity (T1CCxP).
5. Output compare interrupts (GIE, PEIE, T1CCxIE) can be enabled as needed.
6. Enable output compare channel (T1CCxE = 1).
7. Enable the main output automatic control bit (T1AOE = 1), that is, the hardware will automatically enable the main output (T1MOE) when an update event occurs.
8. Enable the counter (T1CEN = 1).

Note: It is recommended to configure the output compare value T1CCRx ≤ the counting cycle value T1ARR.

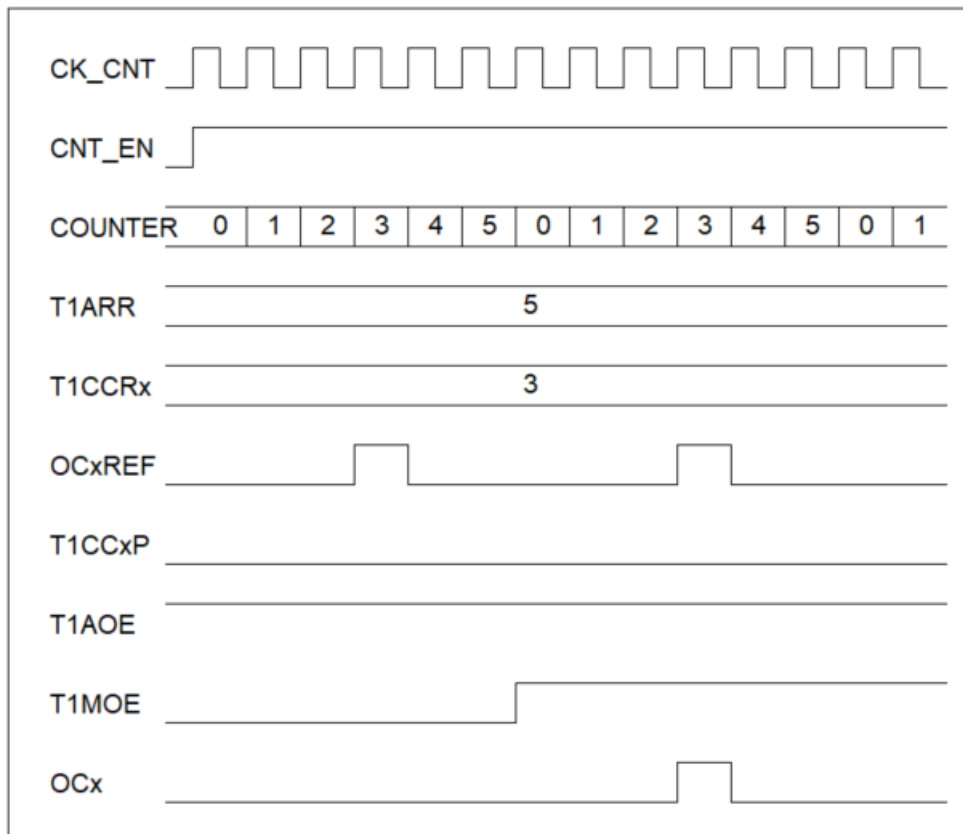


Figure 7-25 Output Timing Diagram with Active Level on Match

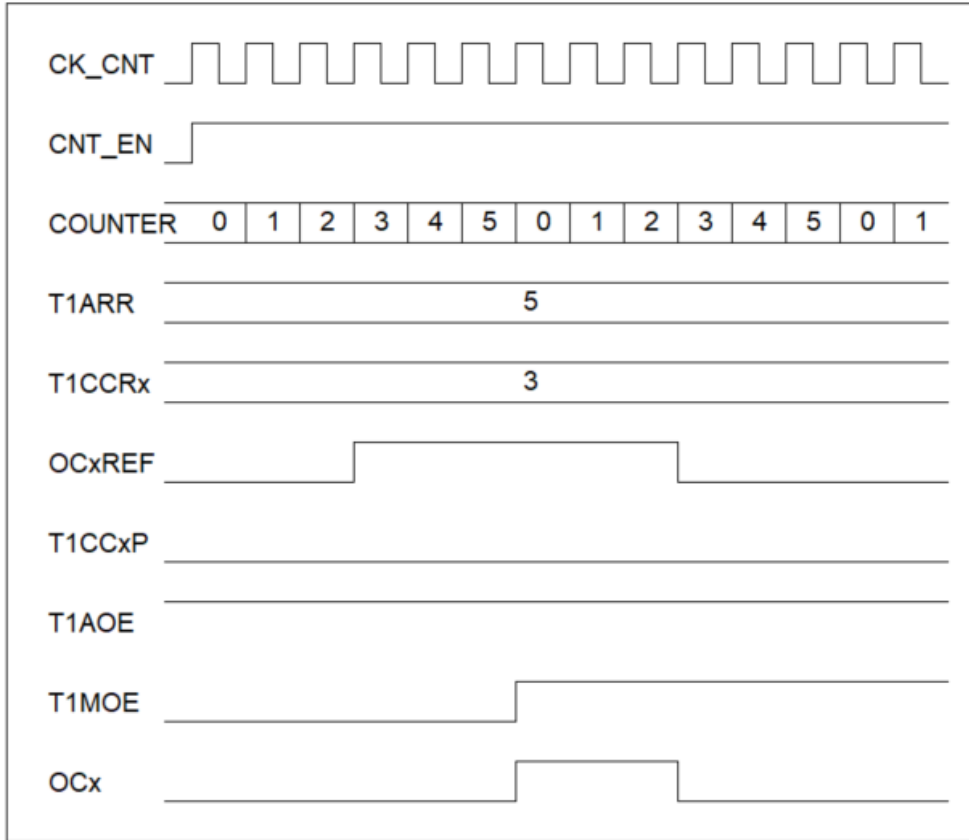


Figure 7-26 Output Timing Diagram when Toggle on Match

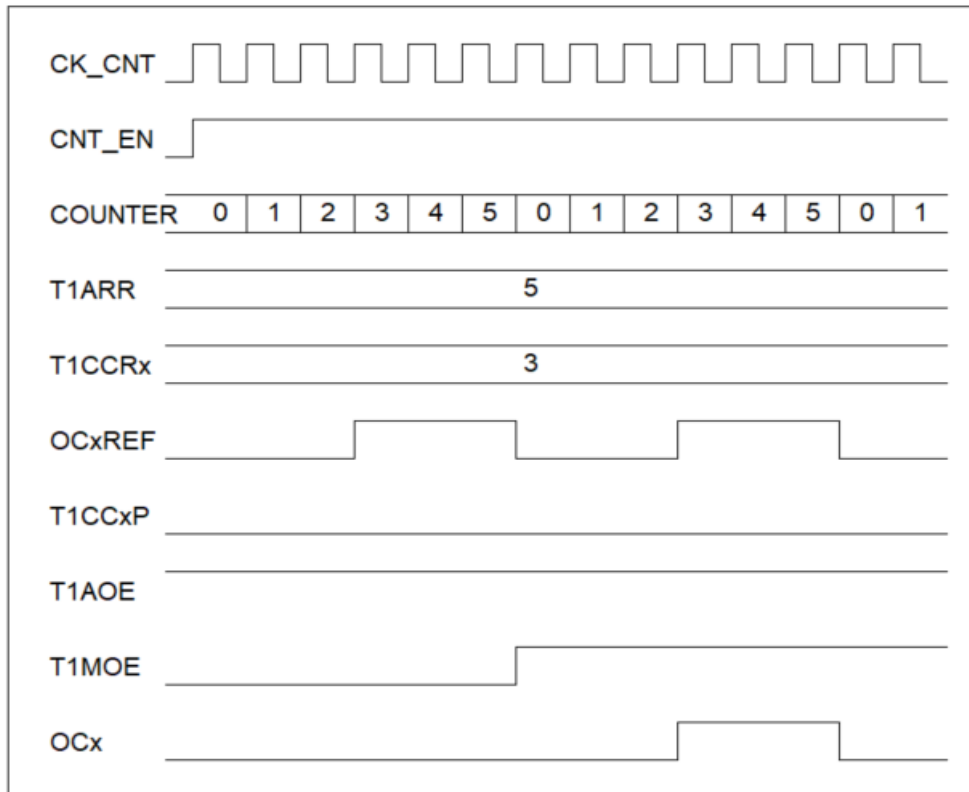


Figure 7-27 Output Timing Diagram in PWM2 Mode

PWM Mode – PWM1/PWM2 cycle is determined by T1ARR and the duty cycle is determined by T1CCRx.

Equation 7-1 $PWM1/2 \text{ Cycle} = (T1ARR+1) * T_{CK_CNT}$

Equation 7-2 $PWM1/2 \text{ Duty Cycle} = T1CCRx \div (T1ARR+1)$

TIM1_CH1/2/3/4 channels can independently enable output PWM signal, among which CH1/2/3 have complementary output function. The polarity of the output signal as well as the complementary output signal is selectable (see T1CCxP/ T1CCxNP). When the output channel and the complementary output channel are enabled simultaneously (T1CCxE = 1, T1CCxNE = 1), the Deadband function will be automatically enabled, and the Dead-Time can be set(see T1DTG), i.e. whenever the falling edge of output signal (OCx or complementary output OCxN) occurs, the rising edge of the other signal will be delayed by the length of deadband.

Note: In PWM mode, the auto-preload function of channel x duty cycle must be enabled (T1OCxPE = 1);

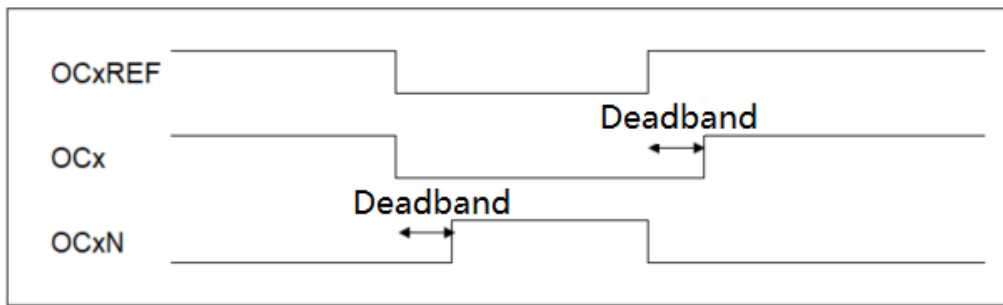


Figure 7-28 Complementary Output with Deadband Timing Diagram

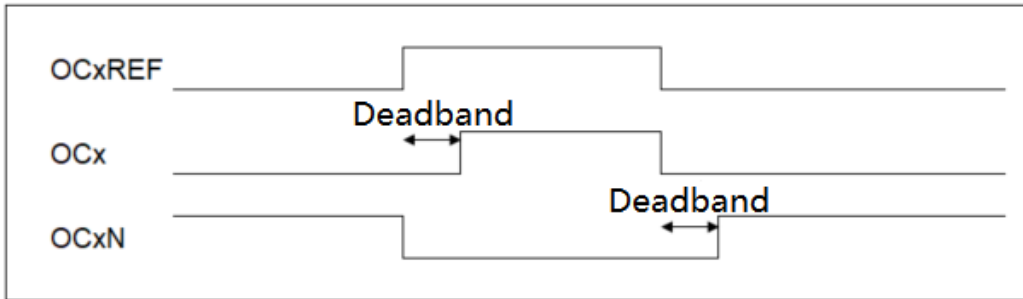


Figure 7-29 Positive Output with Deadband Timing Diagram

When the pulse time of the OCxREF output is shorter than the deadband, a certain pulse signal may be covered by the deadband, resulting in the output unchanged.

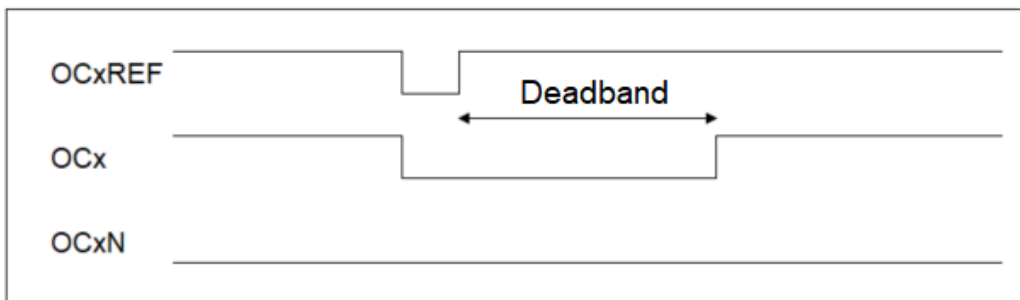


Figure 7-30 Complementary Output Covered by Deadband Timing Diagram

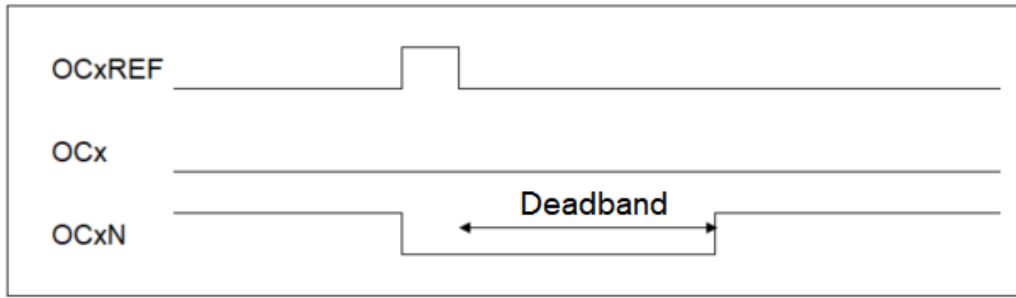


Figure 7-31 Positive Output Covered by Deadband Timing Diagram

The PWM mode is used in conjunction with functions such as repetition counter, update event, cycle preload, and duty cycle preload to generate a specific number of PWM signals.

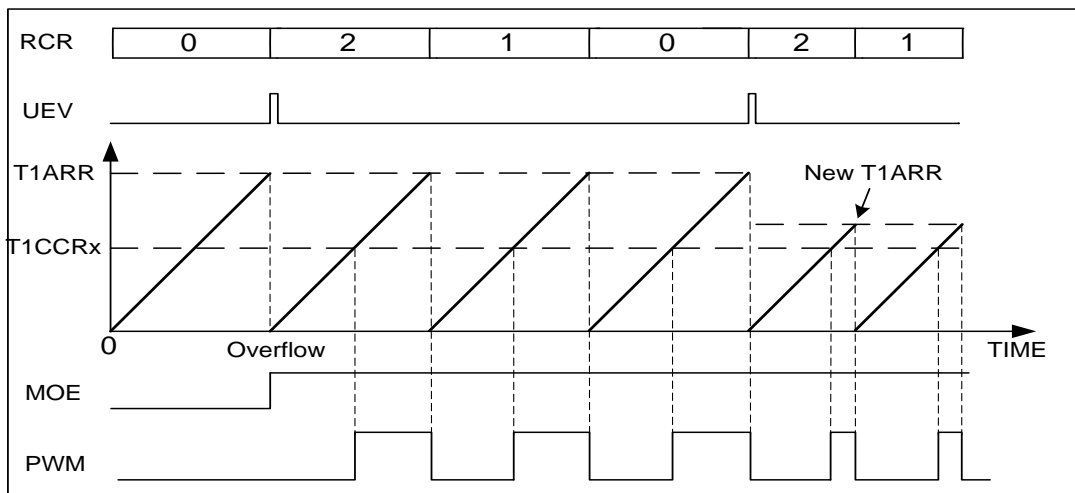


Figure 7-32 Timing Diagram of Outputting 3 Specific PWMs by Repeation Counter

Program Example:

```

BANKSEL PCKEN
BSR PCKEN,0           ; Enable TIM1 module clock
BANKSEL INTCON
LDWI C0H
STR INTCON             ; Enable global and peripheral interrupts
BANKSEL TCKSRC
LDWI 01H
STR TCKSRC             ; Select TIM1 clock source as HIRC
BANKSEL TRISA
LDWI 00H
STR TRISA              ; Configure Channel1 PORT PA0 as output
BANKSEL TIM1ARRL
LDWI 1FH
STR TIM1ARRL          ; Configure the output waveform cycle to 32
LDWI 10H
STR TIM1CCR1L         ; Configure the output waveform duty cycle to 16
LDWI 02H
    
```

```

STR TIM1RCR           ; Configure the repetition counter to 2
BANKSEL TIM1CCMR1
LDWI 70H
STR TIM1CCMR1        ; Configure Channel1 as PWM2 mode output
BSR TIM1IER,0        ; Enable update event interrupt
LDWI 01H
STR TIM1CCER1        ; Enable Channel1 and select polarity
BANKSEL TIM1BKR
BSR TIM1BKR,6        ; Turn on the main output auto-enable bit
BANKSEL TIM1CR1
LDWI 81H
STR TIM1CR1          ; Enable cycle preload function and enable counter
INT :
BANKSEL TIM1ARRL
LDWI 14H
STR TIM1ARRL         ; Reconfigure the output waveform cycle to 20
    
```

One-Pulse Mode – In One-Pulse Mode ($T1OPM = 1$), when the next update event occurs, the hardware turns off the counter enable ($T1CEN = 0$) automatically and the counter stops counting.

To generate a correct pulse, the initial value ($T1CNT$) of the counter must be different from the comparison value ($T1CCR_x$). That is, the following configurations must be met before starting counting:

- Up count mode: $T1CNT < T1CCR_x \leq T1ARR$
- Down count mode: $T1CNT > T1CCR_x$

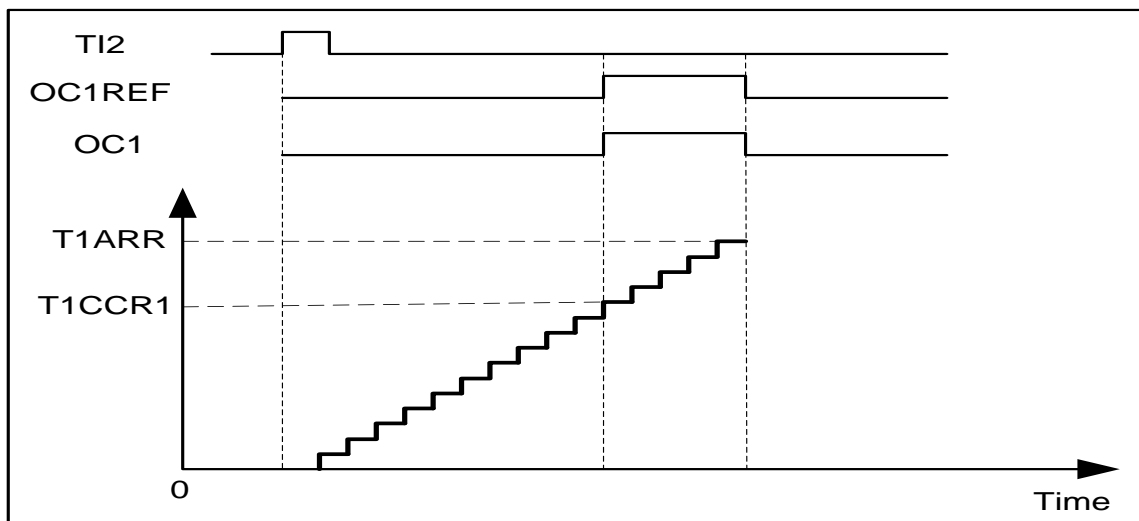


Figure 7-33 Schematic diagram of One-Pulse application

The One-Pulse mode can cooperate with the trigger mode to generate a One-Pulse output at a specific time point, as shown in the figure above. The configuration steps are as follows:

1. Enable the TIM1 module clock ($TIM1EN = 1$), and select the TIM1 clock source ($T1CKSRC$).
2. Configure the PORT corresponding to Channel2 as input and the PORT corresponding to Channel1 as output.

3. Map the input of Channel2 to TI2FP2 (T1CC2S = 01) and select it as rising edge capture (T1CC2P = 0).
4. Configure the counting control mode as trigger mode (T1SMS = 110), and select TI2FP2 (T1TS = 110) as the trigger source.
5. Configure Channel1 as an output channel (T1CC1S = 00).
6. Configure Channel1 as PWM2 mode in output compare mode (T1OC1M = 111), with output polarity configured as active at high level (T1CC1P = 0).
7. Enable the input capture function of Channel2 (T1CC2E=1) and the output compare function of Channel1 (T1CC1E).
8. Enable the main output automatic control bit (T1AOE = 1), that is, the hardware will automatically enable the main output (T1MOE) when an update event occurs.
9. Enable the counter (T1CEN = 1).

Fast Output – When in Trigger mode cooperated with the PWM / One-Pulse mode, the active edge of the trigger input enables the counter to count, and the comparison of the count value with the T1CCRx value will change the output. However, there will be a minimum delay between the trigger input edge when changing and the real output waveform, which can be shortened by setting T1OCxFE.

Sync Mode – The complementary output of channel 1/2/3 is identical to its forward output signals (see "T1SMOD"). In synchronous mode, the hardware automatically disables the deadband function.

Group Mode – The duty cycle of Channel1/2/3 and its complementary output is determined by T1CCR1 [15:0], the original configuration T1CCR2 [15:0] and T1CCR3 [15:0] are invalid (see "T1GP").

TIM1/TIM2 Sync Trigger Mode – The internal enable signal of TIM2 is completely controlled by TICEN of TIM1 (see "T1ENCTRL"). The configuration process is as follows:

1. Configure the corresponding functions of TIM1 and TIM2 at first.
2. Configure T1ENCTRL = 1 to enable synchronous trigger function.
3. Configure TICEN = 1 to enable both TIM1 and TIM2.

7.2.4.3. Fault-Break Function

All 4 PWMs support Fault-Break function. When the break input function is enabled (T1BKE = 1), PWM will output a preset condition(see TIM1OISR) according to its setting upon a Fault-Break event. The PWM will be in this condition as long as the break condition is valid.

Fault-Break event of TIM1 can be one of the followings (see BKS):

- BKIN Event
- LVD Event
- ADC Threshold Comparison Event

When a Fault-Break event occurs, the PWM Output and Complementary Output status (see [Table 7-14](#)) are as follows:

- If the clock source of TIM1 is disabled, T1MOE will be cleared asynchronously, forcing the output to be inactive;

- If the clock source of TIM1 is enabled, T1MOE will be cleared asynchronously, the output will be in an inactive state during the deadband, and will be in an idle state after the deadband (in this case, the real deadband is 2 CK_CNT clocks longer than the setting value);

Meanwhile, the break interrupt flag T1BIF is set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE, T1BIE). In addition, the break software interrupt T1BG can be enabled to trigger an interrupt.

After the Fault event is cancelled, if the main output automatic control bit T1AOE = 1, then T1MOE will be automatically set by hardware when the next update event (UEV) arrives (2 CK_CNT clocks need to be synchronized), and the PWM will resume normal output. Otherwise, T1MOE needs to be set by software to resume the output.

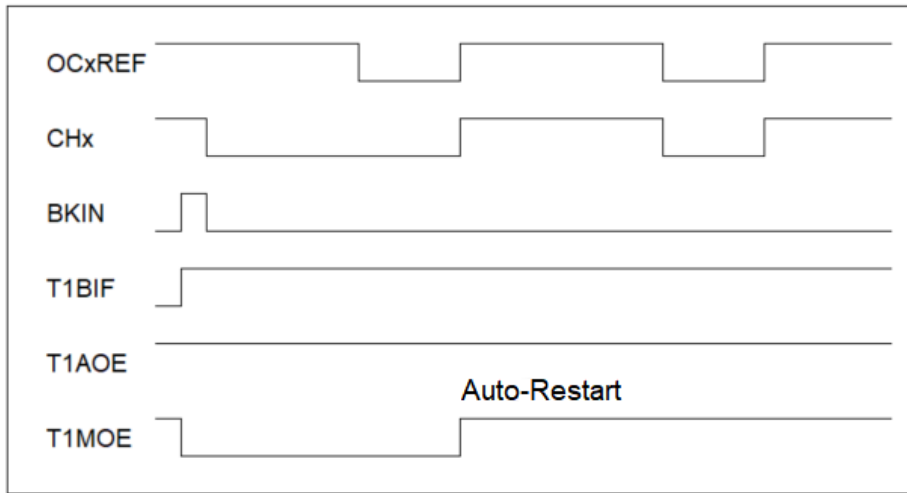


Figure 7-34 PWM Auto-Restart Diagram

7.3. General-purpose TIMER2

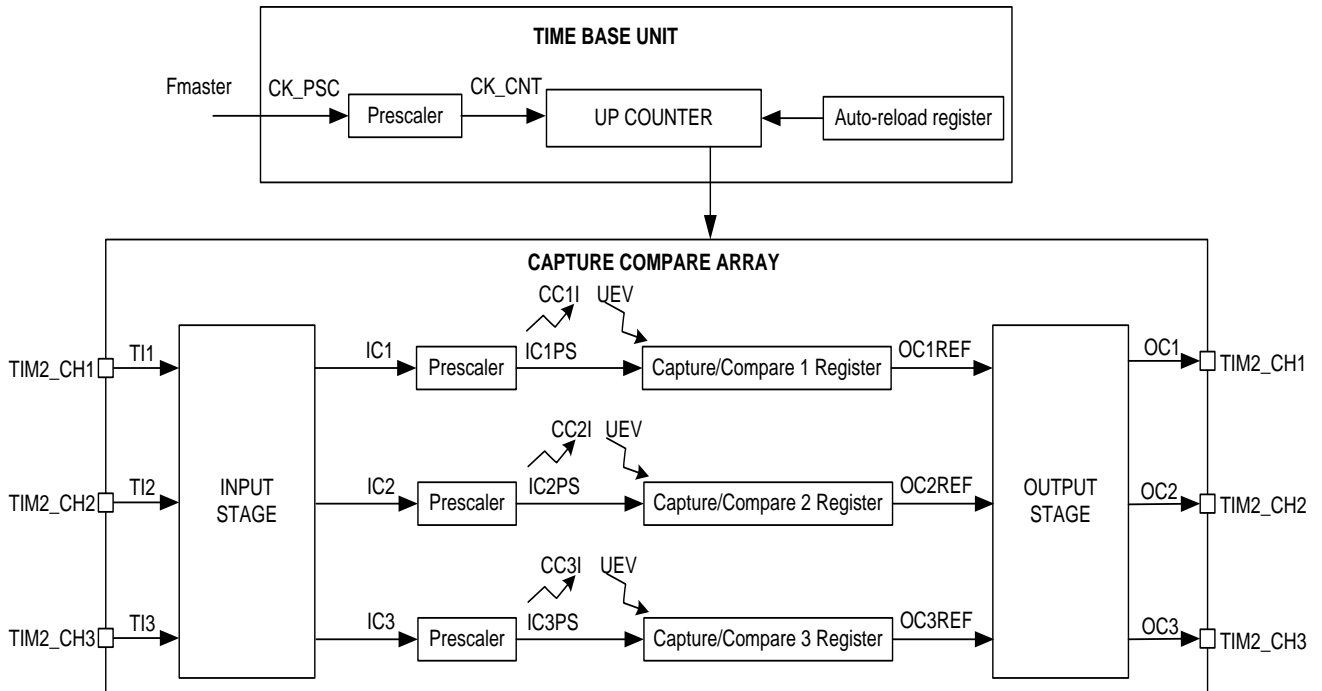


Figure 7-35 TIM2 Block Diagram

TIM2 features:

- 16-bit up counter supporting auto-reload;
- 4-bit programmable prescaler;
- 3 channels with selectable polarity support:
 - ✓ Input capture
 - ✓ Output compare
 - ✓ Same cycle, independent duty cycle PWM channels
 - ✓ One-Pulse mode
- Interrupt events: Update event, input capture, output comparison.

7.3.1. Summary of Timer2 Related Registers

Name	Addr.	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
PCKEN	0x9A	—	—	UARTEN	—	TIM4EN	TIM2EN	TIM1EN	ADCEN	0000 0000
CKOCON	0x95	SYSON	CCORDY	DTYSEL		CCOSEL[2:0]			CCOEN	0010 0000
TIM2CR1	0x30C	T2ARPE	—	—	—	T2OPM	T2URS	T2UDIS	T2CEN	0--- 000
TIM2IER	0x30D	—	—	—	—	T2CC3IE	T2CC2IE	T2CC1IE	T2UIE	--- 0000
TIM2SR1	0x30E	—	—	—	—	T2CC3IF	T2CC2IF	T2CC1IF	T2UIF	--- 0000
TIM2SR2	0x30F	—	—	—	—	T2CC3OF	T2CC2OF	T2CC1OF	—	--- 000-
TIM2EGR	0x310	—	—	—	—	T2CC3G	T2CC2G	T2CC1G	T2UG	--- 0000
TIM2CCMR1 (output mode)	0x311	—	T2OC1M[2:0]			T2OC1PE	—	T2CC1S[1:0]		-000 0-00
TIM2CCMR1 (input mode)		T2IC1F[3:0]				T2IC1PSC[1:0]		T2CC1S[1:0]		0000 0000
TIM2CCMR2 (output mode)	0x312	—	T2OC2M[2:0]			T2OC2PE	—	T2CC2S[1:0]		-000 0-00
TIM2CCMR2 (input mode)		T2IC2F[3:0]				T2IC2PSC[1:0]		T2CC2S[1:0]		0000 0000
TIM2CCMR3 (output mode)	0x313	—	T2OC3M[2:0]			OC3PE	—	T2CC3S[1:0]		-000 0-00
TIM2_CCMR3 (input mode)		T2IC3F[3:0]				T2IC3PSC[1:0]		T2CC3S[1:0]		0000 0000
TIM2CCER1	0x314	—	—	T2CC2P	T2CC2E	—	—	T2CC1P	T2CC1E	--00 --00
TIM2CCER2	0x315	—	—	—	—	—	—	T2CC3P	T2CC3E	--- --00
TIM2CNTRH	0x316	T2CNT[15:8]								0000 0000
TIM2CNTRL	0x317	T2CNT[7:0]								0000 0000
TIM2PSCR	0x318	—	—	—	—	T2PSC[3:0]				--- 0000
TIM2ARRH	0x319	T2ARR[15:8]								1111 1111
TIM2ARRL	0x31A	T2ARR[7:0]								1111 1111
TIM2CCR1H	0x31B	T2CCR1[15:8]								0000 0000
TIM2CCR1L	0x31C	T2CCR1[7:0]								0000 0000
TIM2CCR2H	0x31D	T2CCR2[15:8]								0000 0000
TIM2CCR2L	0x31E	T2CCR2[7:0]								0000 0000
TIM2CCR3H	0x29E	T2CCR3[15:8]								0000 0000
TIM2CCR3L	0x29F	T2CCR3[7:0]								0000 0000

Table 7-23 Summary of Timer2 Related registers (Reserved bits must remain as the reset value and cannot be changed)

Name	Status		Register	Addr.	Reset
T2CNT	TIM2 Count Value	MSB	TIM2CNTRH[7:0]	0x316	RW-0000 0000
		LSB	TIM2CNTRL[7:0]	0x317	RW-0000 0000
T2PSC	TIM2 Prescaler		TIM2PSCR[3:0]	0x318	RW-0000
T2ARR	Auto-reload Register for Counting Cycles (Preload value)	MSB	TIM2ARRH[7:0]	0x319	RW-1111 1111
	Note: When the value is 0, the counter does not work;	LSB	TIM2ARRL[7:0]	0x31A	RW-1111 1111
T2CCR1	Input Capture Mode: Last Capture Event (IC1)	MSB	TIM2CCR1H[7:0]	0x31B	RO-0000 0000
	Captured count value	LSB	TIM2CCR1L[7:0]	0x31C	RO-0000 0000
	Output Compare Mode: output compare value of TIM2_CH1	MSB	TIM2CCR1H[7:0]	0x31B	RW-0000 0000
	(Preloaded value)	LSB	TIM2CCR1L[7:0]	0x31C	RW-0000 0000
T2CCR2	Input Capture Mode: Last Capture Event (IC2)	MSB	TIM2CCR2H[7:0]	0x31D	RO-0000 0000
	Captured count value	LSB	TIM2CCR2L[7:0]	0x31E	RO-0000 0000
	Output Compare Mode: output compare value of TIM2_CH2	MSB	TIM2CCR2H[7:0]	0x31D	RW-0000 0000
	(Preloaded value)	LSB	TIM2CCR2L[7:0]	0x31E	RW-0000 0000
T2CCR3	Input Capture Mode: Last Capture Event (IC3)	MSB	TIM2CCR3H[7:0]	0x29E	RO-0000 0000
	Captured count value	LSB	TIM2CCR3L[7:0]	0x29F	RO-0000 0000
	Output compare mode: output compare value of TIM2_CH3	MSB	TIM2CCR3H[7:0]	0x29E	RW-0000 0000
	(Preloaded value)	LSB	TIM2CCR3L[7:0]	0x29F	RW-0000 0000

Table 7-24 Timer2 Period Related Registers

Name	Status	Register	Addr.	Reset
TIM2EN	<u>TIM2 Clock</u> 1 = Enable 0 = <u>Disable</u>	PCKEN[2]	0x9A	RW-0
SYSON	<u>In SLEEP mode, the system clock controls</u> 1 = Enable 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
T2CKSRC	<u>Timer2 Clock Source (Fmaster)</u> 000 = Sysclk 100 = 2x (XT or EC) (*) 001 = HIRC 101 = LIRC 010 = XT or EC (*) 110 = LP or EC (*) 011 = 2x HIRC 111 = 2x (LP or EC) (*) (*) FOSC should be configured in LP/XT/EC mode accordingly, otherwise the oscillator will not run.	TCKSRC[6:4]	0x31F	RW-000
DTYSEL	<u>TIM1/TIM2 Multiplier Clock Duty Cycle Adjustment Bit</u> 00 = 2ns delay 10 = <u>4ns delay</u> 01 = 3ns delay 11 = 7ns delay	CKOCON[5:4]	0x95	RW-10
T2ARPE	<u>Auto-Preload of Count Cycles</u> 1 = Enable (The T2ARR preload value is loaded when the update event arrives) 0 = <u>Disable</u> (T2ARR is loaded immediately)	TIM2CR1[7]	0x30C	RW-0
T2OPM	<u>One-Pulse mode</u> 1 = Enable (when the next update event comes, T2CEN is automatically cleared and the counter is stopped) 0 = <u>Disable</u> (counters do not stop when the update event occurs)	TIM2CR1[3]		RW-0
T2URS	<u>When T2UDIS=0, update event source</u> 1 / 0 = Counter Overflows	TIM2CR1[2]		RW-0
T2UDIS	<u>Generate Update Event Control</u> 1 = Disable 0 = <u>Allow</u>	TIM2CR1[1]		RW-0
T2CEN	<u>TIM2 Counter</u> 1 = Enable 0 = <u>Disable</u>	TIM2CR1[0]		RW-0

Table 7-25 Timer2 Related User Control Register

Name	Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	Bit0	Reset
TIM2CCMR1	0x311	T2IC1F[3:0]				T2IC1PSC[1:0]		T2CC1S[1:0]		RW-0000 0000
TIM2CCMR2	0x312	T2IC2F[3:0]				T2IC2PSC[1:0]		T2CC2S[1:0]		RW-0000 0000
TIM2CCMR3	0x313	T2IC3F[3:0]				T2IC3PSC[1:0]		T2CC3S[1:0]		RW-0000 0000

Name	Status	Register	Addr.	Reset	
T2ICxF	<u>Sampling Frequency and Digital Filter Length of Channel x Input capture</u>		TIM2CCMRx[7:4] x = 1, 2, 3	RW-0000	
	Value	Sampling frequency (f _{SAMPLING})			Digital Filter Length (N)
	0000	Fmaster/2			0
	0001	Fmaster			2
	0010	Fmaster			4
	0011	Fmaster			8
	0100	Fmaster / 2			6
	0101	Fmaster / 2			8
	0110	Fmaster / 4			6
	0111	Fmaster / 4			8
	1000	Fmaster / 8			6
	1001	Fmaster / 8			8
	1010	Fmaster / 16			5
	1011	Fmaster / 16			6
	1100	Fmaster / 16			8
1101	Fmaster / 32	5			
1110	Fmaster / 32	6			
1111	Fmaster / 32	8			
T2ICxPSC	<u>Channel x Input Capture Prescaler (several events trigger a capture)</u> 00 = 1 01 = 2 10 = 4 11 = 8 Note: When T2CCxE = 0, the prescaler is reset to 00	TIM2CCMRx[3:2]	0x311/ 0x312/ 0x313	RW-00	
T2CC1S ⁸	<u>Channel1 Mode</u> 00 = <u>Output</u> 01 = Input, the input pin is mapped	TIM2CCMR1[1:0]	0x311	RW-00	

⁸ Writable only when channel x is disabled (ie T2CCxE = 0), x = 1, 2, 3.

Name	Status	Register	Addr.	Reset
	<u>Selection</u> to TI1FP1 10 = Input, the input pin is mapped to TI2FP1 11 = Reserved			
T2CC2S ⁹	Channel2 Mode Selection 00 = <u>Output</u> 01 = Input, the input pin is mapped to TI2FP2 10 = Input, the input pin is mapped to TI1FP2 11 = Reserved	TIM2CCMR2[1:0]	0x312	RW-00
T2CC3S ⁹	Channel3 Mode Selection 00 = <u>Output</u> 01 = Input, the input pin is mapped to TI3FP3 1x = Reserved	TIM2CCMR3[1:0]	0x313	RW-00

Table 7-26 TIM2CCMRx as Input Configuration Register

⁹ Writable only when channel x is disabled (ie T2CCxE = 0), x = 1, 2, 3.

Name	Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	Bit0	Reset
TIM2CCMR1	0x311	-	T2OC1M[2:0]		T2OC1PE	-	T2CC1S[1:0]		RW--000 0-00	
TIM2CCMR2	0x312	-	T2OC2M[2:0]		T2OC2PE	-	T2CC2S[1:0]		RW--000 0-00	
TIM2CCMR3	0x313	-	T2OC3M[2:0]		T2OC3PE	-	T2CC3S[1:0]		RW--000 0-00	

T2OCxM	Channel x Output Compare Mode		Level of Reference Signal OCxREF
000	Frozen (No comparison)		<u>Remain unchanged</u>
001	When T2CNT = CCRx_SHAD		1
010	When T2CNT = CCRx_SHAD		0
011	When T2CNT = CCRx_SHAD		Level Reversal
100	Forced inactive		0
101	Forced active		1
110	PWM1 mode	T2CNT < CCRx_SHAD	1
		T2CNT > CCRx_SHAD	0
111	PWM2 mode	T2CNT < CCRx_SHAD	0
		T2CNT > CCRx_SHAD	1

Note: The output reference signal OCxREF is active at high level, which together with the polarity selection T2CCxP determines the actual output value of OCx;

Table 7-27 T2OCxM Configured in Output Compare Mode

Name	Status	Register	Addr.	Reset
T2OCxPE	<u>Auto-preload of Channel x Output Compare value</u> 1 = Enabled (T2CCRx preload value is loaded when the update event arrives) 0 = <u>Disabled</u> (T2CCRx is loaded immediately)	TIM2CCMRx[3] x = 1, 2, 3	0x311/ 0x312/ 0x313	RW-0
T2CC1S ¹⁰	<u>Channel 1 Mode Selection</u> 00 = <u>Output</u> 01 = Input, the input pin is mapped to TI1FP1 10 = Input, the input pin is mapped to TI2FP1 11 = Reserved	TIM2CCMR1[1:0]	0x311	RW-00
T2CC2S ¹⁰	Channel 2 Mode Selection 00 = <u>Output</u> 01 = Input, the input pin is mapped to TI2FP2 10 = Input, the input pin is mapped to TI1FP2 11 = Reserved	TIM2CCMR2[1:0]	0x312	RW-00
T2CC3S ¹⁰	Channel 3 Mode Selection 00 = <u>Output</u> 01 = Input, the input pin is mapped to TI3FP3 1x = Reserved	TIM2CCMR3[1:0]	0x313	RW-00

Table 7-28 TIM2CCMRx as Output Configuration Register

Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Addr	Reset
TIM2CCER1	-	-	T2CC2P	T2CC2E	-	-	T2CC1P	T2CC1E	0x314	RW---00 --00
TIM2CCER2	-	-	-	-	-	-	T2CC3P	T2CC3E	0x315	RW----- --00

Name	Function	Input Capture Mode (T2CCxS = 01/10)	Output Compare Mode (T2CCxS = 00)
T2CCxP	Channel x Input/Output Polarity Selection	1 = Capture occurs on falling edge or low level of TIxF 0 = <u>Capture occurs on rising edge or high level of TIxF</u>	1 = OCx is active at low level 0 = <u>OCx is active at high level</u>
T2CCxE	Channel x Input/Output Pin Function	1 = Enable the input capture function of the pin 0 = <u>Disable</u>	1 = Enable the OCx output function of the pin 0 = <u>Disable</u>

Note: The channel output level is determined by the values of the T2OISx and T2CCxE bits;

Table 7-29 Timer2 Channel Output and Polarity Selection

¹⁰ Writable only when channel x is disabled (ie T2CCxE = 0), x = 1, 2, 3 .

Name	Status	Register	Addr.	Reset
TIM2_CH1	<u>Channel1 Pin Remapping</u> 1 = PB0 0 = PA5	AFP0[4]	0x19F	RW-0
TIM2_CH3	<u>Channel3 Pin Remapping</u> 1 = PA3 0 = PB5	AFP0[3]		RW-0

Table 7-30 Timer2 Channel Pin Remapping

Name	Status	Register	Addr.	Reset
GIE	<u>Global Interrupt</u> 1 = Enable (PEIE, T2CCxIE, T2CCxG, T2UIE apply) 0 = <u>Global Shutdown</u> (Wake-Up not affected)	INTCON[7]	Bank First address+0x0B	RW-0
PEIE	<u>Peripheral Interrupt Enable</u> 1 = Enabled (for T2CCxIE, T2CCxG, T2UIE) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0
T2CC3IE	<u>Channel 3 Capture/Compare Interrupt</u>	TIM2IER[3]	0x30D	RW-0
T2CC2IE	<u>Channel 2 Capture/Compare Interrupt</u>	TIM2IER[2]		RW-0
T2CC1IE	<u>Channel 1 Capture/Compare Interrupt</u>	TIM2IER[1]		RW-0
T2CC3G ¹¹	<u>Channel 3 Capture/Compare Software Interrupt</u>	TIM2EGR[3]	0x310	WO-0
T2CC2G ¹¹	<u>Channel 2 Capture/Compare Software Interrupt</u>	TIM2EGR[2]		WO-0
T2CC1G ¹¹	<u>Channel 1 Capture/Compare Software Interrupt</u>	TIM2EGR[1]		WO-0
T2CC3IF ¹²	<u>Channel x Capture/Compare Interrupt Flag</u> • Output Mode:	TIM2SR1[3]	0x30E	R_W1C-0

¹¹ Set to 1 by software, auto clear by hardware.

¹² Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to only use the STR and MOVWI instructions for Write operations, rather than the BSR or IOR instructions.

Name	Status	Register	Addr.	Reset
T2CC2IF ¹²	1 = The value of T2CNT and T2CCRx match 0 = <u>Mismatch</u>	TIM2SR1[2]		R_W1C-0
T2CC1IF ¹²	• Input Mode: 1 = Count value has been captured to T2CCRx (auto clear when T2CCRx is read) 0 = <u>No capture occurred</u>	TIM2SR1[1]		R_W1C-0
T2CC3OF ¹²	<u>Channel x Recapture Interrupt Flag</u> 1 = Recapture occurs (T2CCxIF is already set when the counter value is captured into the T2CCRx register) 0 = <u>No recapture</u>	TIM2SR2[3]	0x30F	R_W1C-0
T2CC2OF ¹²		TIM2SR2[2]		R_W1C-0
T2CC1OF ¹²		TIM2SR2[1]		R_W1C-0
T2UIE	<u>Allow Update Interrupt</u> 1 = Enable 0 = <u>Disable</u>	TIM2IER[0]	0x30D	RW-0
T2UG ¹¹	<u>Allow Update Software Interruption</u> 0 = <u>Disable</u>	TIM2EGR[0]	0x310	WO-0
T2UIF ¹²	<u>Update Event Interrupt Flag</u> 1 = An update event occurs 0 = <u>No update event</u>	TIM2SR1[0]	0x30E	R_W1C-0

Table 7-31 Timer2 Interrupt Enable and Status Bits

7.3.2. Counting basic units

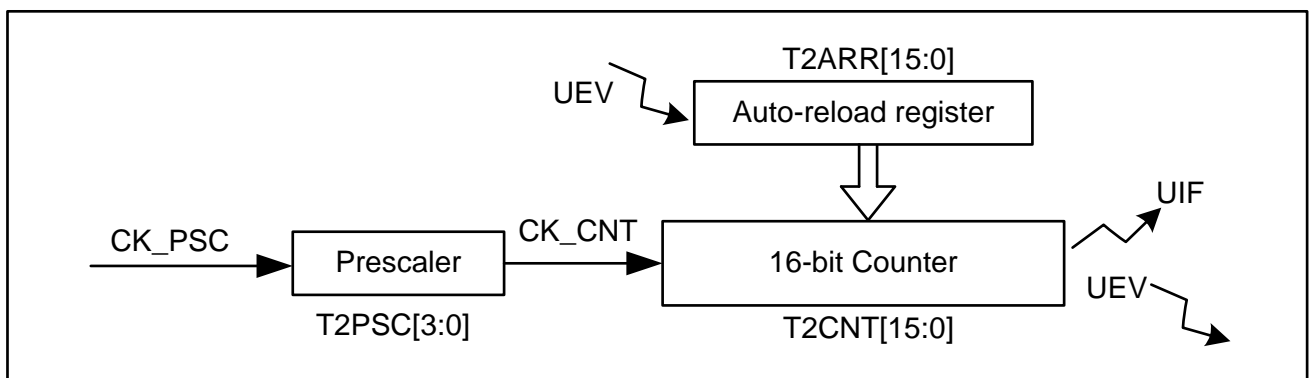


Figure 7-36 Counting basic units

TIM2 basic units:

- 16-bit upward counter
- 4-bit prescaler

- 16-bit auto-reload register

Up count mode: the counter starts counting up from 0, an overflow event occurs when T2CNT = T2ARR, and then the counter starts counting from 0 again.

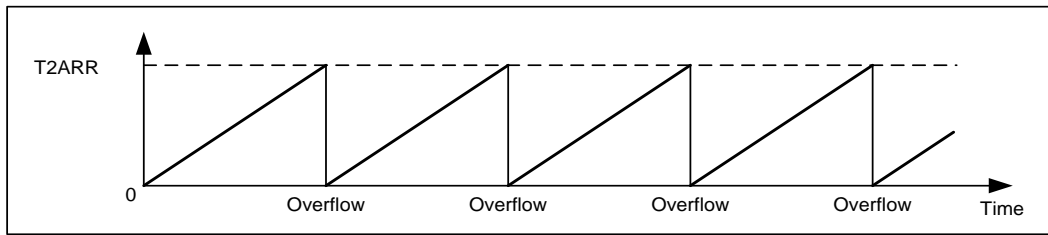


Figure 7-37 Up count mode

The prescaler, output comparison, and auto-reload register consist of preload registers and shadow registers, respectively.

	Prescaler	Output Compare value	Auto-reload Register
Preload Enable	Enabled by default when T2CEN = 1	T2OCxPE	T2ARPE
Preload Register	T2PSC[3:0]	T2CCRx[15:0]	T2ARR[15:0]

Table 7-32 Registers with Preload Function

Six optional clock sources for the TIM2 prescaled clock (CK_PSC) (see T2CKSRC) are as follows:

- Sysclk
- 1x or 2x HIRC
- LIRC
- 1x or 2x external clock (Only valid when FOSC is configured in LP, XT or EC mode accordingly)

The 4-bit prescaler can divide the prescaler clock (CK_PSC) by 1 to 32768 to generate the count clock (CK_CNT).

Frequency division Equation : $f_{CK_CNT} = f_{CK_PSC} / 2^{(PSCR[3:0])}$; (PSCR is the value of prescaler shadow register)

Note:

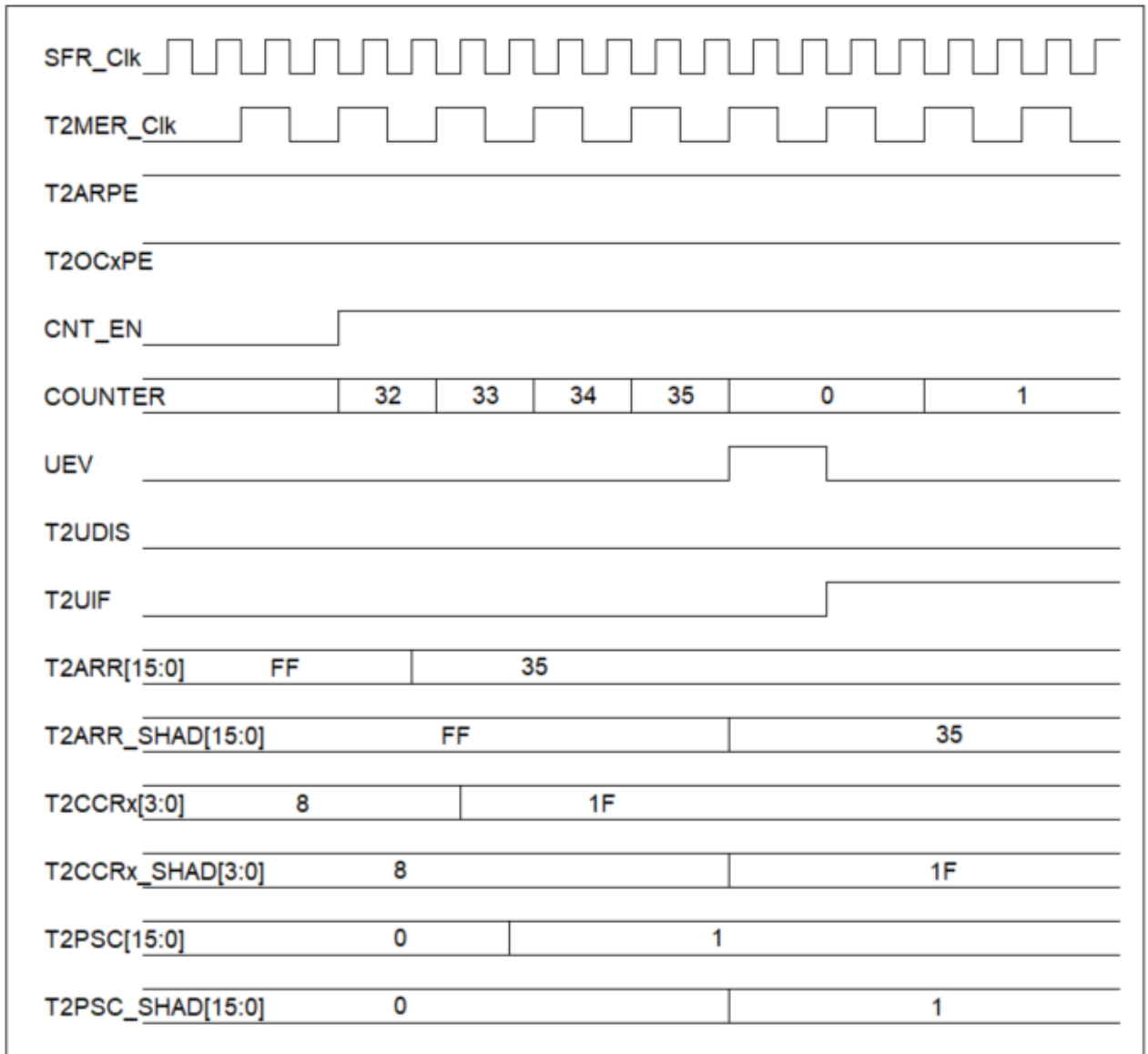
1. It is recommended to read and write the counter value T2CNT[15:0] when the counter is stopped (T2CEN = 0) to avoid errors.
2. It is necessary to configure the cycle, output compare value and other registers first, and configure the prescaler register before enabling the counter (T2CEN = 1).

When T2UDIS = 0, it is allowed to generate update events. The update event source (see "T1URS") is as follows:

- Counter overflows

When an update event occurs, the update event flag T2UIF is set, and whether to trigger an Interrupt and /or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE and

T2UIE).



• **Figure 7-38** Update timing diagram of the pre-load registers under the update event

Additionally, depending on the configuration, the update event can trigger the following:

1. Related to prescaler, output comparison, and auto-reload registers:
 - (1) When the counter is enabled ($T2CEN = 1$) and its corresponding preload is enabled ($T2OCxPE / T2ARPE = 1$), its shadow register will be updated to the preload value when an update event occurs, as shown in [Figure 7-38](#) ;
 - (2) When the counter is disabled ($T2CEN = 0$), or its corresponding preload is disabled ($T2OCxPE / T2ARPE = 0$), its shadow register will be updated directly with the preload value;
2. In one-pulse mode, when an update event occurs, the counter will be automatically turned off ($T2CEN = 0$), and stop counting;

7.3.3. Capture / Compare Channel

The CH1~3 PORTS of TIM2 can be configured as input capture or output compare function (see T2CCxS of the multiplexing register TIM2CCMRx) .

The T2CCRx registers consist of a preload register and a shadow register. Read and write process only operate on preload registers.

- In input capture mode:

T2CCRx[15:0] is a read-only register. When a capture event occurs, the captured counter value is written to the shadow register and then copied to the T2CCRx preload register.

When reading the T2CCRx[15:0] register, the MSB must be read first, followed by the LSB. When the MSB are read, the preload register is frozen, and then the correct LSB can be read. After reading the LSB, the preload register can be updated to the latest captured value.

- In output compare mode:

T2CCRx[15:0] is a readable and writable register. During a write operation the T2CCRx preload register value is copied into the shadow register (see [Section 7.3.2](#)), then the content of shadow register is compared with the counter. The value read during a read operation comes from the preload register.

7.3.3.1. Input Capture Mode

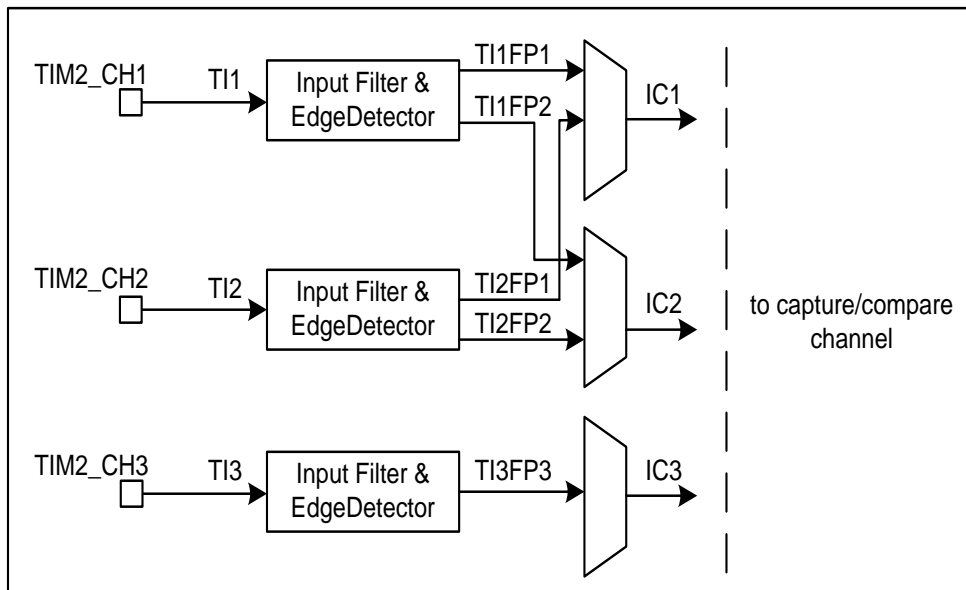


Figure 7-39 Input Capture Channel Block Diagram

In the input capture mode, when an input capture event occurs in channel x, the current count value will be captured into the T2CCRx [15:0] register, and the input capture flag T2CCxIF is set. If the input capture event occurs again when T2CCxIF remains 1, the re-capture flag T2CCxOF will be set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE and T2CCxIE). In addition, the input capture software interrupt bit T2CCxG can be enabled to trigger an interrupt.

The input capture sources of each channel of TIM2 (see T2CCxS) are as follows:

T2CCxS	Channel 1	Channel 2	Channel 4
01	TI1FP1	TI2FP2	TI3FP3
10	TI2FP1	TI1FP2	-

Table 7-33 Input Capture Source for each Channel

Signal name	Detailed description
TIM2_CH1/2/3	I/O inputs corresponding to Channel 1/2/3/4
IC1/2/3	Capture source via selected channel
TI1FP1	Input capture signal corresponding to I/O of channel 1, as one of the capture sources of channel 1
TI1FP2	Input capture signal corresponding to I/O of channel 1, as one of the capture sources of channel 2
TI2FP2	Input capture signal corresponding to I/O of channel 2, as one of the capture sources of channel 2
TI2FP1	Input capture signal corresponding to I/O of channel 2, as one of the capture sources of channel 1
TI3FP3	Input capture signal corresponding to I/O of channel 3, as one of the capture sources of channel 3

Table 7-34 Input Capture Signal Description

Please refer to TIM1 ([Section 7.2.4.1](#)) for configuration steps of input capture channels.

7.3.3.2. Output Compare Mode

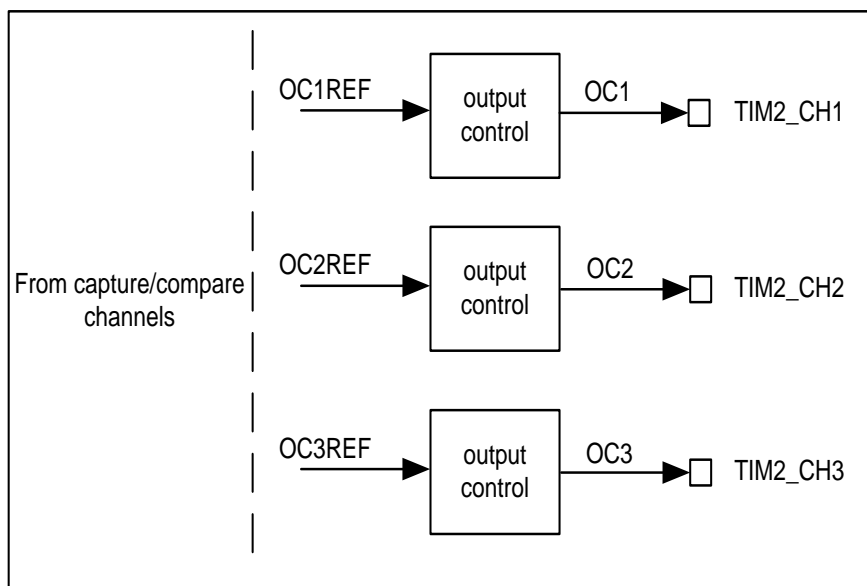


Figure 7-40 Output Compare Channel Block Diagram

The output compare module generates the output reference signal OCxREF (active high) by comparing the count value (T2CNT) with the comparison value (shadow register CCRx_SHAD), and then outputs the waveform to the port after polarity selection and output control (T2CCxE).

The reference signal OCxREF can be configured into 8 output modes via T2OCxM[2:0] (see [Table 7-27](#)):

1. Frozen mode (T2OCxM = 000) : OCxREF value remains unchanged.
2. Active level on match (T2OCxM = 001) : When T2CNT = CCRx_SHAD, OCxREF = 1.
3. Inactive level on match (T2OCxM = 010) : OCxREF = 0 when T2CNT = CCRx_SHAD.
4. Toggle on Match (T2OCxM = 011) : When T2CNT = CCRx_SHAD, the OCxREF value is flipped.
5. Forced inactive (T2OCxM = 100): OCxREF is always 0.
6. Forced active (T2OCxM = 101): OCxREF is always 1.
7. PWM1 mode (T2OCxM = 110):
 - a) When T2CNT < CCRx_SHAD, OCxREF = 1; OCxREF = 0 when T2CNT > CCRx_SHAD.
8. PWM2 mode (T2OCxM = 111):
 - a) When T2CNT < CCRx_SHAD, OCxREF = 0 ; when T2CNT > CCRx_SHAD, OCxREF = 1.

When T2CNT matches CCRx_SHAD, the output compare flag T1CCx2F is set. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding enable control bits (GIE, PEIE, T2CCxIE). In addition, the output compare software interrupt bit T2CCxG, can be enabled to trigger an interrupt.

Please refer to TIM1 ([section 7.2.4.2](#)) for configuration steps for output compare channels.

PWM Mode – PWM1/PWM2 cycle is determined by T2ARR and duty cycle is determined by T2CCRx.

Equation 7-3 $PWM1/2 \text{ Cycle} = (T2ARR+1) * T_{CK_CNT}$

Equation 7-4 $PWM1/2 \text{ Duty Cycle} = T2CCRx \div (T2ARR+1)$

TIM1_CH1/2/3 channels can independently enable the output PWM signal, and the output signal polarity is optional (see T2CCxP) .

One-Pulse Mode – In One-Pulse Mode (T2OPM = 1), when the next update event occurs, the hardware automatically turns off the counter enable (T2CEN = 0) and the counter stops counting.

To generate a correct pulse, the counter initial value (T2CNT) must be different from the compare value (T2CCRx). That is, before starting counting, the following configurations must be met:

- Up-count mode: T2CNT < T2CCRx ≤ T2ARR

7.4. Basic TIMER4

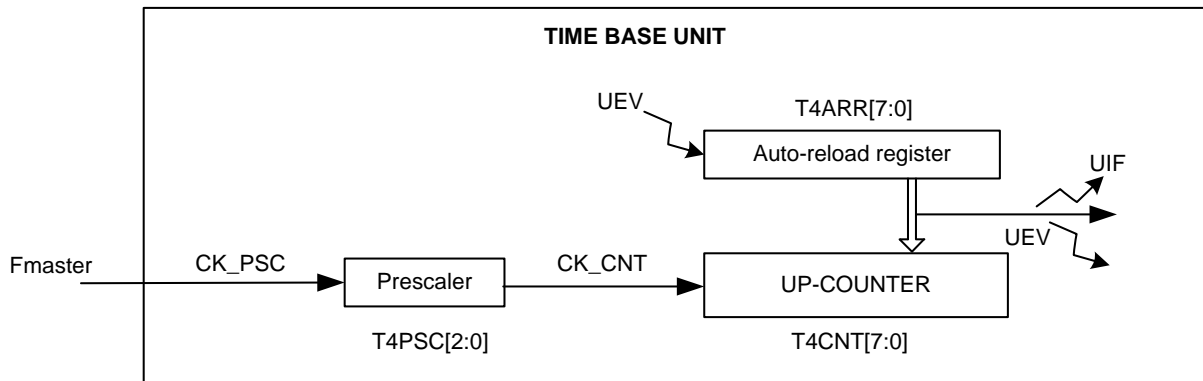


Figure 7-41 TIM4 Block Diagram

TIM4 is an 8-bit up-counter: the counter starts counting up from 0. An overflow event occurs when T4CNT = T4ARR, and then the counter starts counting from 0 again. The auto-reload register T4ARR consists of a preload register and a shadow register.

The optional 4 clock sources for the TIM4 prescaled clock (CK_PSC) (see T4CKSRC) are as follows:

- Sysclk
- HIRC
- External clock LP/XT (Only valid when FOSC is configured in LP or XT mode accordingly)

The 3-bit prescaler divides the prescaler clock (CK_PSC) by 1 ~ 128 to generate the counter clock (CK_CNT).

Frequency division Equation : $f_{CK_CNT} = f_{CK_PSC} / 2^{(PSCR[2:0])}$; (PSCR is the value of prescaler shadow register)

Note:

1. It is recommended that the counter value T4CNT[7:0] be read or written when the counter is stopped (T4CEN = 0) to avoid errors.
2. The cycle and other registers need to be configured first, and the prescaler register must be configured before the counter is enabled (T4CEN = 1).

When T4UDIS = 0, the update event is allowed to be generated and the update event source (see "T1URS") is as follows:

- Counter overflow
- Set T4UG by software or counter overflow

When an update event occurs, the update event flag T4UIF is set, and whether to trigger an Interrupt and /or wake up from SLEEP depends on the corresponding enable control bits(GIE, PEIE and T4UIE).

Additionally, depending on the configuration, the update event can trigger the following conditions:

1. Related to the prescaler registers:

- (1) When the counter is enabled (T4CEN = 1) and its corresponding preload is enabled (T4ARPE = 1), its shadow register will be updated to the preload value when an update event occurs.
 - (2) When the counter is disabled (T4CEN = 0), or its corresponding preload is disabled (T4ARPE = 0), its shadow register will be updated directly with the preload value.
2. One-Pulse mode, when an update event occurs, the counter will be automatically turned off (T4CEN = 0), and stop counting.

7.4.1. Summary of Timer4 Related Registers

Name	Status	Register	Addr.	Reset
TIM4EN	<u>TIM4 Clock</u> 1 = Enable 0 = <u>Disable</u>	PCKEN[3]	0x9A	RW-0
SYSON	In SLEEP mode, the system clock controls 1 = Enable 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
T4ARPE	<u>Auto-preload of Counting Cycles</u> 1 = Enabled (The T4ARR preload value is loaded when the update event occurs) 0 = Disabled (T4ARR is loaded immediately)	TIM4CR1[7]	0x111	RW-0
T4CKS	<u>Timer4 Clock Source</u> 00 = <u>Sysclk</u> 10 = LP ^(*) 01 = HIRC 11 = XT ^(*) ^(*) FOSC needs to be configured in LP/XT mode accordingly, otherwise the oscillator will not run.	TIM4CR1[5:4]		RW-00
T4OPM	<u>One-Pulse Mode</u> 1 = Enable (when the next update event comes, T4CEN auto-clear and the counter stops) 0 = Disable (counter does not stop when update event occurs)	TIM4CR1[3]		RW-0
T4URS	<u>When T4UDIS = 0, Update Event Interrupt Source</u> 1 = Counter overflows 0 = Set T4UG by software or the counter overflows	TIM4CR1[2]		RW-0
T4UDIS	<u>Update Event Generation Control</u> 1 = Disable 0 = Enable	TIM4CR1[1]		RW-0
T4CEN	TIM4 Counter 1 = Enable 0 = <u>Disable</u>	TIM4CR1[0]	RW-0	
T4PSC	<u>Timer4 Prescaler</u>	TIM4PSCR[2:0]	0x116	RW-000

Name	Status	Register	Addr.	Reset
	000 = 1 100 = 16 001 = 2 101 = 32 010 = 4 110 = 64 011 = 8 111 =128			
T4CNT	Timer4 Count Value	TIM4CNTR[7:0]	0x115	RW-0000 0000
T4ARR	<u>Auto-reload register for counting cycles (preload value)</u> Note: When this value is 0, the counter does not work	TIM4ARR[7:0]	0x117	RW-1111 1111

Table 7-35 Timer4 Related User Control Registers

Name	Status	Register	Addr.	Reset
GIE	<u>Global Interrupt</u> 1 = Enable (PEIE, T4UIE, T4UG apply) 0 = <u>Global Shutdown</u> (Wake-Up is not affected)	INTCON[7]	Bank First address	RW-0
PEIE	Peripheral Interrupt Enable 1 = Enable (T4UIE, T4UG applicable) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]	+0x0B	RW-0
T4UIE	Allow Update Interrupt	TIM4IER[0]	0x112	RW-0
T4UG ¹³	Allow Update Software Interruption	TIM4EGR[0]	0x114	WO-0
T4UIF ¹⁴	Update Event Interrupt Flag	TIM4SR[0]	0x113	R_W1C-0

Table 7-36 Timer4 Interrupt Enable and Status Bits

Name	Addr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
PCKEN	0x9A	—	—	UARTEN	—	TIM4EN	TIM2EN	TIM1EN	ADCEN	--0- 0000
CKOCON	0x95	SYSON	CCORDY	DTYSEL		CCOSEL[2:0]			CCOEN	0010 0000
TIM4CR1	0x111	T4ARPE	—	T4CKS[1:0]		T4OPM	T4URS	T4UDIS	T4CEN	0-00 0000
TIM4IER	0x112	—	—	—	—	—	—	—	T4UIE	---- ---0
TIM4SR	0x113	—	—	—	—	—	—	—	T4UIF	---- ---0
TIM4EGR	0x114	—	—	—	—	—	—	—	T4UG	---- ---0
TIM4CNTR	0x115	T4CNT[7:0]								0000 0000
TIM4PSCR	0x116	—	—	—	—	—	T4PSC[2:0]		---- -000	
TIM4ARR	0x117	T4ARR[7:0]								1111 1111

Table 7-37 Summary of Timer4 Related Registers (Reserved bits must remain as the reset value and cannot be changed)

¹³ Set to 1 by software, auto clear by hardware.

¹⁴ Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to use only STR and MOVWI instructions for Write operation, not BSR or IOR instructions.

8. SLEEP (POWER-DOWN)

During SLEEP Instruction Clock is inactive and instructions execution is halted. Most modules are powered down to conserve power. As listed in **Table 8-1**, FT61E14x can selectively turn on individual modules in SLEEP according to actual needs so that functions such as LVR, LVD, WDT, Timers, PWM, ADC and USART, can remain active during SLEEP without instruction interventions. Some modules can configure automatic power down upon SLEEP to save the need to turn them off by instructions.

	Configuration conditions of each module in SLEEP	
	RUN	Auto-Shutdown
Instruction Clock	(always power down)	Yes
LVR (Configure the LVREN)	Enabled or Instruction controlled (SLVREN=1)	Enabled except in SLEEP
LVD	LVDEN = 1	No
WDT	WDTE or SWDTEN	No
TIMER1	SYSON = 1 & TIM1EN = 1 & T1CEN = 1	SYSON = 0
TIMER2	SYSON = 1 & TIM2EN = 1 & T2CEN = 1	SYSON = 0
TIMER4	SYSON = 1 & TIM4EN = 1 & T4CEN = 1	SYSON = 0
Clock Output	SYSON = 1 & CCOEN = 1	SYSON = 0
ADC	SYSON = 1 & ADCEN = 1 & ADON = 1	Yes : SYSON = 0 & ADCS ≠ x11 No: ADCS = x11
USART	SYSON = 1 & UARTEN = 1 & TXEN / RXEN = 1	SYSON = 0
PWM	(follows Timer1 or Timer2)	
HIRC/LIRC/EC/LP/XT	(follow the states of the used peripherals)	
I/O	(maintain their states before SLEEP unless PWM, clock output, or other peripherals SLEEP enabled)	

Table 8-1 All modules except Instruction Clock can remain active in SLEEP if so desired

8.1. Enter SLEEP

The CPU enters SLEEP by executing the SLEEP instruction. When enter SLEEP:

1. If WDT is enabled, it will clear its Prescaler (if assigned) and counter, and start counting.
2. Time Out Flag (/TF) = 1
3. Power Down Flag (/PF) = 0
4. Clock sources
 - When SYSON = 0, the instruction clock is automatically turned off;
 - When SYSON = 1, the instruction clock keeps active, as do the corresponding peripherals and their selected clock sources (HIRC, LIRC, EC, LP or XT) that enable the module system clock (see PCKEN);
 - When SYSON = 1, the clock source selected for the clock output (see CCOSEL) will keep active and the clock output will continue;
5. I/O PORTS

- When SYSON = 1 & TIMxEN = 1 & TxEN = 1, PWM output continue if Timers are active in SLEEP. When SYSON = 0, Timers auto-shutdown and the PWM output will maintain its state before entering SLEEP.
- When SYSON = 1, if the system clock and module function of ADC or USART are enabled at the same time, the module function can keep active. When SYSON = 0, ADC (ADCS ≠ x 11) or USART will automatically shut down, except for ADC clock source selection LIRC (ADCS = x 11) .
- For other Digital Outputs, they will maintain the state before SLEEP (High-z state, “0” or “1”)

For more information about how peripherals work in SLEEP please see the corresponding Sections.

Note :

1. If an interrupt occurs before the SLEEP instruction is executed (the interrupt flag is set and its interrupt is enabled, but the Global Interrupt GIE is disabled), the SLEEP instruction will be executed as a NOP and will not enter sleep mode.
2. Due to the synchronization delay, after clearing the interrupt flag to 0, at least two instructions need to be waited before the SLEEP instruction can be executed, otherwise it will not enter the sleep mode.

8.2. Wake Up from SLEEP

There are 2 general principles to wake up from sleep:

- Time based, in which the CPU wakes up after a certain amount of time. LIRC is the clock choice for keeping time as it has lower power consumption than HIRC.
- Events based that triggers POR, System-Reset, Wake-up without Interrupt, and Interrupts, such as LVD, ADC, EEPROM write completion, and external pin interrupt.

The situations that wake up from SLEEP as follows:

1. Watchdog Timer Wake-up if enabled (see [Section 7.1](#) Watchdog Timer).
2. Full-Reset and System-Reset
 - POR Full-Reset (cannot be disabled)
 - External System-Reset by the /MCLR (if enable)
 - LVR Reset (if enable)
3. Enabled Interrupts (Disabling the “Global Interrupt Enable” will not stop Wake-up). Please see [Section 9](#) Interrupts.

Notes:

1. Waking up from SLEEP will also clear WDT.
2. SLEEP must be followed by NOP

When wakes up from SLEEP in a non interrupt mode (that is, "interrupt service program" is not executed), such as WDT wake up, or attempted Interrupts with Global Interrupt Enable (GIE) disabled, the next instruction will be executed.

When using the Interrupt method to wake up from SLEEP, the next instruction will be executed before

calling the Interrupt Service Routine. To avoid duplicate execution NOP must follow SLEEP.

SLEEP

NOP // Wake-Up by Interrupt

9. INTERRUPTS

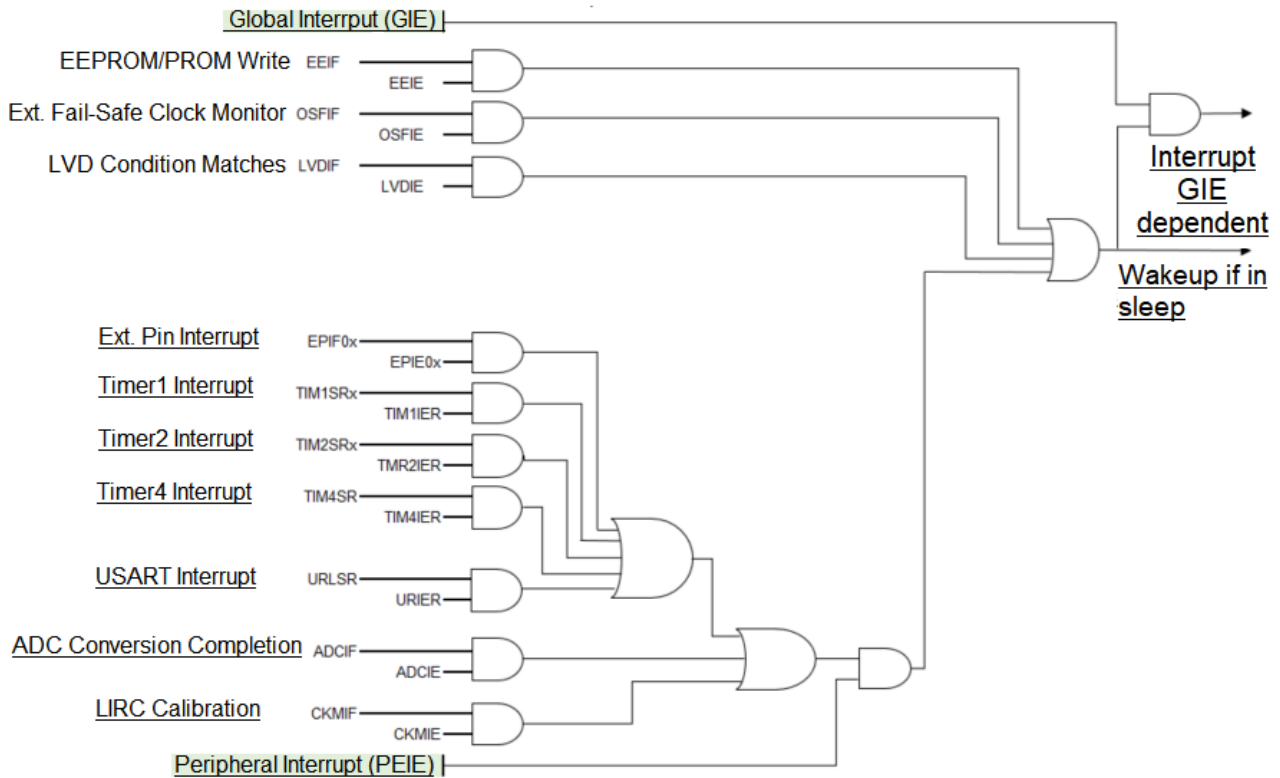


Figure 9-1 Interrupt Block Diagram

The CPU supports 10 interrupt sources, divided into 2 groups:

1) Non-peripheral interrupts

- DATA EEPROM/PROM Write Completion
- Fail-Safe Clock Monitor
- LVD Condition Matches

2) Peripheral interrupt

- External pin interrupt
- Timer1 interrupt
- Timer2 interrupt
- Timer4 interrupt
- USART interrupt
- LIRC and HIRC Cross Calibration Completion
- ADC Conversion Completion

WDT overflows, unlike other Timers, will not result in an Interrupt. For other interrupts besides external I/O interrupts please see the corresponding Sections.

When an interrupt occurs, the PC jumps to and executes the “Interrupt Service Routine (ISR)”. There are multiple levels of Interrupt Disable/Enable.

- Each interrupt source has a local interrupt enable: EEIE, LVDIE, OSFIE, CKMIE, ADCIE, TIM1IER, TIM2IER, TIM4IER, URIER.
- At the same time, there are up to 8 external pin interrupt inputs, sharing a PORT interrupt enable: EPIE0x (External PORTx Interrupt Enable).
- The Peripheral interrupts has a total interrupt enable: PEIE (Peripheral Interrupt Enable).
- All controls above, if disabled, will not execute a Wake-Up from SLEEP.
- All interrupts are controlled by a global enable: GIE (Global Interrupt Enable). This enable differs from the others by allowing a Wake-Up from SLEEP even when disabled.
- Disabling the interrupts does not affect the setting of the interrupt flags.

The following sequences occur upon an Interrupt:

- Auto set “GIE = 0”, disabling further interrupts.
- The return address is pushed onto the stack and the PC (program counter) is loaded with 0x0004.
- Jump to the “Interrupt Service Routine” 3 – 5 instruction cycles after the interrupt.
- “Return from Interrupt (RETI)” instruction exits ISR. Prior to RETI must clear the interrupt flag currently being processed.
- At the completion of the ISR, the PC returns to the address before the interrupt, which in SLEEP, is the address immediate after SLEEP.
- Auto set GIE = 1 upon executing RETI, enabling future interrupts.

Note: Only the returned PC address is saved on the stack during an interrupt, and other important registers [e.g., W, STATUS (except /TO and /PD), BSREG, FSR, PCLATH] are automatically saved in the corresponding shadow registers (R/W, see bank 31) . These register values are automatically restored from the shadow registers when the interrupt service routine is exited. Users desiring to have other registers saved must use instructions to write them into temporary registers explicitly. Use the last 16 bytes of SRAM for temporary storages as they are common to all banks and do not require bank swithing.

9.1. Summary of Interrupt Related Registers

Name	Addr.	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset (RW)
INTCON	0x0B	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
PIE1	0x91	-	-	-	-	-	-	CKMIE	ADCIE	---- --00
PIR1	0x11	-	-	-	-	-	-	CKMIF	ADCIF	---- --00
TIM1IER	0x215	T1BIE	T1TIE	-	T1CC4IE	T1CC3IE	T1CC2IE	T1CC1IE	T1UIE	00-0 0000
TIM1SR1	0x216	T1BIF	T1TIF	-	T1CC4IF	T1CC3IF	T1CC2IF	T1CC1IF	T1UIF	00-0 0000
TIM1SR2	0x217	-	-	-	T1CC4OF	T1CC3OF	T1CC2OF	T1CC1OF	-	---0 000-
TIM1EGR	0x218	-	-	-	T1CC4G	T1CC3G	T1CC2G	T1CC1G	-	---0 000-
TIM2IER	0x30D	-	-	-	-	T2CC3IE	T2CC2IE	T2CC1IE	T2UIE	---- 0000
TIM2SR1	0x30E	-	-	-	-	T2CC3IF	T2CC2IF	T2CC1IF	T2UIF	---- 0000
TIM2SR2	0x30F	-	-	-	-	T2CC3OF	T2CC2OF	T2CC1OF	-	---- 000-
TIM2EGR	0x310	-	-	-	-	T2CC3G	T2CC2G	T2CC1G	T2UG	---- 0000
TIM4IER	0x112	-	-	-	-	-	-	-	T4UIE	---- ---0
TIM4SR	0x113	-	-	-	-	-	-	-	T4UIF	---- ---0
TIM4EGR	0x114	-	-	-	-	-	-	-	T4UG	---- ---0
URIER	0x48E	-	-	TCEN	-	IDELE	RXSE	URTE	URRXNE	--0- 0000
URLSR	0x492	ADDRF	IDLEF	TXEF	BKF	FEF	PEF	OVERF	RXNEF	0010 0000
URTC	0x49C	-	-	-	-	-	-	-	TCF	---- ---1
EPIE0	0x94	External Interrupt Control Register								0000 0000
EPIF0	0x14	External Interrupt Flag Register								0000 0000
TRISA	0x8C	PORTA Data Direction Register								1111 1111
TRISB	0x8D	PORTB Data Direction Register								1111 1111
TRISC	0x8E	PORTC Data Direction Register								1111 1111
EPS0	0x118	External Interrupt EINT3 ~ 0 Pin Select Register								0000 0000
EPS1	0x119	External interrupt EINT7 ~ 4 pin select register								0000 0000

Table 9-1 Interrupt Related Register Addresses and Default

Name	Status	Register	Addr.	Reset	
GIE	<u>Global Interrupt</u> 1 = Enable (PEIE, each interrupt independent enable bit apply) 0 = <u>Global Shutdown</u> (Wake-Up not affected)	INTCON[7]	Bank First address+0x0B	RW-0	
PEIE	<u>Peripheral Interrupt Enable</u> 1 = Enable (Each interrupt independent enable bit apply) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0	
EEIE	EEPROM/PROM Write Completion interrupt	INTCON[5]		1 = Enable 0 = <u>Disable</u> (no Wake-Up)	RW-0
LVDIE	LVD interrupt	INTCON[4]			RW-0
OSFIE	External Oscillator Failed Interrupt	INTCON[3]			RW-0
EEIF ¹	EEPROM/PROM Write Completion interrupt Flag	INTCON[2]		1 = Yes (latched) 0 = <u>No</u>	R_W1C-0
LVDIF ¹	LVD Interrupt Flag	INTCON[1]			R_W1C-0
OSFIF ¹	External Oscillator Failed Interrupt Flag	INTCON[0]	R_W1C-0		

Table 9-2 INTCON register

Name	Status	Register	Addr.	Reset
CKMIE	LIRC and HIRC Cross Calibration Completion interrupt	PIE1[1]	0x91	RW-0
ADCIE	ADC Conversion Completion Interrupt	PIE1[0]		RW-0
CKMIF ¹	LIRC and HIRC Cross Calibration Completion Flag	PIR1[1]	0x11	R_W1C-0
ADCIF ¹	ADC Conversion Completion Flag	PIR1[0]		R_W1C-0

Table 9-3 PIE1 and PIR1 registers

¹ Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to only execute the STR and MOVWI instructions for write operations, rather than the BSR or IOR instructions .

Name	Status	Register	Addr.	Reset
T1BIE	Timer1 Break Interrupt	TIM1IER[7]	0x215	RW-0
T1TIE	Timer1 Trigger Interrupt	TIM1IER[6]		RW-0
T1COMIE	Timer1 Commutation (COM) Interrupt	TIM1IER[5]		RW-0
T1CC4IE	Timer1 Capture/Compare Channel4 Interrupt	TIM1IER[4]		RW-0
T1CC3IE	Timer1 Capture/Compare Channel3 Interrupt	TIM1IER[3]		RW-0
T1CC2IE	Timer1 Capture/Compare Channel2 Interrupt	TIM1IER[2]		RW-0
T1CC1IE	Timer1 Capture/Compare Channel1 Interrupt	TIM1IER[1]		RW-0
T1UIE	Timer1 Update Event Interrupt	TIM1IER[0]		RW-0
T1BG ²	Timer1 Break Software Interrupt	TIM1EGR[7]	0x218	WO-0
T1TG ²	Timer1 Trigger Software Interrupt	TIM1EGR[6]		WO-0
T1COMG ²	Timer1 Commutation (COM) Software Interrupt	TIM1EGR[5]		WO-0
T1CC4G ²	Timer1 Capture/Compare Channel4 Software Interrupt	TIM1EGR[4]		WO-0
T1CC3G ²	Timer1 Capture/Compare Channel3 Software Interrupt	TIM1EGR[3]		WO-0
T1CC2G ²	Timer1 Capture/Compare Channel2 Software Interrupt	TIM1EGR[2]		WO-0
T1CC1G ²	Timer1 Capture/Compare Channel1 Software Interrupt	TIM1EGR[1]		WO-0
T1UG ²	Timer1 Update Event Software Interrupt	TIM1EGR[0]		WO-0
T2CC3IE	Timer2 Capture/Compare Channel3 Interrupt	TIM2IER[3]	0x30D	RW-0
T2CC2IE	Timer2 Capture/Compare Channel2 Interrupt	TIM2IER[2]		RW-0
T2CC1IE	Timer2 Capture/Compare Channel1 Interrupt	TIM2IER[1]		RW-0
T2UIE	Timer2 Update Event Interrupt	TIM2IER[0]		RW-0
T2CC3G ²	Timer2 Capture/Compare Channel3 Software Interrupt	TIM2EGR[3]	0x310	WO-0
T2CC2G ²	Timer2 Capture/Compare Channel2 Software Interrupt	TIM2EGR[2]		WO-0
T2CC1G ²	Timer2 Capture/Compare Channel1 Software Interrupt	TIM2EGR[1]		WO-0
T2UG ²	Timer2 Update Event Software Interrupt	TIM2EGR[0]		WO-0
T4UIE	Timer4 Update Event Interrupt	TIM4IER[0]	0x112	RW-0
T4UG ²	Timer4 Update Event Software Interrupt	TIM4EGR[0]	0x114	WO-0

1 = Enable
 0 = Disable
 (no Wake-Up)

Table 9-4 TIMx INTCON Register

² Set to 1 by software, auto clear by hardware.

Name	Status	Register	Addr.	Reset
T1BIF ³	Timer1 Break Interrupt Flag	TIM1SR1[7]	0x216	R_W1C-0
T1TIF ³	Timer1 Trigger event Interrupt Flag	TIM1SR1[6]		R_W1C-0
T1COMIF ³	Timer1 Commutation (COM) Interrupt Flag	TIM1SR1[5]		R_W1C-0
T1CC4IF ³	Timer1 Capture/Compare Channel4 Interrupt Flag	TIM1SR1[4]		R_W1C-0
T1CC3IF ³	Timer1 Capture/Compare Channel3 Interrupt Flag	TIM1SR1[3]		R_W1C-0
T1CC2IF ³	Timer1 Capture/Compare Channel2 Interrupt Flag	TIM1SR1[2]		R_W1C-0
T1CC1IF ³	Timer1 Capture/Compare Channel1 Interrupt Flag	TIM1SR1[1]		R_W1C-0
T1UIF ³	Timer1 Update Event Interrupt Flag	TIM1SR1[0]		R_W1C-0
T1CC4OF ³	Timer1 Capture/Compare Channel4 Repeated Capture Interrupt Flag	TIM1SR2[4]	0x217	R_W1C-0
T1CC3OF ³	Timer1 Capture/Compare Channel3 Repeated capture Interrupt Flag	TIM1SR2[3]		R_W1C-0
T1CC2OF ³	Timer1 Capture/Compare Channel2 Repeated Capture Interrupt Flag	TIM1SR2[2]		R_W1C-0
T1CC1OF ³	Timer1 Capture/Compare Channel1 Repeated Capture Interrupt Flag	TIM1SR2[1]		R_W1C-0
T2CC3IF ³	Timer2 Capture/Compare Channel3 Interrupt Flag	TIM2SR1[3]	0x30E	R_W1C-0
T2CC2IF ³	Timer2 Capture/Compare Channel2 Interrupt Flag	TIM2SR1[2]		R_W1C-0
T2CC1IF ³	Timer2 Capture/Compare Channel1 Interrupt Flag	TIM2SR1[1]		R_W1C-0
T2UIF ³	Timer2 Update Event Interrupt Flag	TIM2SR1[0]		R_W1C-0
T2CC3OF ³	Timer2 Capture/Compare Channel3 Repeated Capture Interrupt Flag	TIM2SR2[3]	0x30F	R_W1C-0
T2CC2OF ³	Timer2 Capture/Compare Channel2 Repeated Capture Interrupt Flag	TIM2SR2[2]		R_W1C-0
T2CC1OF ³	Timer2 Capture/Compare Channel1 Repeated Capture Interrupt Flag	TIM2SR2[1]		R_W1C-0
T4UIF ³	Timer4 Update Event Interrupt Flag	TIM4SR[0]	0x113	R_W1C-0

1 = Yes (latched)
0 = No

Table 9-5 TIMx Interrupt Flag Register

³ Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to execute only STR and MOVWI instructions for write operations, rather than BSR or IOR instructions.

Name	Status	Register	Addr.	Reset
URTE	Send BUF as empty interrupt 1 = Enable 0 = <u>Disable</u>	URIER[1]	0x48E	RW-0
TXEF	Send BUF status 1 = Empty 0 = <u>Not empty</u> Note: Write DATAL(8bit) / DATAH(9bit) to clear	URLSR[5]	0x492	RO-1
URRXNE	Receive BUF as not empty interrupt 1 = Enable 0 = <u>Disable</u>	URIER[0]	0x48E	RW-0
RXNEF	Receive BUF status 1 = Not empty 0 = <u>Empty, or cleared</u> Note: Read DATAL(8bit) / DATAH(9bit) to clear	URLSR[0]	0x492	RO-0
TCEN	Send Completion Interrupt 1 = Enable 0 = <u>Disable</u>	URIER[5]	0x48E	RW-0
TCF	Transmission Completion Flag 1 = Completed 0 = <u>Not completed</u> Note: Write 1 to clear, or write DATAL(8bit) / DATAH(9bit) to clear	URTC[0]	0x49C	R_W1C-1
IDELE	Idle frame interrupt 1 = Enable 0 = <u>Disable</u>	URIER[3]	0x48E	RW-0
IDLEF ⁴	Idle frame detected Flag 1 = Detected 0 = <u>Not detected</u>	URLSR[6]	0x492	RW0-0
RXSE ⁵	Receive status interrupt 1 = Enable 0 = <u>Disable</u> <u>Conditions for receiving status Interrupt:</u> BKF = 1 FEF = 1 PEF = 1 OVERF = 1	URIER[2]	0x48E	RW-0
BKF ⁴	Received broken frame Flag 1 = Received 0 = <u>Not received, or cleared</u>	URLSR[4]	0x492	RW0-0
FEF ⁴	Received frame error Flag 1 = Error 0 = <u>Correct, or cleared</u>	URLSR[3]	0x492	RW0-0

⁴ Write '0' to clear, and writing '1' has no effect on the bit value.

⁵USART received broken frame, framing error, parity error, receive overflow error status.

Name	Status	Register	Addr.	Reset
PEF ⁴	Received Parity error Flag 1 = Error 0 = <u>Correct, or cleared</u>	URLSR[2]	0x492	RW-0
OVERF ⁶	Receive BUF overflow Flag 1 = Overflow 0 = <u>Normal, or cleared</u>	URLSR[1]	0x492	RW-0
WAKE	Mute Mode wake-up Selection 1 = Address matches 0 = <u>IDLE frame</u>	URMCR[2]	0x491	RW-0
ADDRF	Mute Mode Address Matching Flag 1 = Match 0 = <u>Mismatch</u>	URLSR[7]	0x492	RO-0

Table 9-6 USART Interrupt Enable and Status Bits

Name	Status	Register	Addr.	Reset
EINT0	00 = <u>PA0</u> 01 = PB0 10 = PC0 11 = Reserved	EPS0[1:0]	0x118	RW-00
EINT1	00 = <u>PA1</u> 01 = PB1 10 = PC1 11 = Reserved	EPS0[3:2]		RW-00
EINT2	00 = <u>PA2</u> 01 = PB2 1x = Reserved	EPS0[5:4]		RW-00
EINT3	00 = <u>PA3</u> 01 = PB3 1x = Reserved	EPS0[7:6]		RW-00
EINT4	00 = <u>PA4</u> 01 = PB4 1x = Reserved	EPS1[1:0]	0x119	RW-00
EINT5	00 = <u>PA5</u> 01 = PB5 1x = Reserved	EPS1[3:2]		RW-00
EINT6	00 = <u>PA6</u> 01 = PB6 1x = Reserved	EPS1[5:4]		RW-00
EINT7	00 = <u>PA7</u> 01 = PB7 1x = Reserved	EPS1[7:6]		RW-00

Table 9-7 External Interrupt Pin Selection Register

Name	Status	Register	Addr.	Reset
ITYPE0[1:0]	PORTx.0	ITYPE0[1:0]	0x11E	RW-00
ITYPE0[3:2]	PORTx.1	ITYPE0[3:2]		RW-00
ITYPE0[5:4]	PORTx.2	ITYPE0[5:4]		RW-00
ITYPE0[7:6]	PORTx.3	ITYPE0[7:6]		RW-00
ITYPE1[1:0]	PORTx.4	ITYPE1[1:0]	0x11F	RW-00
ITYPE1[3:2]	PORTx.5	ITYPE1[3:2]		RW-00
ITYPE1[5:4]	PORTy.6	ITYPE1[5:4]		RW-00
ITYPE1[7:6]	PORTy.7	ITYPE1[7:6]		RW-00

Table 9-8 External Interrupt Trigger Type Register (x = A, B, C; y = A, B)

⁶ Write '0' to clear, and writing '1' has no effect on the bit value.

Name	Status	Register	Addr.	Reset
EPIE0x	External Pin Interrupt 1 = Enable 0 = <u>Disable</u>	EPIE0[7:0]	0x94	RW-00000000
EPIF0x ⁷	External Pin Interrupt Flag 1 = Yes (latched) 0 = <u>No</u>	EPIF0[7:0]	0x14	R_W1C-00000000

Table 9-9 External Interrupt Enable and Flag Registers

9.2. External pin interrupt

All I/O support external pin interrupts, and there are up to 8 external pin interrupt inputs (refer to EINT0~7), and the I/O need to be set as input (TRISA/B/C[x] = 1, and ANSELA[x] = 0), the trigger source can be selected as rising edge, falling edge, double edge and low level (refer to ITYPE x) .

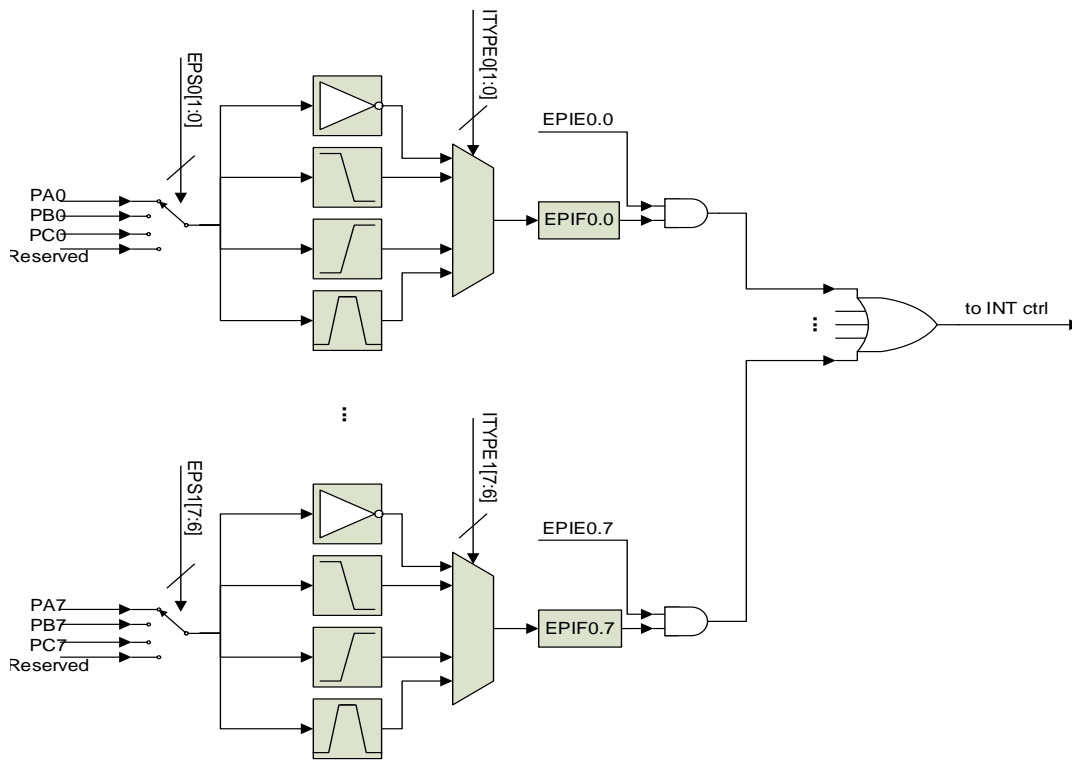


Figure 9-2 External Interrupt Block Diagram

⁷ Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to only execute the STR and MOVWI instructions for write operations, rather than the BSR or IOR instructions .

10. DATA EEPROM AND PROGRAM PROM

Both the non-volatile DATA EEPROM memory array and the program memory PROM integrated on the FT61E14x are R/W accessible by instruction, with "CFGS" and "EEP GD" selecting the accessed memory area. 128 x 8-bit DATA EEPROM and 4k x 14-bit (128 page x 32 words) program PROM are independent of each other.

The DATA EEPROM memory array has a typical R/W endurance of 100,000 cycles. The address range is 0x00 ~ 0x7F. One byte (8-bit) is written or read at a time. There is no page mode. The program PROM memory array has a typical R/W endurance of 100,000 cycles. The address range is 0x0000 ~ 0x0FFF. One word (14-bit) is written or erased at a time.

DATA EEPROM erase/program is self-timed by hardware, without software queries and saving limited code space. This allows WRITE to take place in the background while the CPU runs unhindered, or even to enter SLEEP. But when the PROM is erased/programmed, the CPU will stop executing instructions.

For DATA EEPROM, READ takes one instruction clock cycle, whereas WRITE takes $T_{\text{WRITE-EEPROM}}$ (3 ~ 5 ms). And for PROM, ERASE takes $T_{\text{ERASE-PROM}}$ (0.75 ~ 1.25 ms), whereas WRITE takes $T_{\text{WRITE-PROM}}$ (0.75 ~ 1.25 ms). There is an on-chip charge pump so there is no need to supply an external high voltage for erase and program the EEPROM and PROM array. Before programming, DATA EEPROM can be configured to auto-erase, but PROM must be erased by software. The corresponding interrupt flag EEIF will be set when the EPROM write operation is complete.

There is no sequential READ or sequential WRITE. The address must be updated every time.

Any voltage above V_{POR} , which can be as low as 1.5V from die to die and at high temperature, will be able to run the CPU at 8MHz, 2T. The $V_{\text{DD-WRITE}}$ for writing DATA EEPROM and PROM is higher. For DATA EEPROM, the minimum $V_{\text{DD-WRITE}}$ is 1.9V and 2.2V for Temperature Grade 2 and Grade 1 respectively. For PROM, the minimum $V_{\text{DD-WRITE}}$ is 2.7V. Reading DATA EEPROM and PROM does not have this minimum voltage limit (see $V_{\text{DD-READ}}$).

10.1. Summary of DATA EEPROM and PROM Related Registers

Name	Status	Register	Addr.	Reset
GIE	Global Interrupt 1 = Enable (PEIE, EEIE apply) 0 = <u>Global Shutdown</u> (Wake-Up not affected)	INTCON[7]	Bank First address+0x0B	RW-0
PEIE	Peripheral Interrupt Enable 1 = Enabled (EEIE applies) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0
EEIE	EEPROM/PROM Write Completion Interrupt 1 = Enable 0 = <u>Disable</u> (no Wake-Up)	INTCON[5]		RW-0
EEIF ¹	EEPROM/PROM Write Completion Flag 1 = Yes (latched) 0 = <u>No</u>	INTCON[2]		R_W1C-0

Table 10-1 EEPROM and PROM Interrupt Enable and Status Bits

Name	Status	Register	Addr.	Reset
SYSON	<u>In SLEEP mode, the Sysclk controls</u> 1 = Enable 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
EEADR ²	When EEPGD = 0	DATA EEPROM address	0x191	RW-0000 0000
	When EEPGD = 1	LSB(8 bits) of PROM address		
		MSB(4 bits) of the PROM address	EEADRH[3:0]	0x192
EEDAT ²	when EEPGD = 0	DATA EEPROM data	0x193	RW-xxxx xxxx
	When EEPGD = 1	LSB(8 bits) of PROM data		
		MSB(6 bits) of PROM data	EEDATH[5:0]	0x194
EEPGD	when CFGS = 0 1 = Access to PROM 0 = <u>Access to DATA EEPROM</u>	EECON1[7]	0x195	RW-0
CFGS	1 = Access configuration register (READ access) 0 = <u>Access to PROM or DATA EEPROM</u>	EECON1[6]		RW-0

¹ Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to only use the STR and MOVWI instructions for write operations, rather than the BSR or IOR instructions .

² During a write cycle (see T_{WRITE-EEPROM} and T_{WRITE-PROM}), this register is not writable.

Name	Status	Register	Addr.	Reset
FREE	<u>ROM operation performed by the next WR command</u> 1 = Erase (cleared by hardware after erasing is finished) 0 = <u>Write</u> Note: Valid only when CFGS = 0 and EEPGD = 1	EECON1[4]		RW-0
WRERR	<u>PROM/DATA EEPROM Erase / Write Error Flag</u> 1 = Premature terminated (any reset except POR) 0 = Finished	EECON1[3]		RW-x
WREN	<u>PROM/DATA EEPROM Write Enable</u> 1 = Enable 0 = <u>Disable</u>	EECON1[2]		RW-0
WR	<u>PROM/DATA EEPROM Write Control</u> 1 = Start a write or writing (After set to 1, wait at least 1 Sysclk to Read back, and it will reset to 0 automatically after the Write is finished) 0 = Finished	EECON1[1]		RW1-0
RD	<u>PROM/DATA EEPROM Read Control bit</u> 1 = Yes (auto clear after 4 instruction cycles) 0 = <u>No</u>	EECON1[0]		RW1-0
EECON2	<u>PROM/DATA EEPROM Write Unlock Control</u> Write 0x55 before writing 0xAA for unlock operation, and then set WR to 1. Note: These Write operations must be completed in consecutive instruction cycles and cannot be interrupted.	EECON2[7:0]	0x196	WO-xxxx xxxx

Table 10-2 EEPROM and PROM Related Control Registers

10.2. DATA EEPROM

10.2.1. Writing DATA EEPROM

1. Set "GIE = 0";
2. If "GIE = 1", then repeat (1);
3. Write target address to EEADRL;
4. Write target data to EEDATL;
5. Set "CFGS = 0" and "EEPGD = 0" to select access to DATA EEPROM;
6. Set "WREN=1";

7. Write 0x55 and 0xAA sequentially to EECON2;
8. Set "WR = 1" to start writing;
9. After programming completed (see $T_{\text{WRITE-EEPROM}}$ for writing time), "WR = 0" set automatically by hardware;

Program Example:

```

BCR INTCON, GIE
NOP
NOP                               ; interrupt response delay is 2 NOP
BTSC INTCON, GIE
GOTO $-1

BANKSEL EEADRL
LDWI DATA_EE_ADDR
STR EEADRL                         ; write target address
LDWI DATA_EE_DATA
STR EEDATL                         ; write target data
BCR EECON1, CFGS
BCR EECON1, EEPGD                 ; select access to DATA EEPROM
BSR EECON1, WREN

LDWI 55H
STR EECON2                         ; write 0x55 to EECON2
LDWI AAH
STR EECON2                         ; write 0xAA to EECON2

BSR EECON1, WR                     ; start writing
BSR INTCON, GIE                    ; set GIE to 1
BCR EECON1, WREN                   ; disable write enable
BTSC EECON1, WR
LJUMP $-2
    
```

Note:

1. Data EEPROM Read while the array is still in programming will yield an incorrect result.
2. Before starting the write operation of the DATA EEPROM, it needs to be unlocked, i.e., write 0x55 and 0xAA sequentially to EECON2, and cannot be interrupted, so all interrupts need to be disabled before unlocking.
3. After GIE is cleared, wait for the interrupt response delay of 2 NOP, and then determine if GIE is cleared again.
4. WR is set to 1, wait at least one Sysclk (NOP or any other instructions) for software to read the correct WR value, otherwise it will read back to 0 (mistaken for writing finished).
5. After WR is set to 1, clearing WREN will not affect the current write cycle.

6. When the write of DATA EEPROM is finished, WREN needs to be cleared by software, this protection mechanism can prevent accidental write operations. In addition, the Power-up Timer PWRT (~ 64 ms) also prevents writing to the DATA EEPROM.

10.2.2. Read DATA EEPROM

1. Set "GIE = 0";
2. If "GIE = 1", then repeat (1);
3. Write target address to EEADRL;
4. Set "CFG5 = 0" and "EEPGD = 0" to select access to DATA EEPROM ;
5. Set "RD = 1" to start reading;
6. After waiting 4 instruction cycles, read the target data from EEDATL. The EEDATL register will hold this value until the next read or write operation. "RD" will auto clear by hardware;

The following is an example on how to read the DATA EEPROM:

```

BCR INTCON, GIE
NOP
NOP                               ; Interrupt response delay is 2 NOP
BTSC INTCON, GIE
GOTO $-1

BANKSEL EEADRL
LDWI DATA_EE_ADDR
STR EEADRL                         ; Write target address
BCR EECON1, CFG5
BCR EECON1, EEPGD                   ; Select access to DATA EEPROM
BSR EECON1, RD                      ; Start reading
NOP
NOP
NOP
NOP
LDR EEDATL, W                      ; Data is read by instruction
    
```

Note: The EEPROM can always be read by software regardless of the value of CPB.

10.3 Program PROM

The program address counter PC is 15 bits (0x0000 ~ 0x7FFF), supporting up to 32k address space. FT61E14x implements a 4k program PROM, divided into 128 page x 32 words (1 word = 14 bits), and the address range is 0x0000 ~ 0x0FFF. When the program address exceeds 0x0FFF, it will cause a rewind to 0x0000.

The software needs to erase the program PROM before executing the programming operation.

Note:

1. When BOOT (see FSECPB0) is set to sector encryption, the encrypted PROM sectors can only be read, not erased or written.

10.3.1 Erase Program PROM

The unit of software erasing PROM is 1 page (32 words).

1. Set "GIE = 0";
2. If "GIE = 1", then repeat (1);
3. Write target address to EEADRL and EEADRH;
4. Set "CFGS = 0" and "EEPGD = 1" to select access to PROM;
5. Set "FREE = 1" and "WREN = 1";
6. Write 0x55 and 0xAA sequentially to EECON2;
7. Set "WR = 1" to start erasing;
8. After the erasing is finished (the erasing time $T_{\text{ERASE-PROM}}$ is 0.75 ~ 1.25 ms), "FREE" will auto clear by hardware;

Program Example:

```

BCR INTCON, GIE
NOP
NOP ; Interrupt response delay is 2 NOP
BTSC INTCON, GIE
GOTO $-1

BANKSEL EEADRL
LDR ADDRL,W
STR EEADRL ; Write the LSB(8 bits) of the target address
LDR ADDRH,W
STR EEADRH ; Write the MSB(7 bits) of the target address
BCR EECON1, CFGS
BCR EECON1, EEPGD ; Welect access to PROM
BSR EECON1, FREE
BSR EECON1, WREN

LDWI 55H
STR EECON2 ; Write 0x55 to EECON2
LDWI AAH
STR EECON2 ; Write 0xAA to EECON2

BSR EECON1, WR ; Start erasing
NOP
NOP ; Wait for 2 NOP to set Erase
BCR EECON1, WREN ; Disable Write enable
BSR INTCON, GIE ; GIE set to 1

```


Note:

1. Before starting the erase operation of the PROM, it needs to be unlocked, that is, write 0x55 and 0xAA sequentially to EECON2, and cannot be interrupted, so all interrupts need to be disabled before unlocking.
2. After WR is set to 1, it takes 2 instruction cycles for the processor to set the erase operation, so 2 NOP instructions must follow immediately after the erase instruction.
3. During the erase cycle $T_{ERASE-PROM}$, the CPU will suspend execution of instructions and the clocks and peripherals will continue to run.
4. After the erase is complete, the program will continue to execute from the third instruction after the Erase instruction.

10.3.2 Writing Program PROM

The unit of software programming PROM is 1 word (14 bits), so 1 page needs to be programmed 32 times. Before programming, the corresponding address must be erased or unprogrammed.

1. Set "GIE = 0";
2. If "GIE = 1", then repeat (1);
3. Write target address to EEADRL and EEADRH;
4. Set "CFGS = 0" and "EPPGD = 1" to select access to PROM;
5. Set "FREE = 0" and "WREN = 1";
6. Write target data to EEDATL and EEDATH;
7. Write 0x55 and 0xAA sequentially to EECON2;
8. Set "WR = 1" to start writing;
9. After writing is finished (programming time $T_{WRITE-PROM}$ is 0.75 ~ 1.25 ms), "WR" will auto clear by hardware;
10. Repeat the above steps until all data is written;

Program Example (target data is loaded via indirect addressing):

```

BCR INTCON, GIE
NOP
NOP ; Interrupt response delay is 2 NOP
BTSC INTCON, GIE
GOTO $-1

BANKSEL EEADRL
LDR ADDRL,W
STR EEADRL ; Write the LSB (8 bits) of the target address
LDR ADDRH,W
STR EEADRH ; Write the MSB (7 bits) of the target address
LDWI LOW DATA_ADDR ; Load the LSB (8 bits) of the address of the target data
    
```

```

STR FSR0L
LDWI HIGH DATA_ADDR          ; Load the MSB (7 bits) of the address of the target data
STR FSR0H
BCR EECON1, CFGS
BCR EECON1, EEPGD             ; Select access to PROM
BCR EECON1, FREE
BSR EECON1, WREN

MOVIW FSR++
STR EEDATL                    ; Write the LSB (8 bits) of the target data
MOVIW FSR++
STR EEDATH                     ; Write MSB (6 bits) of target data

LDWI 55H
STR EECON2                    ; Write 0x55 to EECON2
LDWI AAH
STR EECON2                     ; Write 0xAA to EECON2

BSR EECON1, WR                ; Start writing
NOP
NOP                            ; Set the write operation to wait for 2 NOPs
BCR EECON1, WREN              ; Disable write enable
BSR INTCON, GIE               ; Set GIE to 1

```

Note:

1. When writing target data to EEDATL and EEDATH, it will be loaded into the 14-bit write latch. After finishing writing, the write latch will be reset to 0x3FFF.
2. Before starting the PROM write operation, it needs to be unlocked, i.e., write 0x55 and 0xAA to EECON2 sequentially and cannot be interrupted, so all interrupts need to be disabled before unlocking.
3. After WR is set to 1, it takes 2 instruction cycles for the processor to set the write operation, so 2 NOP instructions must be followed immediately after the write instruction.
4. During the cycle $T_{\text{WRITE-PROM}}$, the CPU will suspend instruction execution, and the clocks and peripherals will continue to run.
5. After finishing writing, the program will continue execution from the third instruction after the Write instruction.
6. When some PROM data needs to be changed, and other data of the current page needs to be preserved, modify it according to the following steps:
 - a) Load the starting address of the page to be modified;
 - b) Read all the data of the current page and save it to the RAM mapping area;
 - c) Modify the new data to be changed in the RAM mapping area;
 - d) Load the starting address of the page to be modified and erase the current page;
 - e) Write the data of the RAM mapped area to the current page one by one according to the programming steps;

10.3.3 Reading Program PROM

1. Set "GIE = 0";
2. If "GIE = 1", then repeat (1);
3. Write target address to EEADRL and EEADRH;
4. Set "CFGs = 0" and "EEPGD = 1" to select access to PROM;
5. Set "RD = 1" to start reading;
6. After waiting for 2 instruction cycles, the PROM data is written to the EEDATH:EEDATL register, thus 2 NOP instructions must follow immediately after the read instruction. RD" will auto clear by hardware. The EEDATH:EEDATL register will hold this value until the next Read or Write operation.

The following is an example on how to read the PROM:

```

BCR INTCON, GIE
NOP
NOP                               ; Interrupt response delay is 2 NOP
BTSC INTCON, GIE
GOTO $-1

BANKSEL EEADRL
LDWI PROG_ADDR_LO
STR EEADRL                         ; Write the LSB (8 bits) of the target address
LDWI PROG_ADDR_HI
STR EEADRH                         ; Write the MSB (7 bits) of the target address
BCR EECON1, CFGS
BSR EECON1, EEPGD                  ; Select access to PROM
BSR EECON1, RD                     ; Start reading
NOP
NOP                               ; Read wait for 2 NOPs
LDR EEDATL, W                      ; LSB(8 bits) of read data
STR PROG_DATA_LO
LDR EEDATH, W                      ; MSB (6 bits) of read data
STR PROG_DATA_HI

```

Notice:

1. The PROM can always be read by software regardless of the value of CPB.

10.4. Read BOOT Register UCFGx

When CFGS = 1, software can read the BOOT register area UCFGx (see [Section 14.1](#)). UCFGx and program PROM are independent of each other, and the address starts from 0x8000. For unimplemented units, read returns undefined.

11. 12-bit ADC

The ADC module can convert the analog input signal into a 12-bit digital signal and operate at different clock speeds with a 11-bit accuracy at clock speeds up to 2MHz (ie, 100 kHz sample rate, 10 μs/sample).

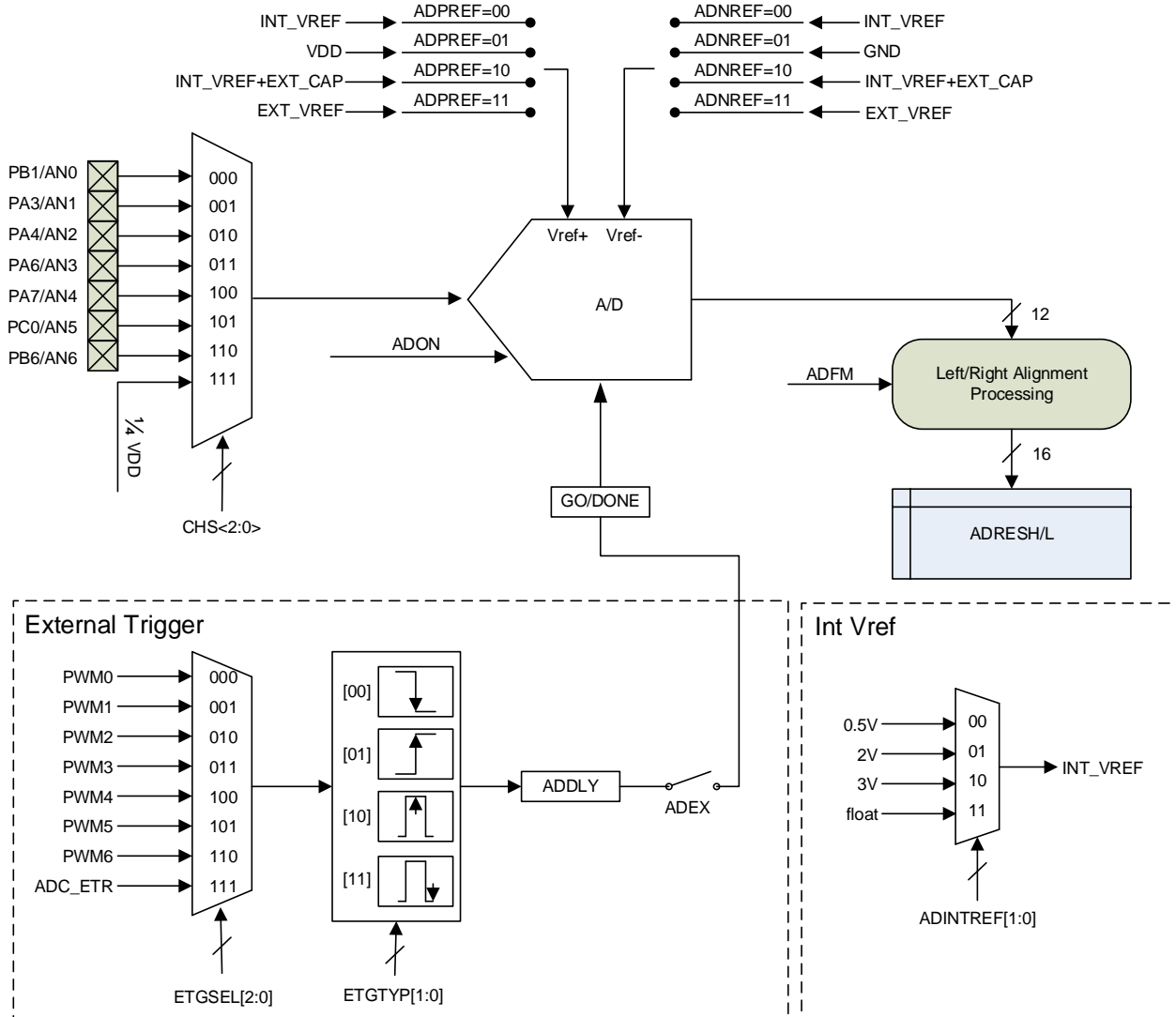


Figure 11-1 ADC Block Diagram

The analog input signal can be selected as one of seven I/O (ANx) channels or an internal channel (1/4VDD). ADC is triggered by instructions, I/O (PA4 / PB3) or PWM. A delay or leading edge blanking (LEB) can be added between trigger and ADC sampling.

When the ADC conversion is complete, the corresponding interrupt flag will be set, it can trigger an interrupt and/or Wake-up from SLEEP.

The ADC reference voltage ($V_{ADC-REF}$) can be selected as V_{DD} by instructions, one of three internal reference voltages (0.5V, 2V, 3V), or input the external reference voltage via I/O.

ADC does not require calibration. In addition, the ADC conversion process runs in the background, and the CPU can execute other instructions during the conversion.

If the ADC needs to keep active in SLEEP:

1. Set SYSON = 1 to keep Sysclk active;
2. When the ADC conversion clock source is LIRC, LIRC will keep active after entering SLEEP, regardless of SYSON;

When the ADC is configured as hardware trigger (PA4/PB3 or PWM), GO/DONE is directly set by the hardware trigger event and starts A/D conversion, and the software set GO/DONE will be ignored.

In applications with high sampling rates, there are 3 time points to pay attention to when using the ADC:

1. The moment when the selected channel starts sampling.
2. The moment when the sampling ends. Immediately before the sample-and-hold circuit is disconnected, the voltage value on the selected channel is used to measure the conversion.
3. The moment when the data conversion is completed.

11.1. Summary of ADC Related Registers

Name	Addr.	bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0	Reset
PCKEN	0x9A	-	-	UARTEN	-	TIM4EN	TIM2EN	TIM1EN	ADCEN	--00 0000
CKOCON	0x95	SYSON	CCORDY	DTYSEL		CCOSEL[2:0]			CCOEN	0010 0000
ADRESL	0x9B	LSB of A/D conversion result								xxxx xxxx
ADRESH	0x9C	MSB of A/D conversion result								xxxx xxxx
ADCON0	0x9D	-	CHS[2:0]			-	ADEX	GO/DONE	ADON	-000 -000
ADCON1	0x9E	ADFM	ADCS[2:0]			ADNREF[1:0]		ADPREF[1:0]		0000 0000
ADCON2 ¹	0x9F	ADINTREF[1:0]		ETGTYP[1:0]		ADDLY.8	ETGSEL[2:0]			0000 0000
ADDLY ¹	0x1F	ADDLY[7:0] / LEBPRL[7:0]								0000 0000
ADCON3 ¹	0x41A	ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	LEBADT	-	ELVDS[1:0]		0000 0-00
ADCMPH	0x41B	ADCMPH[7:0]								0000 0000
LEBCON ¹	0x41C	LEBEN	LEBCH		-	EDGS	BKS2	BKS1	BKS0	000- 0000

Table 11-1 ADC Related Register Address

¹ This register is still readable and writable when ADCEN = 0.

Name	Status	Register	Addr.	Reset
GIE	Global Interrupt 1 = Enable (PEIE, ADCIE apply) 0 = <u>Global Shutdown</u> (Wake-Up not affected)	INTCON[7]	Bank First address + 0x0B	RW-0
PEIE	Peripheral Interrupt Enable 1 = Enabled (ADCIE applies) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0
ADCIE	ADC Conversion Completion Interrupt 1 = Enable 0 = <u>Disable</u> (no Wake-Up)	PIE1[0]	0x91	RW-0
ADCIF ²	ADC Conversion Completion Flag 1 = Yes (latched) 0 = <u>No</u>	PIR1[0]	0x11	R_W1C-0

Table 11-2 ADC Interrupt Enable and Status Bits

Name	Status	Register	Addr.	Reset
ADRESL	<u>LSB of A/D conversion result</u> ADFM=0: ADRESL[7:4] = least significant of 4 bits (the rest are "0") ADFM=1: ADRESL[7:0] = LSB	ADRESL[7:0]	0x9B	RW-0000 0000
ADRESH	<u>MSB of A/D conversion result</u> ADFM=0: ADRESH[7:0] = MSB ADFM=1: ADRESH[3:0] = Most significant of 4 bits (the rest are "0")	ADRESH[7:0]	0x9C	RW-0000 0000
SYSON	<u>In SLEEP mode, the system clock controls</u> 1 = Enable 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
ADCEN	<u>ADC Clock</u> 1 = Enable 0 = <u>Disable</u>	PCKEN[0]	0x9A	RW-0
CHS	<u>ADC Analog Input Channel</u> 000 = AN0 001 = AN1 010 = AN2 011 = AN3 100 = AN4 101 = AN5 110 = AN6 111 = 1/4 V _{DD}	ADCON0[6:4]	0x9D	RW-000
ADEX	<u>ADC Trigger Condition (GO/DONE)</u> 1 = GO/DONE is set by PA4 / PB3 or PWM (hardware triggered) 0 = <u>GO/DONE</u> is set by instructions (software triggered)	ADCON0[2]		RW-0

² Write '1' to clear, and writing '0' has no effect on the bit value. It is recommended to only use the STR and MOVWI instructions for write operations, rather than the BSR or IOR instructions.

Name	Status	Register	Addr.	Reset
GO/DONE	<u>ADC Conversion Start and status bits</u> 1 = A/D conversion enabled by software, PA4/PB3 or PWM (auto clear after conversion is complete) 0 = <u>Conversion completed / No conversion</u>	ADCON0[1]		RW-0
ADON	1 = ADC enabled 0 = <u>ADC disabled</u> (no current consumption)	ADCON0[0]		RW-0
LFMOD	1: LIRC = 256kHz 0: LIRC = <u>32kHz</u>	TCKSRC[7]	0X31F	RW-0
ADFM	<u>A/D Conversion Result Format (See "ADRESH")</u> 1 = Right aligned 0 = <u>Left aligned</u>	ADCON1[7]		RW-0
ADCS	<u>A/D Conversion Clock Sources</u> 000 = <u>SysClk/2</u> 100 = SysClk/4 001 = SysClk/8 101 = SysClk/16 010 = SysClk/32 110 = SysClk/64 011 = LIRC 111 = LIRC	ADCON1[6:4]	0x9E	RW-000
ADNREF	<u>V_{ADC-REF-} (negative reference voltage)</u> 00 = Internal V _{ADC-REF} 01 = <u>GND</u> 10 = Internal V _{ADC-REF} + External Capacitor C _{EXT} 11 = External reference voltage (I/O)	ADCON1[3:2]	0x9E	RW-00
ADPREF	<u>V_{ADC-REF+} (positive reference voltage)</u> 00 = <u>Internal V_{ADC-REF}</u> 01 = V _{DD} 10 = Internal V _{ADC-REF} + External Capacitor C _{EXT} 11 = External reference voltage (I/O)	ADCON1[1:0]	0x9E	RW-00
ADINTREF	<u>Internal V_{ADC-REF}</u> 00 = <u>0.5</u> 01 = 2.0 10 = 3.0 11 = (not connected)	ADCON2[7:6]	0x9F	RW-00
ETGTYP	<u>External Trigger Edge (applicable when ADEX=1)</u> 00 = <u>(PWM or PA4/PB3-ADC_ETR) Falling edge</u> 01 = (PWM or PA4/PB3-ADC_ETR) Rising edge 10 = Midpoint of one PWM period (*)	ADCON2[5:4]		RW-00

Name	Status	Register	Addr.	Reset
	11 = End of one PWM period ^(*) (*) : The center-aligned PWM mode of TIM1 is selected by default ;			
ADDLY.8 /LEBPR9	8th bit of ADC Delay Counter or LEB Counter (See "ADDLY")	ADCON2[3]		RW-0
ETGSEL	<u>External Trigger Source (applicable when ADEX=1)</u> 000 = <u>PWM1, TIM1_CH1</u> 100 = PWM5, TIM2_CH1 001 = PWM2, TIM1_CH2 101 = PWM6, TIM2_CH2 010 = PWM3, TIM1_CH3 110 = PWM7, TIM2_CH3 011 = PWM4, TIM1_CH4 111 = ADC_ETR	ADCON2[2:0]		RW-000
ADDLY /LEBPRL	<u>ADC Delay/LEB (Non-software triggered, i.e. valid when ADEX = 1)</u> (This is the LSB, ADDLY.8 is the MSB) Delay time = (ADDLY+6) x T _{AD} (If the PWM output is enabled to trigger the ADC, ADDLY must not be changed during PWM operation)	ADDLY[7:0]	0x1F	RW-0000 0000
ADFBEN	<u>ADC Threshold Comparison Result Match Event Triggers PWM Fault-Break</u> 1 = Enable 0 = <u>Disable</u>	ADCON3[7]		RW-0
ADCMPOP	<u>Polarity of ADC Threshold Comparison</u> 1 = MSB of ADC result < ADCMPH[7:0] 0 = MSB of ADC result ≥ ADCMPH[7:0]	ADCON3[6]		RW-0
ADCM PEN	<u>ADC Threshold Comparison</u> 1 = Enable 0 = <u>Disable</u> (Clear the break event generated by ADCMP)	ADCON3[5]		RW-0
ADCMPO	<u>ADC Comparison Output (Updated every time A/D conversion is completed)</u> When ADCMPPOP = 1 1 = MSB of ADC result < ADCMPH[7:0] (no latch) 0 = MSB of ADC result ≥ ADCMPH[7:0] when ADCMPPOP = 0 1 = MSB of ADC result ≥ ADCMPH[7:0] (no latch) 0 = MSB of ADC result < ADCMPH[7:0]	ADCON3[4]	0x41A	RO-0
LEBADT	<u>ADC starts automatic conversion after LEB</u> 1 = Trigger ADC conversion	ADCON3[3]		RW-0

- External Reference Voltage (V_{REF+} for PA1, V_{REF-} for PA0)

V_{REF+} and V_{REF-} can be different combinations of the above selections, the internal reference voltage cannot be selected at the same time, otherwise V_{REF-} will be forced to connect to GND.

The internal reference voltage can be 0.5V, 2.0V, 3.0V or "Not connected" (see "ADINTREF").

ADC Conversion Clock Selection – The ADC can select 7 clock frequencies by instructions (see "ADCS"):

- SysClk/N; N = 2, 4, 8, 16, 32, 64
- LIRC (256 kHz or 32 kHz, see "LFMOD")

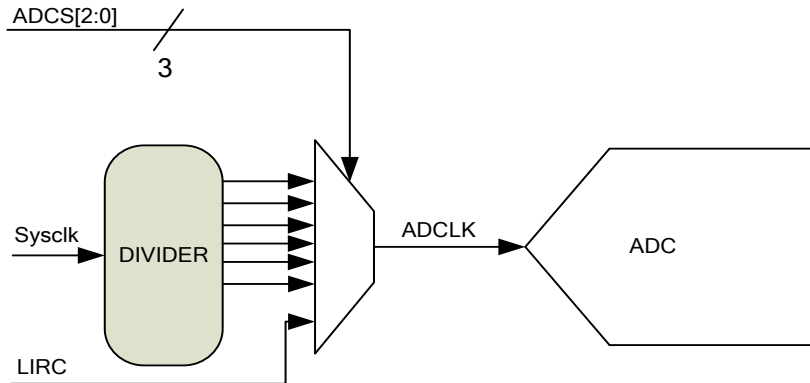


Figure 11-2 ADC Clock Configuration

Conversion Result Format – A/D conversion results can be stored in either left-aligned or right-aligned formats (see "ADFM"). A/D auto-calibration values are also affected by this format.

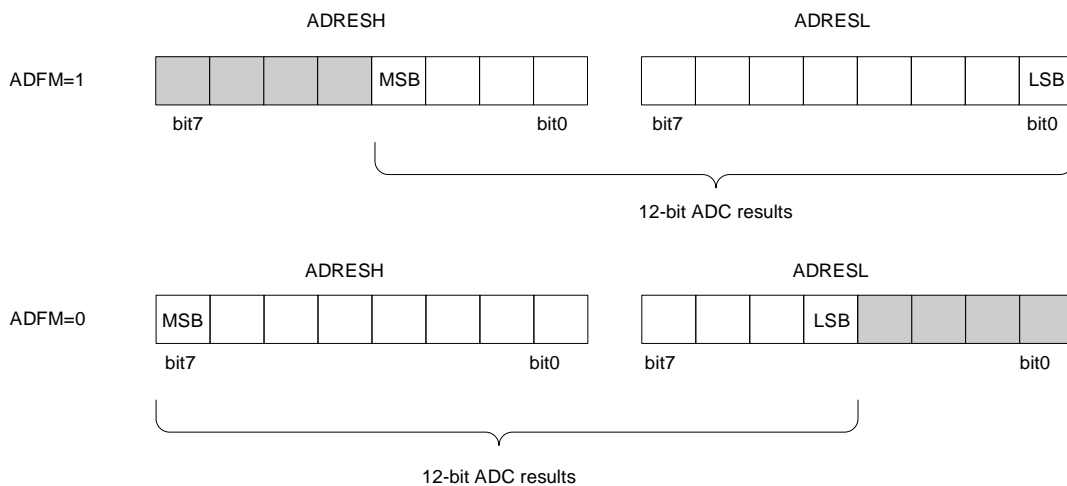


Figure 11-3 ADC Conversion Result Format

11.2.1. ADC Trigger and Configuration of Delay

ADC conversion can be triggered by an instruction (ADEX = 0), PWM (edge / cycle) or I/O (PA4 / PB3) transition edge (ADEX = 1). Among them, the trigger type of PWM can be selected as "Rising edge", "Falling edge", "Midpoint of cycle" or "End of cycle", and the trigger edge of PA4 / PB3 can be selected as "Rising edge" or "Falling edge" (see "ETGTYP" and "ETGSEL").

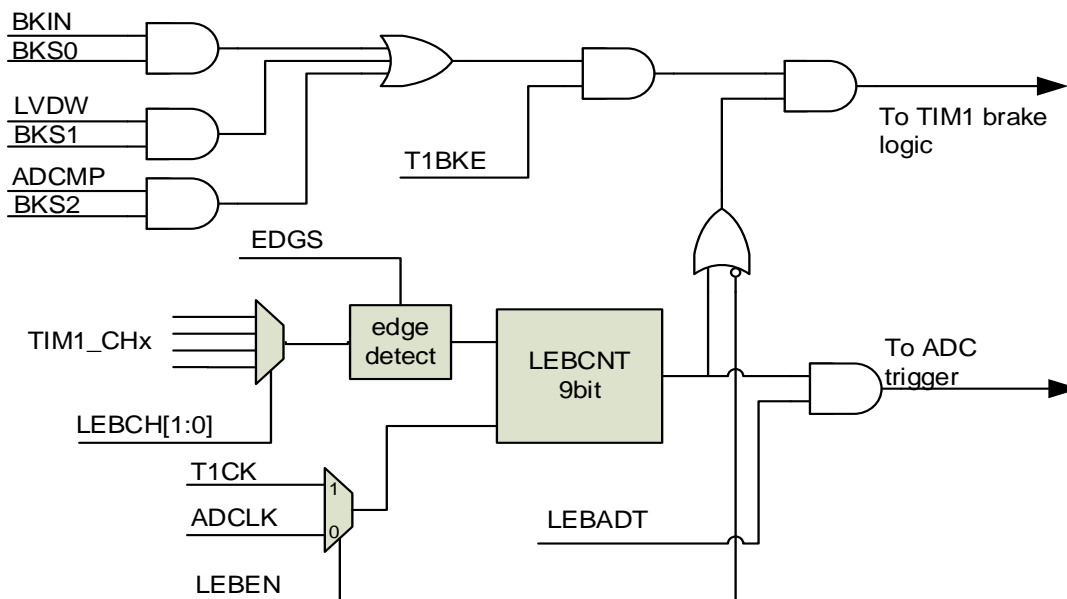


Figure 11 -4 LEB Block Diagram

In high-speed switching applications, the conduction of switching devices (e.g. MOSFETs/IGBTs) usually generates extremely large transient currents immediately, and these transients can lead to measurement errors. Considering the LEB feature, applications can ignore the expected transients caused by the MOSFETs / IGBTs near the PWM Output Edge.

The Clock Source for both LEB and PWM is T1CK (Timer1 Clock Source). During LEB timing, the ADC keeps sampling until LEB timing overflows (see "LEBPR", Table 11-3). If an active LEB trigger edge occurs again during the LEB timing cycle, the LEB timer will resume and start counting again

Trigger Conditions	Delay/LEB	Trigger Channel
Instruction	(No delay)	(N/A)
I/O (PA4/PB3)	$(ADDLY+6) \times T_{AD}$; $ADDLY = LEBPR$	I/O (PA4 or PB2)
PWM	$(LEBPR+6) \times T_{AD}$	LEBEN = 0; ETGSEL (LEBCH ignored)
	$(LEBPR+3) \times T_{T1CK} + 3 \times T_{AD}$ ($T_{T1CK} = \text{Timer1 period}$)	LEBEN = 1; LEBCH (ETGSEL ignored)

Table 11-4 ADC Trigger, Delay and Channel Settings

If triggered by software (ADEX = 0), A/D conversion starts immediately after GO/DONE is set by the instruction. If triggered by PA4/PB2 or PWM, there is a certain delay time (" $6 \times T_{AD}$ " or " $3 \times T_{T1CK} + 3 \times T_{AD}$ ", see Table 11-4). Before GO/DONE is set, additional delay can be added by setting the ADDLY/LEBPR registers. The ADC delay timer (ADDLY) and the LEB timer (LEBPR) share the same 9-bit counter, which consists of LEBPR9 and LEBPRL[7:0]. After the delay, the sample-and-hold circuit will be disconnected within " $3.5 \times T_{AD} - 4.5 \times T_{AD}$ " time.

Note:

1. ADEX and ADON registers need to be set before enabling LEB.

2. New trigger conditions will be ignored until the ADC conversion is completed. .
3. If LEBEN=1, ETGSEL will be ignored, and will share the trigger source with LEB. At this time, the automatic conversion of the ADC will be triggered by the overflow of the LEB timer (see "LEBADT" or "EDGS", [Table 11-3](#)).

11.2.2. ADC Aborts Conversion

Sometimes ADC need to be aborted, such as starting new sampling.

- When ADEX = 0 (instruction triggered), the ADC can be aborted by software setting GO/DONE = 0.
- When ADEX = 1, the ADC must be stopped by turning off the ADC module (ADON = 0).
- When ADC conversion is aborted, the aborted operation takes $4 \times T_{AD}$ to process, after which ADRESH and ADRESL will be partially updated with the value of the converted completed bits and the incomplete bits will all be filled with the value of the last converted bit.
- When the system is reset, the ADC will be aborted and the ADC module will be turned off because the corresponding registers are reset.

11.2.3. Threshold Comparison

The ADC can automatically compare the result with the threshprevious value in the ADCMPH register after the conversion is completed (see "ADCMPEN"). The comparison polarity is set by ADCMPOP, and the comparison result is output by ADCMPO. The PWM Fault Break can be triggered when the corresponding matching condition occurs (see "ADFBEN"). Only the MSB of the conversion result is used for the threshold comparison, so the comparison step between V_{REF+} and V_{REF-} is 0.4%.

Note:

1. ADCMPO will be cleared when ADCMPEN = 0 or ADON = 0; when entering sleep mode, ADCMPO will not be cleared.

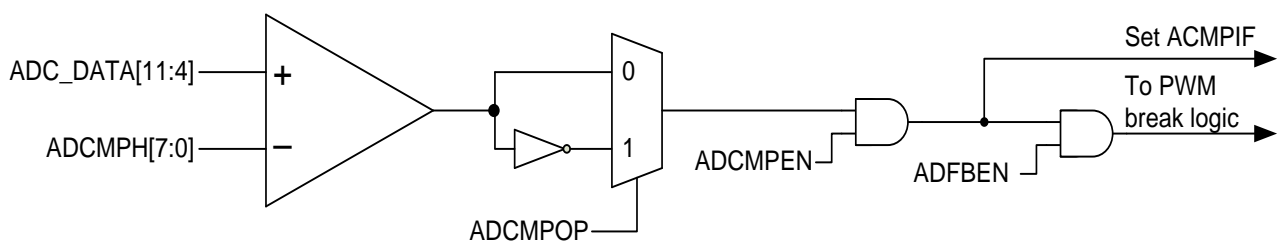


Figure 11-5 ADC Threshold Comparison Block Diagram

11.2.4. Interrupt

The corresponding interrupt flag bit ADCIF will be set when the ADC conversion is complete. Whether to trigger an interrupt and/or wake up from SLEEP depends on the corresponding interrupt enable control bits (GIE, PEIE, ADCIE).

Note:

1. ADCIF is set every time an ADC normal conversion completes, regardless of whether the Interrupt

Enable is on.

- ADCIF will not be set when automatic calibration is completed or when software aborts AD conversion.

11.3. Sample-and-hold time

The sample hold time, T_{ACQ} must be long enough to ensure that the internal ADC voltage is stable within 0.01% of the input channel voltage, resulting in 12-bit accuracy (0.024%). The relationship between the sample-and-hold time and the external series resistance is as follows (**Table 11-5**):

$$T_{ACQ} > 0.09 \times (R + 1) \mu s . \text{ (the unit of R is k}\Omega \text{) .}$$

When T_{ACQ} is $2\mu s$, the external series resistor must $\leq 21 \text{ k}\Omega$. If a larger series resistor is used, T_{ACQ} will increase proportionally. Junction leakage current limits the maximum allowable value of series resistance. For a junction leakage current of 5nA, a voltage drop of 0.25mV (0.0125% of the 2V reference) occurs across the series resistance of 50 k Ω . When the temperature exceeds 100°C, the junction leakage current will increase significantly. Therefore, the smaller the series resistance is, the better.

Series resistance	T_{ACQ}
> 50k Ω	(Not recommended)
43 k Ω	$\geq 4.0 \mu s$
21 k Ω	$\geq 2.0 \mu s$
< 21 k Ω	$\geq 2.0 \mu s$

Table 11-5 Correspondence between different external series resistances and the shortest T_{ACQ}

The sample-and-hold time is the time that the internal ADC observes the voltage of the input channel.

Start of sample-and-hold time = after channel switching (see “CHS”) or ADC stabilization (see T_{ST}), the longer time shall prevail.

End of sample-and-hold time = $0 - 1 \times T_{AD}$ after the hardware trigger delay or setting GO/DONE to 1 by software, the delay time is determined by the trigger condition (see **Table 11 -4**), and the sample-and-hold circuit is disconnected.

Sampling point = the instant before the sample-and-hold circuit is disconnected, with the uncertainty of $0 - 1 \times T_{AD}$.

Data conversion starts after turning off the sampling, and the conversion process takes $16 \times T_{AD}$. Therefore, it takes $16 \times T_{AD}$ to $17 \times T_{AD}$ from the end of the hardware trigger delay or the software GO/ONE setting to the completion of data conversion. After the data conversion is completed, the sample-and-hold circuit is shutdown again to start the next sampling cycle. It is also necessary to wait for a sufficient sampling time T_{ACQ} before starting A/D conversion again.

11.4. Minimum sampling time

T_{AD} is the clock cycle of the ADC. The minimum time required to complete 12-bit conversion: $T_{ACQ} + 17 \times T_{AD}$

The maximum sampling rate that can guarantee the accuracy of 11-bit accuracy is 100 kHz (~10 μs /sample)

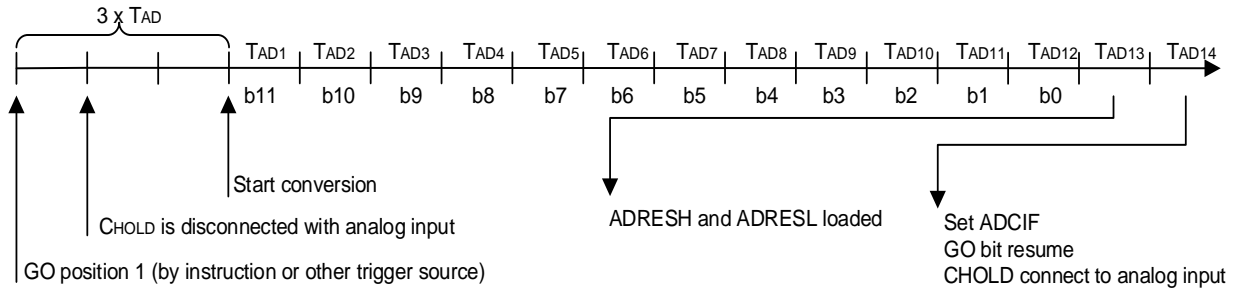


Figure 11-6 Analog-to-Digital conversion T_{AD} cycle

11.5. Example of ADC Conversion Steps

To set up the ADC:

1. Set $ADCEN = 1$ to turn on the ADC module clock.
2. Configure the PORT:
 - a. Set $TRISx = 1$ to disable pin output driving;
 - b. Set $ANSELx = 1$ to disable digital input, weak pull-up and weak pull-down.
3. Configure the ADC module:
 - a. Select ADC conversion clock source;
 - b. Select ADC reference voltage;
 - c. Select ADC trigger conditions: software, PA4/PB3-ADC_ETR or PWM, with or without LEB;
 - d. Select the conversion result format;
 - e. Enable threshold comparison (optional);
4. Configure ADC interrupt (optional):
 - a. Enable ADC conversion completion interrupt;
 - b. Enable Master Peripheral Interrupt;
 - c. Global Shutdown (enable if the interrupt service routine needs to be executed);
5. Turn on the ADC module. Then wait for the required stabilization time T_{ST} (~15 μs), when $V_{ADC-REF}$ selects the internal reference voltage, then wait for the longer of the internal reference voltage stabilization time T_{VRINT} (see " T_{VRINT} ", [Section 16.7](#)) and T_{ST} time, namely $\max(T_{VRINT}, T_{ST})$.

So far, the ADC is ready to sample the different channels. When sampling the input channel:

1. The ADC input is selected as the channel to be measured (see "CHS").
2. If necessary, clear the ADC conversion completion interrupt flag ADCIF.
3. The shortest sampling time T_{ACQ} , which must be long enough to ensure that the internal ADC input capacitor is fully charged within 0.01% of the input channel voltage. In addition, depending on the trigger type, there may be a delay in retriggering after switching channels or after the ADC has stabilized (the longer time shall prevail).

- a. For software triggering, additional T_{ACQ} is required.
- b. For PA4/PB3-ADC_ETR or PWM triggering, unless a very large series resistor is used, the internal delay time $(ADDLY+6) \times T_{AD}$ is usually longer than T_{ACQ} , so no additional delay T_{ACQ} is required .
4. After waiting the delay required, set GO/DONE by an instruction, or wait for a hardware trigger event to automatically set GO/DONE to start the A/D conversion.
5. Wait for the conversion to complete by:
 - a. waiting for one sysclk cycle and querying the GO/DONE bit;
 - b. waiting for ADC interrupt (when interrupt is enabled).
6. Read ADC conversion result.
7. If necessary, clear the ADCIF.

Note:

1. Although GO/DONE and ADON are in the same register (ADCON0), they should not be set at the same time.
2. The configuration cannot be changed during conversion or while waiting for an external trigger. Changes are recommended when $ADON = 0$.

The following is an example of the ADC program (the input sampling channel is PB1, and the ADC clock is LIRC):

```

BANKSEL PCKEN
BSR PCKEN,0           ; ADC module clock
BANKSEL TRISB
BSR TRISB,1           ; Set PB1 to input
BANKSEL ANSELA
BSR ANSELA, 0         ; Set PB1 to analog
BANKSEL ADCON1
LDWI B'11110101'     ; Right justify, ADC LIRC clock
STR ADCON1            ; Vref+: VDD, Vref-: GND
BANKSEL ADCON0
LDWI B'00000000'     ; Select channel AN0
STR ADCON0
BSR ADCON0,ADON       Turn ADC On
CALL StableTime       ; ADC stable time
BSR ADCON0,GO         ; Start conversion
NOP                   ; GO/DONE ReadBack WaitTime
BTSC ADCON0,GO        ; Conversion done?
GOTO $-1              ; No, test again
BANKSEL ADRESH
LDR ADRESH,W          ; Read upper 4 bits
STR RESULTHI          ; store in SRAM space
BANKSEL ADRESL
  
```

LDR ADRESL,W ; *Read LSB*
STR RESULTLO ; *Store in SRAM space*

12. USART INTERFACE

The Universal Synchronous/Asynchronous Transceiver USART can communicate with peripherals in the industry standard NRZ serial data format. Features are as follows:

- Full-duplex, single-wire half-duplex asynchronous mode
- Full Duplex Synchronous Mode
 - ✓ Synchronized Clock Output : Programmable Clock Polarity and Phase
- Infrared 1.0 mode
 - ✓ 8-bit prescaled baud rate generator
 - ✓ Low power mode
- Smart card mode
 - ✓ 8-bit prescaled baud rate generator
 - ✓ STOP: 1.5 bits
 - ✓ Programmable guard time
- LIN master mode
 - ✓ Support the transmission and detection of disconnected frames
- Multi-chip communication mode
 - ✓ The mute mode can be woken up by address matching or IDLE frame, and it starts to receive data after waking up
- Data transmission length: 7, 8 or 9 bits
- Parity bit
- STOP: 1 or 2 bits
- 16-bit programmable baud rate generator up to 1 Mbit/s
- Data is sent/received from low bits
- Transmitter and receiver can be enabled independently
- Automatic baud rate detection
- Support USART interface TX open-drain output
- Send BUF is empty interrupt, receive BUF is not empty interrupt
- Send completion interrupt
- Idle frame interrupt
- Receive status interrupt: frame break, frame error, parity error, or receive overflow

Note: The default is asynchronous full-duplex mode. When the operating mode is selected, please disable other modes.

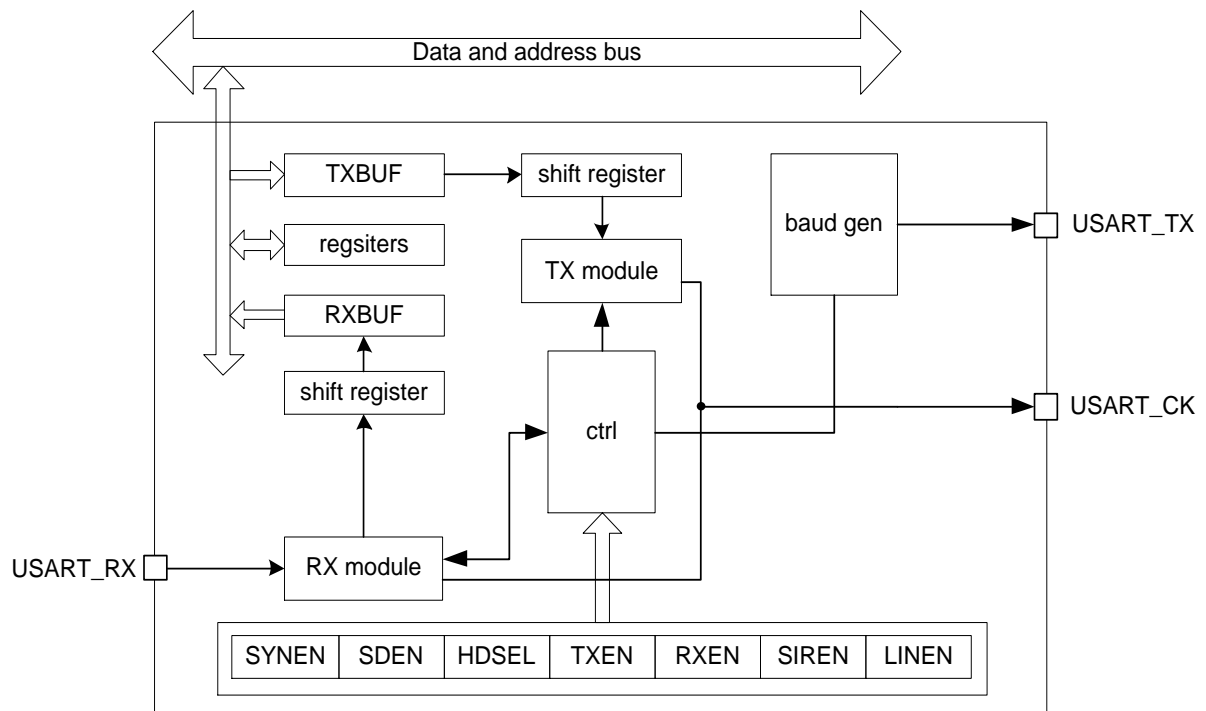


Figure 12-1 USART Block Diagram

The USART serial module has 3 pins:

USART_RX: Serial data input.

USART_TX: Serial data output. In single-wire half-duplex mode, the TX pin is used for both data input and data output (need to be configured in open-drain mode).

USART_CK : used as synchronous clock output in synchronous mode, and used as system clock frequency division output in smart card mode.

Note:

- When the transmitter is enabled, but not transmitting data, the TX pin is high.
- When the transmitter is enabled and data is transmitted, the TX pin is low during the START and high during the STOP.

12.1. Summary of USART Interface Related Registers

Name	Status	Register	Addr.	Reset
UARTEN	<u>USART module clock</u> 1 = Enable 0 = <u>Disable</u>	PCKEN[6]	0x9A	RW-0
SYSON	<u>In SLEEP mode, the system clock controls</u> 1 = Keep active 0 = <u>Disable</u>	CKOCON[7]	0x95	RW-0
DATAL	Data transmission/reception BUF LSB (inappropriate bit manipulation)	URDATA[7:0]	0x48C	RW-0000 0000
DATAH	Send/receive MSB of 1 bit BUF (when EXTEN=1) Note: DATAL needs to be written first, then DATAH;	URDATAH[0]	0x48D	RW-0
BKREQ	<u>Send break frame</u> 1 = Enabled, or in progress 0 = <u>Disabled, or transmission completed</u> Note: 1. Please set the length of the disconnected frame before sending the disconnected frame; 2. This bit auto clear after the transmission is completed, and it is forbidden to write 0 to it during the transmission process;	URLCR[6]	0x48F	RW-0
EVEN	<u>Odd/even parity</u> 1 = Even parity 0 = <u>Odd parity</u>	URLCR[4]		RW-0
PEN	<u>Parity Enable</u> 1 = Enable 0 = <u>Disable</u>	URLCR[3]		RW-0
URSTOP	<u>STOP length</u> 1 = 1.5 bit (smart card mode) or 2 bits 0 = <u>1 bit</u>	URLCR[2]		RW-0
LTH	<u>Communication data length control (excluding parity bit)</u> 1 = 8 bits 0 = <u>7 bits</u>	URLCR[0]		RW-0
RWU	<u>In multiprocessor mode, enter mute mode</u> 1 = Enable 0 = <u>Disable, or exits</u>	URLCREXT[1]	0x490	RW-0
EXTEN	<u>Communication data length total controls (excluding parity bits)</u> 1 = 9 bits 0 = <u>7 bits or 8 bits (depending on LTH)</u>	URLCREXT[0]		RW-0

Name	Status		Register	Addr.	Reset
SIRLP	<u>Infrared low power mode</u>	1 = Enable 0 = <u>Disable</u>	URMCR[5]	0x491	RW-0
TXEN	<u>Serial transmitter</u> 1 = Enable (pin TX function is automatically enabled) 0 = <u>Disable</u>		URMCR[4]		RW-0
RXEN	<u>Serial receiver</u> 1 = Enable (pin RX function is automatically enabled) 0 = <u>Disable</u>		URMCR[3]		RW-0
WAKE	<u>Mute mode wake-up method</u>	1 = Address matches 0 = <u>IDLE frame</u>	URMCR[2]		RW-0
HDSEL	<u>Half duplex</u>	1 = Enable 0 = <u>Disable</u>	URMCR[1]		RW-0
SIREN	<u>Infrared mode</u>	1 = Enable 0 = <u>Disable</u>	URMCR[0]		RW-0
RAR	Local address in multiprocessor mode[3:0]		URRAR[3:0]	0x493	RW-0000
DLL	<u>Baud rate divider counter LSB and MSB</u> baud rate = Fmaster / (16 * {DLH, DLL})		URDLL[7:0]	0x494	RW-0000 0000
DLH	Note: Fmaster = Sysclk; the minimum value of {DLH, DLL} is 0x0001, when it is 0x0000, USART does not work;		URDLH[7:0]	0x495	RW-0000 0000
ABRE	<u>Baud rate detect overflow Flag</u>	1 = Overflow 0 = <u>Normal</u>	URABCR[3]	0x496	RW-0
ABRM	<u>Baud rate detection mode</u> 1 = Detection length is [(START + 1st bit data) / 2] (The 1st bit of the data must be 1, the 2nd bit must be 0) 0 = Only the START length is detected (the 1st bit data must be 1)		URABCR[2]		RW-0
ABRF	<u>Baud rate flag detected</u> 1 = Detected 0 = <u>Not detected</u> Note: Write 0 to clear, after the bit is cleared, it will enter the baud rate detection again immediately. In order to ensure the bit detected is the START, it is recommended to clear this bit after RXNEF is set;		URABCR[1]		RW-0
ABREN	<u>Automatic baud rate</u>	1 = Enable	URABCR[0]		RW-0

Name	Status	Register	Addr.	Reset
	<u>detection</u> 0 = <u>Disable</u>			
LBCL	<u>In synchronous mode, the clock output corresponding to the last 1bit data (MSB) is sent</u> 1 = Enable 0 = <u>Disable</u>	URSYNCR[3]	0x497	RW-0
URCPHA	<u>Synchronous mode clock phase (data sampling point)</u> 1 = 2nd clock transition edge 0 = <u>1st clock transition edge</u>	URSYNCR[2]		RW-0
URCPOL	<u>Synchronous mode clock polarity (state of SCK when the bus is idle)</u> 1 = High level 0 = <u>Low level</u>	URSYNCR[1]		RW-0
SYNEN	<u>Synchronous mode</u> 1 = Enable (pin CK automatically outputs a synchronous clock) 0 = <u>Disable</u>	URSYNCR[0]		RW-0
LINEN	<u>LIN Master mode</u> 1 = Enable 0 = <u>Disable</u>	URLINCR[4]	0x498	RW-0
BLTH	<u>Break frame length (bit)</u> Note: BLTH>0 is valid, it is recommended to set it to 12bit or 13bit, if it is too short, the received frame will be misjudged as a normal frame;	URLINCR[3:0]		RW-0000
NACK	<u>Smart card mode, reply NACK when parity error is detected</u> 1 = Send NACK 0 = <u>Do not send NACK</u>	URSDCR0[6]	0x499	RW-0
CKOE	<u>Smart Card Clock Source</u> 1 = Enable (need to configure the PSC register to an active value) 0 = <u>Disable</u>	URSDCR0[5]		RW-0
SDEN	<u>Smart Card Mode</u> 1 = Enable (STOP must be 1.5bit) 0 = <u>Disable</u>	URSDCR0[4]		RW-0
GT	<u>Smart card mode, guard time (baud clock interval between two characters)</u> Note: The minimum value is 1 (0 is inactive), after the	URSDCR1[7:0]	0x49A	RW-0000 0000

Name	Status	Register	Addr.	Reset		
	protection time expires, the transmission completion flag will be set					
PSC	Divide the system clock to provide a clock for smart card or infrared low power consumption	URSDCR2[7:0]	0x49B	RW-0000 0000		
	Smart Card Clock Source				Infrared Low Power Clock Source	
	0				inactive	inactive
	1				divide by 2	divide by 1
	2				divide by 3	divide by 2
	3				divide by 4	divide by 3

255	256 frequency division	255 frequency division				

Table 12-1 USART Related User Registers

Name	Status	Register	Addr.	Reset
AFP1[5:4]	<u>USART_TX</u> 00 = PA6 10 = PA7 01 = PB6 11 = PA2	AFP1[5:4]	0x19F	RW-00
AFP1[3:2]	<u>USART_RX</u> 00 = PA7 10 = PA6 01 = PA2 11 = PB6	AFP1[3:2]		RW-00
UROD	<u>USART_TX Open-Drain Output</u> 1 = Enable 0 = Disable	ODCON0[0]	0x21F	RW-0

Table 12-2 USART Interface Pin Control

Name	Status	Register	Addr.	Reset
GIE	Global Interrupt 1 = Enable (PEIE, URTE, URRXNE, TCEN, IDELE, RXSE applicable) 0 = <u>Global Shutdown</u> (Wake-Up is not affected)	INTCON[7]	Bank First address+0x0B	RW-0
PEIE	Peripheral Interrupt Enable 1 = Enable (URTE, URRXNE, TCEN, IDELE, RXSE apply) 0 = <u>Disable</u> (no Wake-Up)	INTCON[6]		RW-0
URTE	Transmit BUF as empty interrupt 1 = Enable 0 = <u>Disable</u>	URIER[1]	0x48E	RW-0

Name	Status	Register	Addr.	Reset
TXEF	Transmit BUF status 1 = Empty 0 = <u>Not empty</u> Note: write DATAL(8bit) / DATAH(9bit) to clear;	URLSR[5]	0x492	RO-1
URRXNE	Receive BUF as not empty interrupt 1 = Enable 0 = <u>Disable</u>	URIER[0]	0x48E	RW-0
RXNEF	Receive BUF status 1 = Not empty 0 = <u>Empty, or cleared</u> Note: read DATAL(8bit) / DATAH(9bit) to clear;	URLSR[0]	0x492	RO-0
TCEN	Transmit Completion Interrupt 1 = Enable 0 = <u>Disable</u>	URIER[5]	0x48E	RW-0
TCF	Transmission Completion Flag 1 = Yes 0 = <u>No</u> Note: write 1 to clear, or write DATAL(8bit) Cleared after /DATAH(9bit);	URTC[0]	0x49C	R_W1C-1
IDELE	Idle Frame Interrupt 1 = Enable 0 = Disable	URIER[3]	0x48E	RW-0
IDLEF ¹	Idle Frame Detection Flag 1 = Detected 0 = <u>Not detected</u>	URLSR[6]	0x492	RW0-0
RXSE	Receive error interrupt 1 = Enable 0 = <u>Disable</u> Note: Conditions for receiving error interrupt are as follows BKF = 1 FEF = 1 PEF = 1 OVERF = 1	URIER[2]	0x48E	RW-0
BKF ¹	Receive Break Frame Flag 1 = Received 0 = <u>Not received, or cleared</u>	URLSR[4]	0x492	RW0-0
FEF ¹	Receive Frame Error Flag 1 = Yes 0 = <u>No, or cleared</u>	URLSR[3]	0x492	RW0-0
PEF ¹	Parity received Error Flag 1 = Yes 0 = <u>No, or cleared</u>	URLSR[2]	0x492	RW0-0

¹ Write '0' to clear, and writing '1' has no effect on the bit value.

Name	Status	Register	Addr.	Reset
OVERF ¹	Receive BUF Overflow Error Flag 1 = Overflow 0 = <u>Normal, or cleared</u>	URLSR[1]	0x492	RW0-0
WAKE	Mute Mode wake-up mode selection 1 = Address match 0 = <u>IDLE frame</u>	URMCR[2]	0x491	RW-0
ADDRF	Mute Mode address match Flag 1 = Match 0 = <u>Mismatch</u>	URLSR[7]	0x492	RO-0

Table 12-3 USART Interrupt Enable and Status Bits

Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset	
PCKEN	0x9A	—	—	UARTEN	—	TIM4E N	TIM2E N	TIM1E N	ADCEN	--00- 0000	
CKOCON	0x95	SYSON	CCORD Y	DTYSEL		CCOSEL[2:0]			CCOEN	0010 0000	
URDATAL	0x48C	DATAL[7:0]								0000 0000	
URDATAH	0x48D	—								DATAH	---- ---0
URIER	0x48E	—		TCEN	—	IDELE	RXSE	URTE	URRXNE	--0- 0000	
URLCR	0x48F	—	BKREQ	—	EVEN	PEN	STOP	—	LTH	-0-0 00-0	
URLCREXT	0x490	—							RWU	EXTEN	---- --00
URMCR	0x491	—		SIRLP	TXEN	RXEN	WAKE	HDSEL	SIREN	--00 0000	
URLSR	0x492	ADDRF	IDLEF	TXEF	BKF	FEF	PEF	OVERF	RXNEF	0000 0000	
URRAR	0x493	—				RAR[3:0]				---- 0000	
URDLL	0x494	DLL[7:0]								0000 0000	
URDLH	0x495	DLH[7:0]								0000 0000	
URABCR	0x496	—				ABRE	ABRM	ABRF	ABREN	---- 0000	
URSYNCR	0x497	—				LBCL	CPHA	CPOL	SYNEN	---- 0000	
URLINCR	0x498	—			LINEN	BLTH[3:0]				---0 0000	
URSDCR0	0x499	—	NACK	CKOE	SDEN	—				-000 ----	
URSDCR1	0x49A	GT[7:0]								0000 0000	
URSDCR2	0x49B	PSC[7:0]								0000 0000	
URTC	0x49C	—								TCF	---- ---1

Table 12-4 USART Related Register Addresses

12.2. USART function

12.2.1. Asynchronous Operating Mode

Full-duplex and half-duplex configuration process:

1. Set UARTEN = 1 to enable the USART module clock;
2. Set the communication baud rate = Fmaster / (16 * {DLH, DLL}) (see "DLH", "DLL");
3. Set the communication data length to 7, 8 or 9 bits (see "EXTEN", "LTH") ;
4. Set parity bit (see "PEN", "EVEN") ;
5. Set the length of STOP to 1 or 2 bits (see "URSTOP");
6. Select full-duplex (default) or half-duplex mode of operation (see " HDSEL ");
7. If necessary, enable the corresponding interrupt (see "GIE", "PEIE", "URTE", "URRXNE", "TCEN" and "RXSE" etc.);
8. Set TXEN = 1 or RXEN = 1 to enable transmit or receive function as required;

Note:

- Fmaster of USART peripheral clock= Sysclk;
- In half-duplex mode, if both transmitting and receiving functions are enabled, the transmitted data will also be received by the machine;

The data communication format of the asynchronous mode is to send the LSB first, and then send the MSB. The data frame format comparison with or without parity bit is as follows:

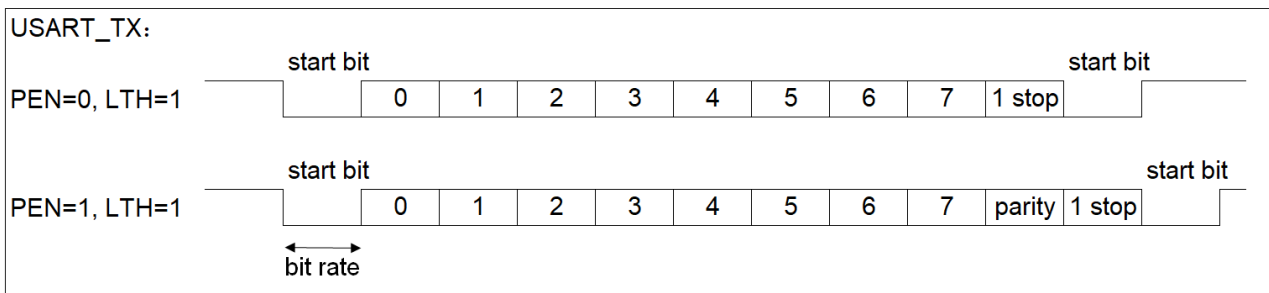


Figure 12-2 Communication Format in Asynchronous Mode (take 8bit length as an example)

The data processing flow includes blocking mode and non-blocking mode:

	Blocking mode	Non-blocking mode
Transmit data	After writing data to DATAL/H (TXBUF), query TXEF or TCF, write the next data when TXEF or TCF is set to 1	When URTE = 1 or TCEN = 1, TXEF or TCF is set to 1 to enter the interrupt after writing data to DATAL/H (TXBUF)
Receive data	Query RXNEF, the value of DATAL/H (RXBUF) can be read when RXNEF is set to 1	When URRXNE = 1, enter the interrupt after RXNEF is set to 1; In addition, it is recommended to enable the RXSE interrupt, and enter the corresponding interrupt for processing when receiving errors;
<i>Remark</i>	-	After entering the interrupt, query the corresponding status flag and handle the transmitting and receiving process, and exit the interrupt after the processing is completed

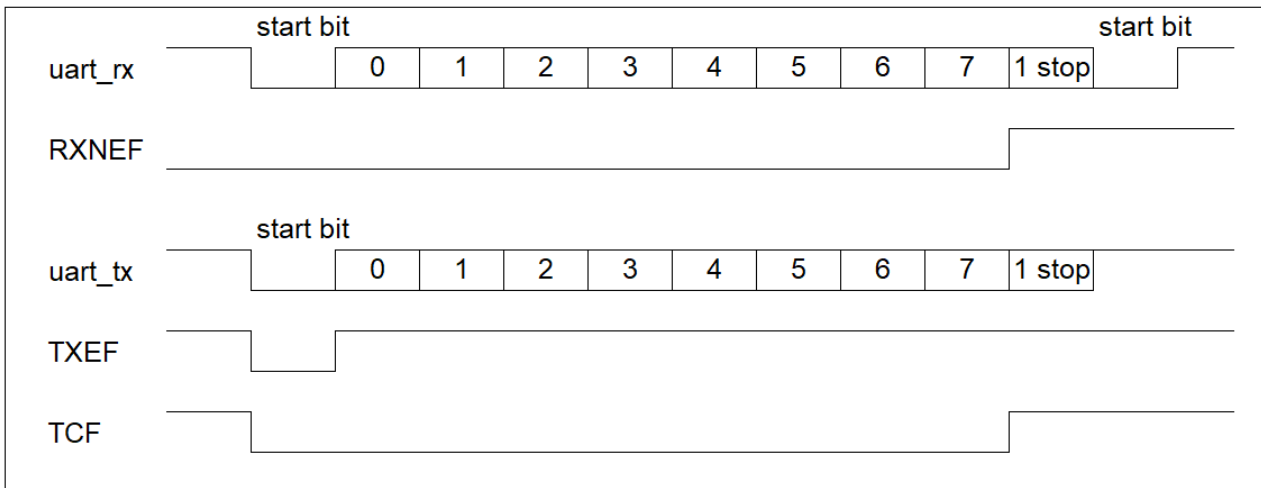


Figure 12-3 Asynchronous Mode Flag Timing Diagram

12.2.2. Synchronous Operating Mode

Synchronous mode is used to simulate the communication function in SPI master mode. When `SYNEN = 1`, the `USART_CK` pin will output a clock synchronized with the data. Data output sends the LSB first, followed by the MSB.

In addition, the polarity and phase of the synchronization clock can be selected (see "CPOL", "CPHA"). During the START and STOP, there is no clock pulse on the `USART_CK` pin. Whether to output the synchronous clock when the last 1bit of data is sent is determined by `LBCL`.

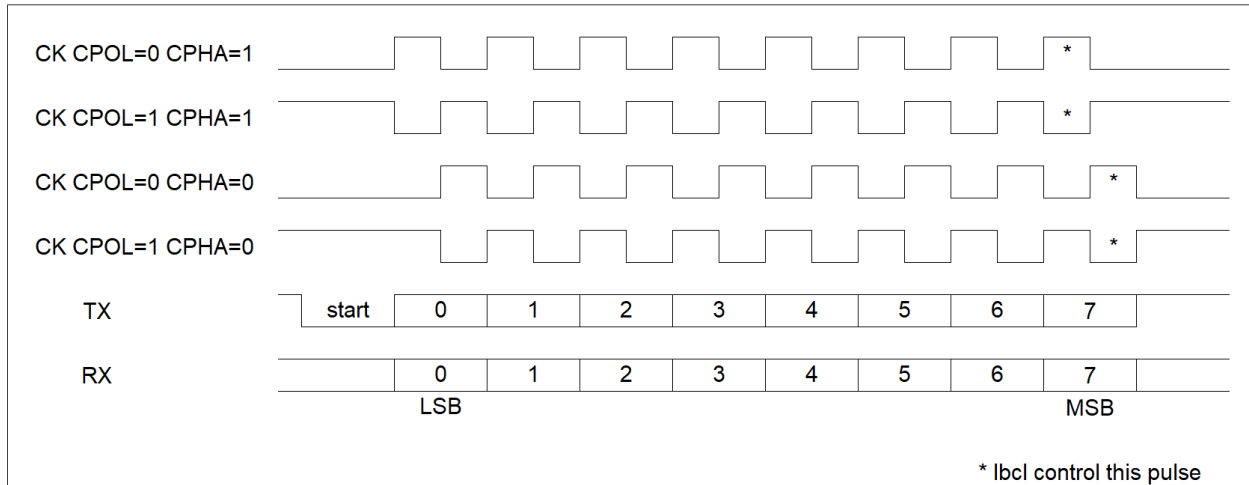


Figure 12-4 Sync Mode Communication Format (8bit Data Length)

Note:

- The sync clock rate is set the same as the baud rate, i.e. $F_{master} / (16 * \{DLH, DLL\})$;
- When TXEN = 0 and RXEN = 1, the synchronous clock will still be output, which is then used only for receiving data, and the TX pin remains high.

12.2.3. Infrared Operating Mode

Infrared mode is used for infrared communication. The infrared mode is enabled when SIREN = 1, and the default communication data length is 8 bits.

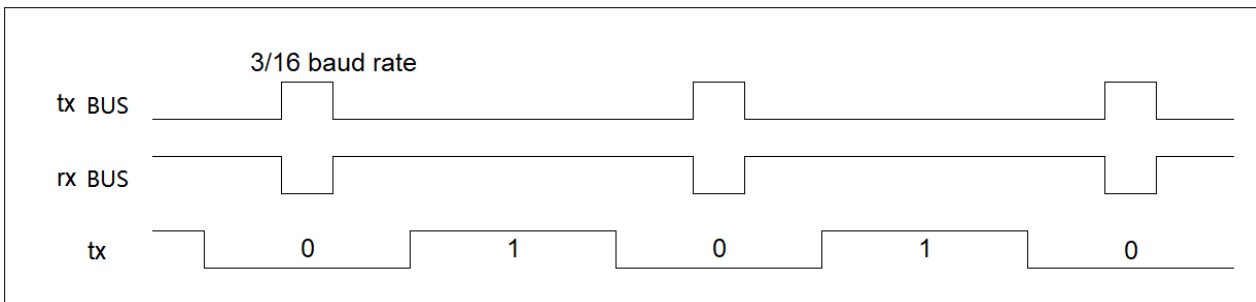


Figure 12-5 Infrared Mode Communication Timing Diagram

As shown in Figure 12-5, the data pulse width of the infrared module's transmitting or receiving bus is 3/16 of the bit cycle in normal mode . A high pulse is generated when the transmitted data is zero, and a low pulse is decoded as zero when it is received . The polarity of the transmitting and receiving bus are opposite, the bus keeps the low level when the transmitting is idle, and the bus keeps the high level when the receiving is idle.

Infrared module in normal mode, communication baud rate = $F_{master} / (16 * [DLH:DLL])$;

In low power mode (see "SIRLP"), communication baud rate = $F_{master} / (PSC * 16 * [DLH:DLL])$;

12.2.4. Smart Card Mode

The smart card mode is a half-duplex mode and supports the ISO7816-3 standard. When SDEC = 1, to

enable smart card mode, the protocol requires setting the data length to 8 bits (see "LTH"), enabling the parity bit (see "PEN"), and setting the stop bit to 1.5 bits (see "URSTOP"). "URSTOP"), and configure the corresponding IO to open-drain mode.

The clock source and the frequency division output of the smart card are set by CKOE and PSC.

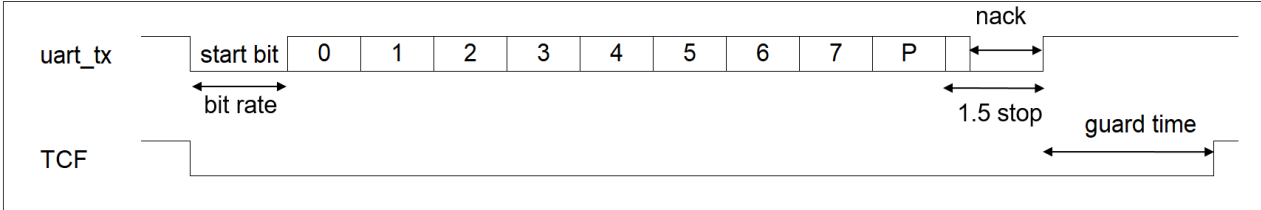


Figure 12-6 Smart Card Mode Communication Timing Diagram

When NACK = 1, after the receiver detects a parity error, it will pull down the bus for 1 bit cycle after 0.5 stop bits. At the same time, the transmitter will detect whether the bus is pulled down at the stop bit, if the bus is detected to be pulled down, the frame error flag FEF will be set to 1. The transmitter can choose to retransmit the current data upon request, and the number of transmissions is determined by the user.

When NACK = 0, the receiver will not pull down the bus after detecting a parity error, and the parity error flag PEF is set to 1.

In addition, in smart card mode, a guard time can be set (see "GT"), when the transmitter finishes transmitting data, wait for GT baud clock cycles before TCF is set.

12.2.5. LIN Master Mode

Enter LIN Master mode after LINEN is set.

The transmitter needs to configure the length of the break frame first (see "BLTH"). When setting BKREQ = 1 to enable disconnected frame transmission, the TX pin will continuously send BLTH low levels, and BKREQ will auto clear after the transmission is completed.

After receiving a number of consecutive low levels greater than (START + data length + STOP), the receiver will assume that a break frame has been received and the break frame flag BKF will be set to 1..

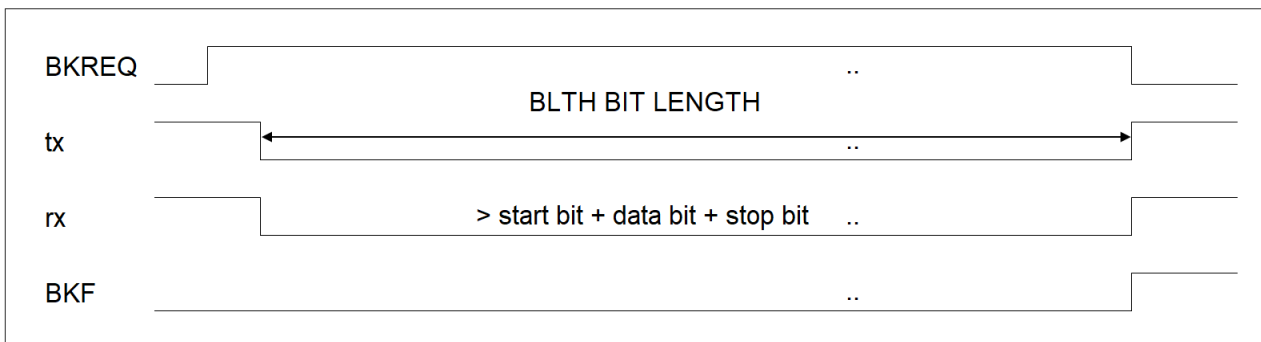


Figure 12-7 LIN Master Mode

Note: The reception and transmission of disconnected frames are not only applicable to LIN Master mode, but also to other asynchronous modes, infrared modes, etc.

12.2.6. Multiprocessor Communication Mode

Multiprocessor communication mode, for example, a USART is used as the master mode, other USARTs are used as the slave mode, and the TX output of the slave is connected to the RX input of the master by means of logical AND.

When RWU is set to 1, the master enters mute mode, blocking all reception. According to the setting of WAKE, there are two ways for USART to awake the master to receive data or exit mute mode:

- WAKE = 0: Wake-up by idle address. Wake-Up when an idle frame is detected and start receiving data. If the bus data is always busy, it will not Wake-Up.

Note: Idle frame, i.e. a complete data frame consisting entirely of '1' (Number of consecutive '1' bits \geq (START + data bit + STOP) number of bits).

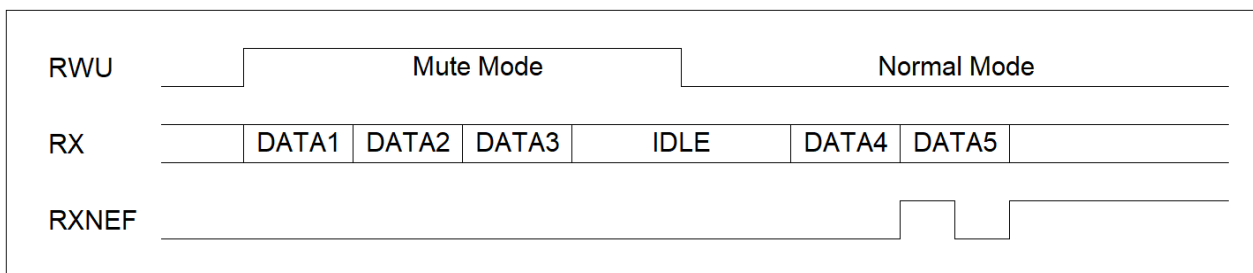


Figure 12-8 Mute Mode Address Idle Wake-Up

- WAKE = 1: Wake-up by address matching. Each time the data is received it will determine whether the high bit is 1 (indicating that the received data is address data). If the high bit is 1, continue to compare the LSB (4 bits) of the data with the value of URRAR. If they are equal, the address match flag ADDRFR is set to 1. Exit the mute mode and start receiving the following data. If it is not equal, it will enter the mute mode immediately.

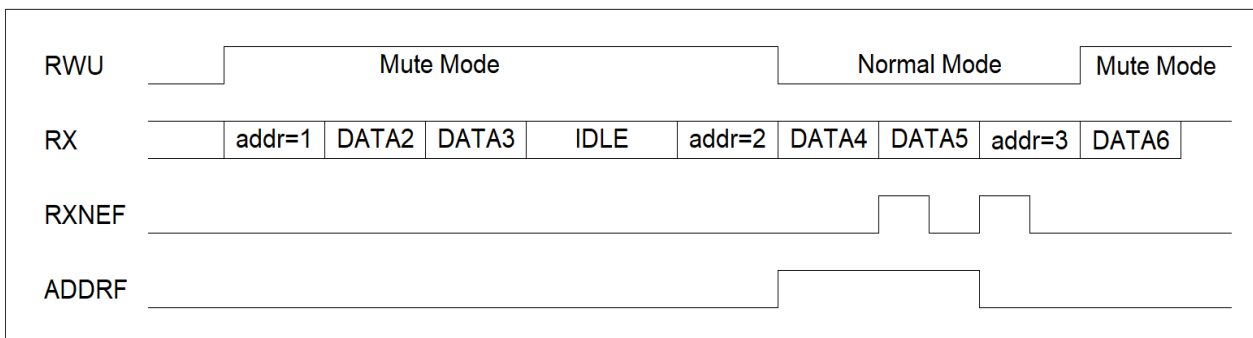


Figure 12-9 Mute Mode Address Match Wakeup

12.2.7. Automatic baud rate detection

The automatic baud rate detection function is used for the receiver to calibrate the communication baud rate so as to keep the same as the transmitter's baud rate. The baud rate detection module has two modes:

1. ABRM = 0: Only the length of the START is detected, and the 1st bit of the data is required to be 1. For example data 0x03, 0x55, etc.

2. ABRM = 1: Detect the START and the length of the 1st bit, and require the 1st bit = 1 and the 2nd bit = 0. For example data 0x55, 0x01 etc.

The baud rate detection data is used to automatically configure the DLL/DLH. If the baud rate data of the transmitter is not close to the receiver's $F_{baudrate} = F_{master} / (16 * \{DLH, DLL\})$, the baud rate detection module will be automatically configured to a closer baud rate. The serial PORT module does not support decimal baud rate, so there is an error in the baud rate detection of this module.

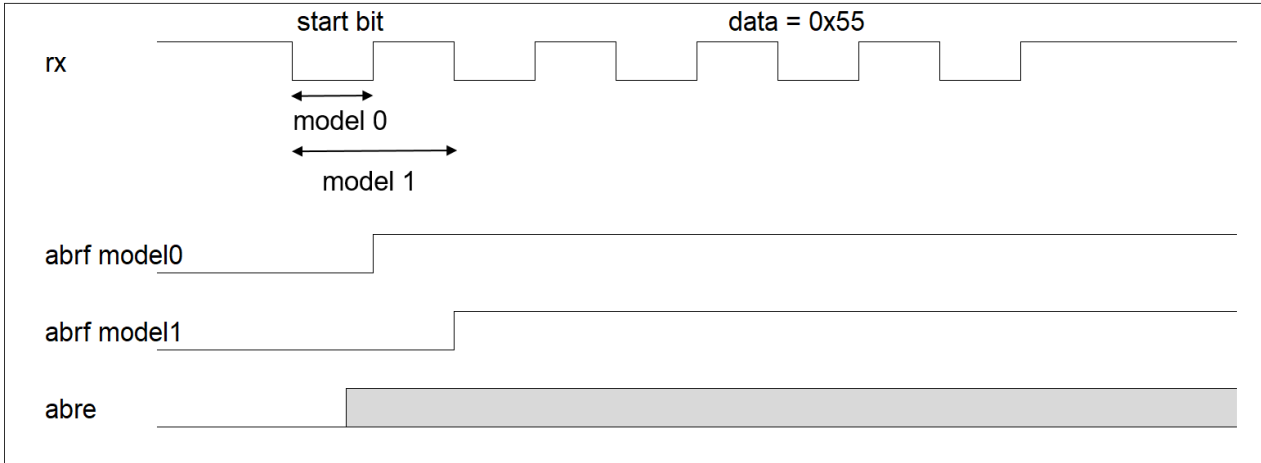


Figure 12-10 Automatic Baud Rate Detection

Process of automatic baud rate detection:

1. Select detection mode ABRM;
2. Configure ABREN = 1 to enable automatic baud rate detection;
3. Read and detect whether the baud rate flag ABRF is 1 (not cleared last time), if it is 1, write 0 to clear it;
4. Start to receive data, ABRF is set to 1 after baud rate detection is completed;
5. After the current data reception is completed, the receiving BUF as not empty flag RXNEF is set to 1;
6. Before starting the next baud rate detection, ABRF needs to be cleared first;

Note:

- ABRF must not be cleared immediately after baud rate detection is complete and ABRF is set to 1. Because clearing ABRF will immediately be in the current transmission position (which may no longer be the position of the START) to perform baud rate detection, resulting in wrong results .
- When the baud rate detection is out of range, the baud rate detection overflow flag ABRE will be set to 1.

13. MEMORY READ / WRITE PROTECTON

The PROGRAM AREA(PROM) can be Array Read Protected, or Sector Read/Program protected (1 k x 14 each). These protections selected at the IDE.

Name	Function	default
CPB	PROM Array Read Protection	disabled
FSECPB0	PROM Sector 0 (1k x 14) Read/Progarm Protection	disabled
FSECPB1	PROM Sector 1 (1k x 14) Read/Progarm Protection	disabled
FSECPB2	PROM Sector 2 (1k x 14) Read/Progarm Protection	disabled
FSECPB3	PROM Sector 3 (1k x 14) Read/Progarm Protection	disabled

Table 13-1 Bank Read/Write Protection Initialization Configuration Register

The difference between full encryption and sectorized encryption is as follows:

Encryption	CPU fetch	Software read	Software write	Serial read	Serial write
None	√	√	√(2)	√	√
Whole array	√	√	√(2)	×(1)	×(4)
Sector	√	×(1)	×(3)	×(3)	×(5)

Note:

1. EEDAT keeps the previous value unchanged;
2. Software cannot program or erase UCFG pages;
3. Only unencrypted sectors can be read or written;
4. Only the serial PORT is allowed to do full chip erasure (unencryption) including UCFG;
5. Only the serial PORT is allowed to do full chip erasure (unencryption) including UCFG, or page erase and programming of unencrypted sectors;
6. Under any circumstances, software cannot do full chip erasure including UCFG;

14. SPECIAL FUNCTION REGISTERS (SFR)

There are two types of Special Function Registers (SFR).

- BOOT level registers are set at the Integrated Development Environment (IDE);
- User registers.

14.1. Boot Level Registers



Figure 14-1 Boot Selectables in the IDE

Name	Function	default
CPB	PROM All-area Read Protection	Disabled
MCLRE	Reset by External I/O	Disabled
PWRTEB	Power-Up Timer (PWRT), additional delay~64ms after initialization configuration	Disabled
WDTE	<u>WDT</u> <ul style="list-style-type: none"> • Enable (Instructions can not be disabled) • <u>Instruction controls (SWDTEN)</u> 	SWDTEN control

Name	Function	default
FOSC	<ul style="list-style-type: none"> LP: external low-speed oscillator across PC1 (+) and PB7 (-) XT: external high-speed oscillator across PC1 (+) and PB7 (-) EC: external oscillator at PC1 (+), PB7 as I/O <u>INTOSCIO</u>: PC1 and PB7 as I/O 	INTOSCIO
STVREN	Stack overflow/underflow reset <ul style="list-style-type: none"> <u>Enabled</u> Disabled 	Enabled
OSTPER	<u>OST timer period selection (XT/LP apply)</u> <ul style="list-style-type: none"> 512 <u>1024</u> 2048 4096 (32768 in LP mode) 	1024
TSEL	<u>The correspondence between the instruction clock and the system clock SysClk (2T or 4T):</u> <ul style="list-style-type: none"> <u>2</u> (Instruction Clock = SysClk/2) 4 (Instruction Clock = SysClk/4) 	2
FSCMEN	<u>Fail-Safe Clock Monitor</u> <ul style="list-style-type: none"> <u>Enabled</u> Disabled 	Enabled
IESO	<u>XT/ LP two-speed clock start</u> <ul style="list-style-type: none"> <u>Enabled</u> Disabled 	Enabled
LVREN	<u>LVR</u> <ul style="list-style-type: none"> Enabled <u>Disabled</u> Enable in non-SLEEP mode Instruction controlled (SLVREN) 	Disabled
LVRS	<u>7 V_{BOR} Voltage levels (V): 2.0 / 2.2 / <u>2.5</u> / 2.8 / 3.1 / 3.6 / 4.1</u>	2.5
FSECPB0	PROM Sector 0 (1k x 14) Read/Write Protection	Disabled
FSECPB1	PROM Sector 1 (1k x 14) Read/Write Protection	Disabled
FSECPB2	PROM Sector 2 (1k x 14) Read/Write Protection	Disabled
FSECPB3	PROM Sector 3 (1k x 14) Read/Write Protection	Disabled

Table 14-1 Boot Level Registers (set by IDE)

14.2. User Registers

User Special Function Registers (SFR) and SRAM are stored in 12 banks (bank0~10, bank31), and each bank is 128 bytes in size. The corresponding bank must be selected before the registers inside can be accessed. A valid bank can be selected by writing the bank number (0~10, 31) to the Bank Selection Register (BSREG). The address of the user register is 12 bits, the address range is 0x000 ~ 0xFFFF, the MSB (5 bits) are the bank area address, and the LSB (7 bits) are the SFR/SRAM address.

All user registers can be accessed directly through INDFn, or indirectly through the FSRn File Selection Registers (see [Section 14.5](#), Indirect addressing).

Since extra instructions are involved in switching BANK, some often-used SFR are stored in all 12 banks to minimize switching. Registers common to all 12 BANKS are synchronized.

Bank	First address	Bank	First address
Bank0	000H	Bank6	300H
Bank1	080H	Bank7	380H
Bank2	100H	Bank8	400H
Bank3	180H	Bank9	480H
Bank4	200H	Bank10	500H
Bank5	280H	Bank31	F80H

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
First address + 0H	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
First address + 1H	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
First address + 2H	PCL	LSB of Program Counter's (PC)								0000 0000	
First address + 3H	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
First address + 4H	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
First address + 5H	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
First address + 6H	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
First address + 7H	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
First address + 8H	BSREG	Bank Selection Register								xxxx xxxx	
First address + 9H	WREG	Working register W								xxxx xxxx	
First address + AH	PCLATH	-	MSB of Program counter(PC) latches								---0 0000
First address + BH	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
First address + (70- 7F)		COMMON BANK SRAM								xxxx xxxx	

Table 14-2 Registers common to all 12 banks

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
000	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
001	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
002	PCL	LSB of Program Counter's (PC)								0000 0000	
003	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
004	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
005	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
006	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
007	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
008	BSREG	Bank Selection Register								xxxx xxxx	
009	WREG	Working register W								xxxx xxxx	
00A	PCLATH	-	MSB of Program counter(PC) latches								-000 0000
00B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
00C	PORTA	PORTA [7:0]								xxxx xxxx	
00D	PORTB	PORTB [7:0]								xxxx xxxx	
00E	PORTC	-	-	-	-	-	-	PORTC[1:0]		xxxx xxxx	
011	PIR1	-	-	-	-	-	-	CKMIF	ADCIF	---- --00	
014	EPIF0	External Pin Interrupt Flag								0000 0000	
01F	ADDLY /LEBPRL	LSB of ADC external trigger start delay counter threshold / multiplexed as leading edge blanking count threshold								0000 0000	
020-06F		SRAM BANK0 (80Bytes)								xxxx xxxx	
070-07F		SRAM BANK0 (16Bytes), physical address 0x70-0x7F								xxxx xxxx	

Table 14-3 SFR, BANK 0

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
080	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx
081	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx
082	PCL	LSB of Program Counter's (PC)								0000 0000
083	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx
084	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx
085	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx
086	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx
087	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx
088	BSREG	Bank Selection Register								xxxx xxxx
089	WREG	Working register W								xxxx xxxx
08A	PCLATH	-	MSB of Program counter(PC) latches							-000 0000
08B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
08C	TRISA	TRISA[7:0]								1111 1111
08D	TRISB	TRISB[7:0]								1111 1111
08E	TRISC	-	-	-	-	-	-	TRISC[1:0]		---- --11
091	PIE1	-	-	-	-	-	-	CKMIE	ADCIE	---- --00
094	EPIE0	External pin interrupt enable								0000 0000
095	CKOCON	SYSON	CCORDY	DTYSEL		CCOSEL[2:0]			CCOEN	0010 0000
096	PCON	STKOVF	STKUNF	EMCF	IERRR	/MCLRR	/SRTF	/PORF	/BORF	qqqq qqqq
097	WDTCON	WDTPRE[2:0]			WDTPS[3:0]				SWDTEN	1110 1000
098	OSCTUNE	HIRC Clock Frequency Tuner								-xxx xxxx
099	OSCCON	MCKCF[3:0]				OSTS	HTS	LTS	SCS	0100x000
09A	PCKEN	-	-	UARTEN	-	TIM4EN	TIM2EN	TIM1EN	ADCEN	0000 0000
09B	ADRESL	ADC result register LSB								0000 0000
09C	ADRESH	ADC result register MSB								0000 0000
09D	ADCON0	-	CHS[2:0]			-	ADEX	GO/DONE	ADON	0000 0000
09E	ADCON1	ADFM	ADCS[2:0]			ADNREF[1:0]		ADPREF[1:0]		0000 0000
09F	ADCON2	ADINTREF[1:0]		ETGTYP[1:0]		ADDLY.8	ETGSEL[2:0]			0000 0000
0A0-0EF	SRAM BANK1 (80Bytes)									xxxx xxxx
0F0-0FF	SRAM BANK1 (16Bytes), access BANK0's physical address 0x70-0x7F									xxxx xxxx

Table 14-4 SFR, BANK 1

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
100	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx
101	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx
102	PCL	LSB of Program Counter's (PC)								0000 0000
103	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx
104	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx
105	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx
106	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx
107	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx
108	BSREG	Bank Selection Register								xxxx xxxx
109	WREG	Working register W								xxxx xxxx
10A	PCLATH	-	MSB of Program counter(PC) latches							-000 0000
10B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
10C	LATA	LATA[7:0]								xxxx xxxx
10D	LATB	LATB[7:0]								xxxx xxxx
10E	LATC	LATC[7:0]								xxxx xxxx
10E	LATC	-	-	-	-	-	-	LATC[1:0]		---- --xx
111	TIM4CR1	T4ARPE	-	T4CKS[1:0]		T4OPM	T4URS	T4UDIS	T4CEN	0-00 0000
112	TIM4IER	-	-	-	-	-	-	-	T4UIE	---- --0
113	TIM4SR	-	-	-	-	-	-	-	T4UIF	---- --0
114	TIM4EGR	-	-	-	-	-	-	-	T4UG	---- --0
115	TIM4CNTR	T4CNT[7:0]								0000 0000
116	TIM4PSCR	-	-	-	-	-	T4PSC[2:0]			---- -000
117	TIM4ARR	T4ARR[7:0]								1111 1111
118	EPS0	EPS0[7:0]								0000 0000
119	EPS1	EPS1[7:0]								0000 0000
11A	PSRC0	PSRCA[7:0]								1111 1111
11B	PSRC1	PSRCB[7:0]								1111 1111
11C	PSRC2					PSRCC[3:2]		PSRCC[1:0]		---- 1111
11E	ITYPE0	ITYPE0[7:0]								0000 0000
11F	ITYPE1	ITYPE1[7:0]								0000 0000
120-16F	SRAM BANK2 (80Bytes)								xxxx xxxx	
170-17F	SRAM BANK2 (16Bytes), access BANK0's physical address 0x70-0x7F								xxxx xxxx	

Table 14-5 SFR, BANK 2

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
180	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx
181	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx
182	PCL	LSB of Program Counter's (PC)								0000 0000
183	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx
184	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx
185	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx
186	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx
187	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx
188	BSREG	Bank Selection Register								xxxx xxxx
189	WREG	Working register W								xxxx xxxx
18A	PCLATH	-	MSB of Program counter(PC) latches							-000 0000
18B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
18C	WPUA	WPUA[7:0]								0000 0000
18D	WPUB	WPUB[7:0]								0000 0000
18E	WPUC	-	-	-	-	-	-	WPUC[1:0]		---- --00
191	EEADRL	EEADR[7:0]								0000 0000
192	EEADRH	-	-	-	-	EEADR[11:8]				-000 0000
193	EEDATL	EEDAT[7:0]								xxxx xxxx
194	EEDATH	-	EEDAT[13:8]							-xxx xxxx
195	EECON1	EEPGD	CFGS	-	FREE	WRERR	WREN	WR	RD	00-0x000
196	EECON2	EEPROM Control Register 2								xxxx xxxx
197	ANSELA	Analog Pin Setting Register								0000 0000
199	LVDCON	SLVREN	LVDM	-	LVDEN	LVDW	LVDL[3:0]			0000 0000
19A	PSINK0	PSINK0[7:0]								0000 0000
19B	PSINK1	PSINK1[7:0]								0000 0000
19C	PSINK2	-	-	-	-	-	-	PSINK2[1:0]		---- --00
19D	MISC0	-	-	-	-	-	-	WCKSEL[1:0]		---- --00
19E	AFP0	-	-	AFP0[5:1]					-	--00 000-
19F	AFP1	-	-	AFP1[5:0]					-	---00 0000
1A0-1EF		SRAM BANK3 (80Bytes)								xxxx xxxx
1F0-1FF		SRAM BANK3 (16Bytes), access BANK0's physical address 0x70-0x7F								xxxx xxxx

Table 14-6 SFR, BANK3

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
200	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
201	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
202	PCL	LSB of Program Counter's (PC)								0000 0000	
203	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
204	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
205	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
206	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
207	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
208	BSREG	Bank Selection Register								xxxx xxxx	
209	WREG	Working register W								xxxx xxxx	
20A	PCLATH	-	MSB of Program counter(PC) latches								-000 0000
20B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
20C	WPDA	WPDA[7:0]								0000 0000	
20D	WPDB	WPDB[7:0]								0000 0000	
20E	WPDC	-	-	-	-	-	-	WPDC[1:0]		---- --00	
211	TIM1CR1	T1ARPE	T1CMS[1:0]		TIDIR	T1OPM	TIURS	T1UDS	T1CEN	0000 0000	
212	TIM1CR2	T1ENCTRL	-	-	-	-	T1COMS	-	T1CCPC	0--- -0-0	
213	TIM1SMCR	-	T1TS[2:0]			-	T1SMS[2:0]			-000 -000	
215	TIM1IER	T1BIE	T1TIE	T1COMIE	T1CC4IE	T1CC3IE	T1CC2IE	T1CC1IE	T1UIE	0000 0000	
216	TIM1SR1	T1BIF	T1TIF	T1COMIF	T1CC4IF	T1CC3IF	T1CC2IF	T1CC1IF	T1UIF	0000 0000	
217	TIM1SR2	-	-	-	T1CC4OF	T1CC3OF	T1CC2OF	T1CC1OF	-	---0 000-	
218	TIM1EGR	T1BG	T1TG	T1COMG	T1CC4G	T1CC3G	T1CC2G	T1CC1G	T1UG	0000 0000	
219	TIM1CCMR1 (output mode)	T1OC1CE	T1OC1M[2:0]			T1OC1PE	T1OC1FE	T1CC1S[1:0]		0000 0000	
	TIM1CCMR1 (input mode)	T1IC1F[3:0]				T1IC1PSC[1:0]		T1CC1S[1:0]		0000 0000	
21A	TIM1CCMR2 (output mode)	T1OC2CE	T1OC2M[2:0]			T1OC2PE	T1OC2FE	T1CC2S[1:0]		0000 0000	
	TIM1CCMR2 (input mode)	T1IC2F[3:0]				T1IC2PSC[1:0]		T1CC2S[1:0]		0000 0000	
21B	TIM1CCMR3 (output mode)	T1OC3CE	T1OC3M[2:0]			T1OC3PE	T1OC3FE	T1CC3S[1:0]		0000 0000	
	TIM1CCMR3 (input mode)	T1IC3F[3:0]				T1IC3PSC[1:0]		T1CC3S[1:0]		0000 0000	
21C	TIM1CCMR4 (output mode)	T1OC4CE	T1OC4M[2:0]			T1OC4PE	T1OC4FE	T1CC4S[1:0]		0000 0000	
	TIM1CCMR4 (input mode)	T1IC4F[3:0]				T1IC4PSC[1:0]		T1CC4S[1:0]		0000 0000	
21D	TIM1CCER1	T1CC2NP	T1CC2NE	T1CC2P	T1CC2E	T1CC1NP	T1CC1NE	T1CC1P	T1CC1E	0000 0000	
21E	TIM1CCER2	T1GP	T1SMOD	T1CC4P	T1CC4E	T1CC3NP	T1CC3NE	T1CC3P	T1CC3E	0000 0000	
21F	ODCON0	-	-	-	-	-	-	-	UROD	---- --0	
220–26F		SRAM BANK4 (80Bytes)								xxxx xxxx	
270–27F		SRAM BANK4 (16Bytes), access BANK0's physical address 0x70–0x7F								xxxx xxxx	

Table 14-7 SFR, BANK4

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
280	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
281	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
282	PCL	LSB of Program Counter's (PC)								0000 0000	
283	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
284	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
285	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
286	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
287	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
288	BSREG	Bank Selection Register								xxxx xxxx	
289	WREG	Working register W								xxxx xxxx	
28A	PCLATH	-	MSB of Program counter(PC) latches								-000 0000
28B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
28C	TIM1CNTRH	T1CNT[15:8]								0000 0000	
28D	TIM1CNTRL	T1CNT[7:0]								0000 0000	
28E	TIM1PSCRH	T1PSC[15:8]								0000 0000	
28F	TIM1PSCRL	T1PSC[7:0]								0000 0000	
290	TIM1ARRH	T1ARR[15:8]								1111 1111	
291	TIM1ARRL	T1ARR[7:0]								1111 1111	
292	TIM1RCR	T1REP[7:0]								0000 0000	
293	TIM1CCR1H	T1CCR1[15:8]								0000 0000	
294	TIM1CCR1L	T1CCR1[7:0]								0000 0000	
295	TIM1CCR2H	T1CCR2[15:8]								0000 0000	
296	TIM1CCR2L	T1CCR2[7:0]								0000 0000	
297	TIM1CCR3H	T1CCR3[15:8]								0000 0000	
298	TIM1CCR3L	T1CCR3[7:0]								0000 0000	
299	TIM1CCR4H	T1CCR4[15:8]								0000 0000	
29A	TIM1CCR4L	T1CCR4[7:0]								0000 0000	
29B	TIM1BKR	T1MOE	T1AOE	T1BKP	T1BKE	T1OSSR	T1OSSI	T1LOCK[1:0]		0000 0000	
29C	TIM1DTR	T1DGT[7:0]								0000 0000	
29D	TIM1OISR	-	T1OIS4	T1OIS3N	T1OIS3	T1OIS2N	T1OIS2	T1OIS1N	T1OIS1	-000 0000	
29E	TIM2CCR3H	T2CCR3[15:8]								0000 0000	
29F	TIM2CCR3L	T2CCR3 [7:0]								0000 0000	
2A0–2EF		SRAM BANK5 (80Bytes)								xxxx xxxx	
2F0–2FF		SRAM BANK5 (16Bytes), access BANK0's physical address 0x70–0x7F								xxxx xxxx	

Table 14-8 SFR, BANK5

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
300	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
301	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
302	PCL	LSB of Program Counter's (PC)								0000 0000	
303	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
304	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
305	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
306	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
307	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
308	BSREG	Bank Selection Register								xxxx xxxx	
309	WREG	Working register W								xxxx xxxx	
30A	PCLATH	-	MSB of Program counter(PC) latches								-000 0000
30B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
30C	TIM2CR1	T2ARPE	-	-	-	T2OPM	T2URS	T2UDIS	T2CEN	0--- 0000	
30D	TIM2IER	-	-	-	-	T2CC3IE	T2CC2IE	T2CC1IE	T2UIE	---- 0000	
30E	TIM2SR1	-	-	-	-	T2CC3IF	T2CC2IF	T2CC1IF	T2UIF	---- 0000	
30F	TIM2SR2	-	-	-	-	T2CC3OF	T2CC3OF	T2CC3OF	-	---- 000-	
310	TIM2EGR	-	-	-	-	T2CC3G	T2CC2G	T2CC1G	T2UG	---- 0000	
311	TIM2CCMR1 (output mode)	-	T2OC1M[2:0]			T2OC1PE	-	T2CC1S[1:0]		-000 0-00	
	TIM2CCMR1 (input mode)	T2IC1F[3:0]				T2IC1PSC[1:0]		T2CC1S[1:0]		0000 0000	
312	TIM2CCMR2 (output mode)	-	T2OC2M[2:0]			T2OC2PE	-	T2CC2S[1:0]		-000 0-00	
	TIM2CCMR2 (input mode)	T2IC2F[3:0]				T2IC2PSC[1:0]		T2CC2S[1:0]		0000 0000	
313	TIM2CCMR3 (output mode)	-	T2OC3M[2:0]			T2OC3PE	-	T2CC3S[1:0]		-000 0-00	
	TIM2CCMR3 (input mode)	T2IC3F[3:0]				T2IC3PSC[1:0]		T2CC3S[1:0]		0000 0000	
314	TIM2CCER1	-	-	T2CC2P	T2CC2E	-	-	T2CC1P	T2CC1E	--00 --00	
315	TIM2CCER2	-	-	-	-	-	-	T2CC3P	T2CC3E	---- --00	
316	TIM2CNTRH	T2CNT[15:8]								0000 0000	
317	TIM2CNTRL	T2CNT[7:0]								0000 0000	
318	TIM2PSCR	-	-	-	-	T2PSC[3:0]				---- 0000	
319	TIM2ARRH	T2ARR[15:8]								1111 1111	
31A	TIM2ARRL	T2ARR[7:0]								1111 1111	
31B	TIM2CCR1H	T2CCR1[15:8]								0000 0000	
31C	TIM2CCR1L	T2CCR1[7:0]								0000 0000	
31D	TIM2CCR2H	T2CCR2[15:8]								0000 0000	
31E	TIM2CCR2L	T2CCR2[7:0]								0000 0000	
31F	TCKSRC	LFMOD	T2CKSRC[2:0]			-	T2CKSRC[2:0]			0000 -000	
320–32F		SRAM BANK6 (16Bytes)								xxxx xxxx	
370–37F		SRAM BANK6 (16Bytes), access BANK0's physical address 0x70–0x7F								xxxx xxxx	

Table 14-9 SFR, BANK6

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
380	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
381	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
382	PCL	LSB of Program Counter's (PC)								0000 0000	
383	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
384	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
385	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
386	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
387	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
388	BSREG	Bank Selection Register								xxxx xxxx	
389	WREG	Working register W								xxxx xxxx	
38A	PCLATH	-	MSB of Program counter(PC) latches								-000 0000
38B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
3F0-3FF		SRAM BANK7 (16Bytes), access BANK0's physical address 0x70-0x7F								xxxx xxxx	

Table 14-10 SFR, BANK7

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset	
400	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx	
401	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx	
402	PCL	LSB of Program Counter's (PC)								0000 0000	
403	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx	
404	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx	
405	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx	
406	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx	
407	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx	
408	BSREG	Bank Selection Register								xxxx xxxx	
409	WREG	Working register W								xxxx xxxx	
40A	PCLATH	-	MSB of Program counter(PC) latches								-000 0000
40B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000	
41A	ADCON3	ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	LEBADT	-	ELVDS[1:0]		0000 0-00	
41B	ADCMPPH	ADCMPPH[7:0]								0000 0000	
41C	LEBCON	LEBEN	LEBCH[1:0]		-	EDGS	BKS[2:0]		000- 0000		
41D	MSCKCON	-	-	-	-	-	-	CKMAVG	CKCNTI	---- --01	
41E	SOSCPR	SOSCPR[7:0]								1111 1111	
41F	SOSCPRH	-	-	-	-	SOSCPR[11:8]				---- 1111	
470-47F		SRAM BANK8 (16Bytes), access BANK0's physical address 0x70-0x7F								xxxx xxxx	

Table 14-11 SFR, BANK8

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
480	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx
481	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx
482	PCL	LSB of Program Counter's (PC)								0000 0000
483	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx
484	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx
485	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx
486	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx
487	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx
488	BSREG	Bank Selection Register								xxxx xxxx
489	WREG	Working register W								xxxx xxxx
48A	PCLATH	-	MSB of Program counter(PC) latches							-000 0000
48B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
48C	URDATAL	DATA[7:0]								0000 0000
48D	URDATAH	-							DATAH	---- --0
48E	URIER	-	-	TCEN	-	IDELE	RXSE	URTE	URRXNE	--0- 0000
48F	URLCR	-	BKREQ	-	EVEN	PEN	URSTOP	-	LTH	-0-0 00-0
490	URLCREXT	-	-	-	-	-	-	RWU	EXTEN	---- --00
491	URMCR	-	-	SIRLP	TXEN	RXEN	WAKE	HDSSEL	SIREN	--00 0000
492	URLSR	ADDRF	IDLEF	TXEF	BKF	FEF	PEF	OVERF	RXNEF	0000 0000
493	URRAR	-	-	-	-	RAR[3:0]			----	0000
494	URDLL	DLL[7:0]								0000 0000
495	URDLH	DLH[7:0]								0000 0000
496	URABCR	-	-	-	-	ABRE	ABRM	ABRF	ABREN	---- 0000
497	URSYNCR	-	-	-	-	LBCL	URCPHA	URCPOL	SYNEN	---- 0000
498	URLINCR	-	-	-	LINEN	BLTH[3:0]			---	0000
499	URSDCR0	-	NACK	CKOE	SDEN	-	-	-	-	-000 0000
49A	URSDCR1	GT[7:0]								0000 0000
49B	URSDCR2	PSC[7:0]								0000 0000
49C	URTC	-	-	-	-	-	-	-	TCF	---- --1
4F0-4FF		SRAM BANK9 (16Bytes), access BANK0's physical address 0x70-0x7F								xxxx xxxx

Table 14-12 SFR, BANK9

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
500	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx
501	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx
502	PCL	LSB of Program Counter's (PC)								0000 0000
503	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx
504	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx
505	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx
506	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx
507	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx
508	BSREG	Bank Selection Register								xxxx xxxx
509	WREG	Working register W								xxxx xxxx
50A	PCLATH	-	MSB of Program counter(PC) latches							---0 0000
50B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
570-57F	SRAM BANK10 (16Bytes), access BANK0's physical address 0x70-0x7F									xxxx xxxx

Table 14-13 SFR, BANK10

Addr.	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
F80	INDF0	Addressing this location uses contents of FSR0 to address data memory (not a physical register)								xxxx xxxx
F81	INDF1	Addressing this location uses contents of FSR1 to address data memory (not a physical register)								xxxx xxxx
F82	PCL	LSB of Program Counter's (PC)								0000 0000
F83	STATUS	-	-	-	/TO	/PD	Z	DC	C	0001 1xxx
F84	FSR0L	LSB of indirect addressing pointer register FSR0								xxxx xxxx
F85	FSR0H	MSB of indirect addressing pointer register FSR0								xxxx xxxx
F86	FSR1L	LSB of indirect addressing pointer register FSR1								xxxx xxxx
F87	FSR1H	MSB of indirect addressing pointer register FSR1								xxxx xxxx
F88	BSREG	Bank Selection Register								xxxx xxxx
F89	WREG	Working register W								xxxx xxxx
F8A	PCLATH	-	MSB of Program counter(PC) latches							-000 0000
F8B	INTCON	GIE	PEIE	EEIE	LVDIE	OSFIE	EEIF	LVDIF	OSFIF	0000 0000
FE4	STATUS_SHAD	STATUS shadow register								xxxx xxxx
FE5	WREG_SHAD	WREG shadow register								xxxx xxxx
FE6	BSREG_SHAD	BSREG shadow register								xxxx xxxx
FE7	PCLATH_SHAD	PCLATH shadow register								xxxx xxxx
FE8	FSR0L_SHAD	FSR0L shadow register								xxxx xxxx
FE9	FSR0H_SHAD	FSR0H shadow register								xxxx xxxx
FEA	FSR1L_SHAD	FSR1L shadow register								xxxx xxxx
FEB	FSR1H_SHAD	FSR1H shadow register								xxxx xxxx
FEC	-	-								-
FED	STKPTR	STKPTR								xxxx xxxx
FEE	TOSL	TOSL								xxxx xxxx
FEF	TOSH	TOSH								xxxx xxxx
FF0-FFF		SRAM BANK31 (16Bytes), access BANK0's physical address 0x70-0x7F								xxxx xxxx

Table 14-14 SFR, BANK31

Notes:

1. INDF is not a physical register;
2. Gray parts indicate not used;
3. Do not write to unimplemented register bits

14.3. STATUS Register

Name	Status	Register	Addr.	Reset
/TO	<u>Time-out Flag</u> 1 = CLRWDT or SLEEP instruction after Power-up 0 = WDT time-out occurred	STATUS[4]	Bank First address + 0x03	RO-1
/PD	<u>Power-down Flag</u> 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction	STATUS[3]		RO-1
Z	<u>Zero: Result of an arithmetic or logic operation is zero Flag</u> 1 = Yes 0 = No	STATUS[2]		RW-x
DC	<u>Half carry/half borrow: Half Carry-Over or Borrow from the 4th low-order bit of the result</u> 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[1]		RW-x
C	<u>Carry/borrow: Digit Carry-Over or Borrow from MSB of the result</u> 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[0]		RW-x

Table 14-15 STATUS register

Notes:

1. The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, HC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.
2. It is recommended, therefore, that only BCR, BSR, SWAPR and STR instructions are used to alter the STATUS register.

14.4. Stack

FT61E14x has a hardware stack of 16 levels deep x 15 bits wide. The stack space is independent of program PROM, data EEPROM or data storage area SRAM.

TOSH:TOSL points to the top of the stack, and STKPTR is the current value of the stack pointer. When accessing the stack, the STKPTR value used to locate TOSH:TOSL can be tuned and then read/write operations can be performed on TOSH:TOSL.

During normal program operation, LCALL, CALLW, and interrupts increment the STKPTR value by 1, and the PC value is pushed onto the stack. When the RETW, RET and RETI instructions are executed, the PC value is popped from the stack and the STKPTR value is decremented by 1. The PCLATH value is not affected by push or pop operations. Available stack space can be viewed by reading STKPTR .

STKPTR is 5 bits, allowing detection of overflow and underflow. Performing a push operation after filling 16 levels will result in an overflow and the STKOVF flag will be set to 1. After popping the first level and then performing the pop operation, an underflow will occur, and the STKUNF flag will be set to 1. An overflow or underflow event will cause the system to reset, and the 16-level stack will all be cleared to 0.

Note: Be careful when modifying STKPTR with interrupts enabled.

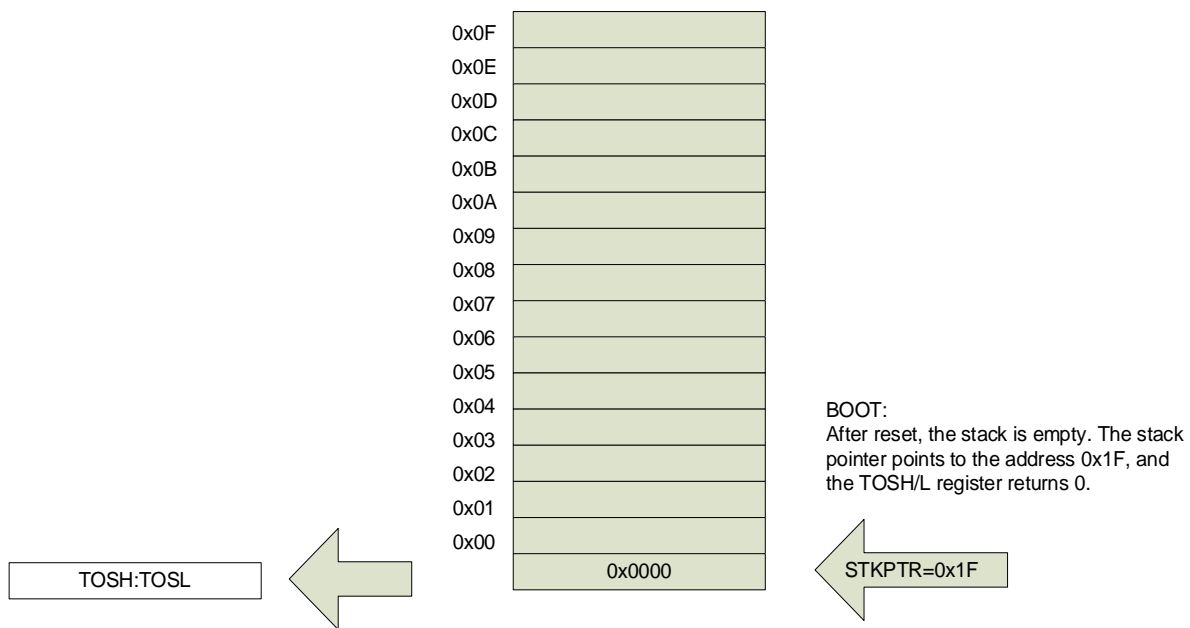


Figure 14-2 Software Access Stack

14.5. Indirect addressing

INDFn is not a physically register, and addressing INDFn will result in indirect addressing. Any instruction that accesses the INDFn register actually accesses the unit pointed to by the File Selection Register (FSRn) . An indirect READ of INDF will return 0, and an indirect WRITE of INDF will result in a NOP (possibly affecting the status flags). FSRnH : The 16-bit address composed of FSRnL allows 65536 address units to be addressed, which can be divided into 3 memory areas:

- Conventional data memory
- Linear data memory
- Flash

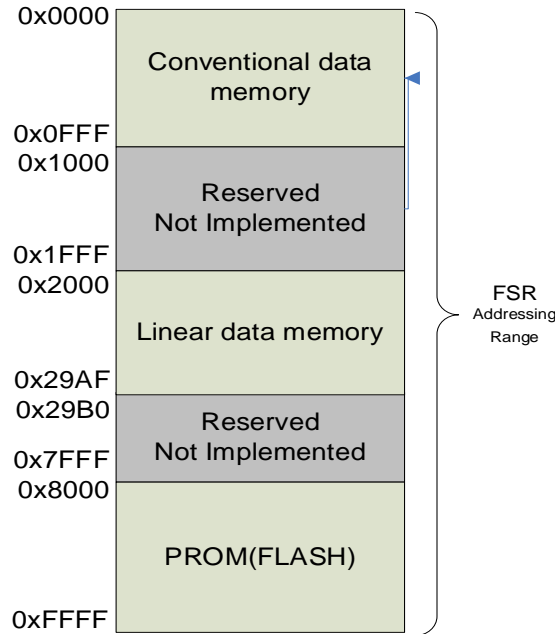


Figure 14-3 Indirect addressing

14.5.1. Conventional data memory

Conventional data memory, i.e. user register, with an address range of 0x0000 ~ 0x0FFF, correspond to the absolute addresses of all SFRs and SRAMs.

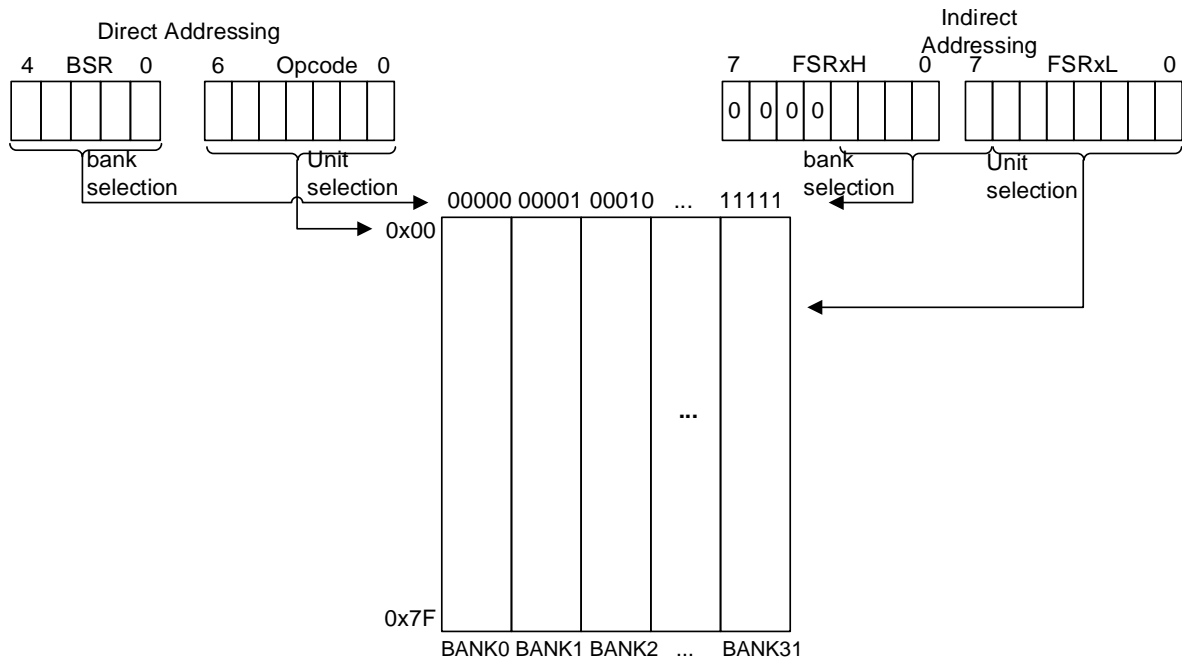


Figure 14-4 Conventional Data Memory Mapping

14.5.2. Linear data memory

Linear data memory with an address range of 0x2000 ~0x29AF, is a virtual array, pointing to the 80-byte SRAM storage area in all Banks (excluding the 16 -byte common SRAM), the unused memory area (Bank 6 ~30) is read as 0x00 .

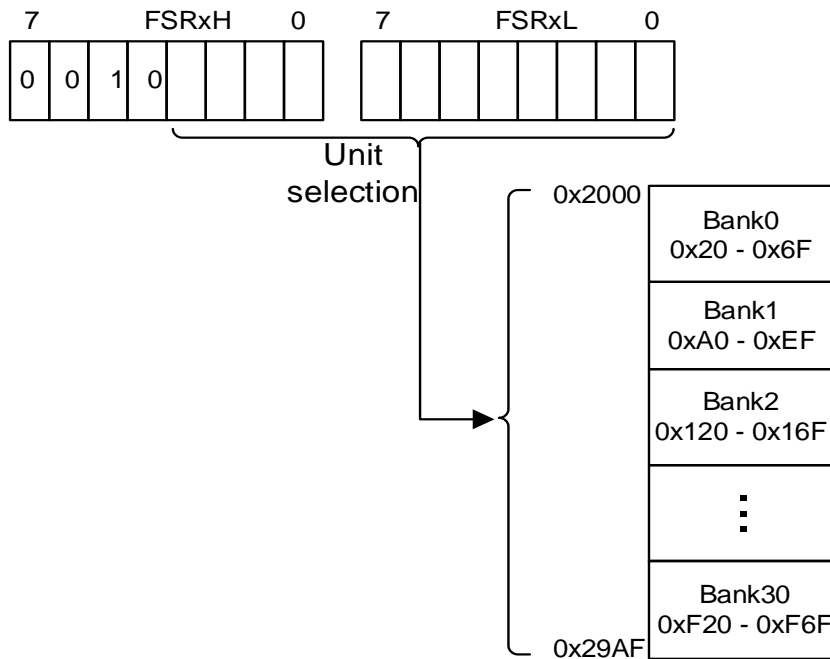


Figure 14-5 Linear Data Memory Mapping

14.5.3. Flash program memory

When the MSB of FSRnH is set to 1, the lower 15 bits of FSRnH:FSRnL are the address of the program PROM memory that needs to be accessed, and the corresponding lower 8-bit data can be read through INDFn. The program PROM cannot be written through FSR/INDF, while the read operation requires 2 instruction cycles.

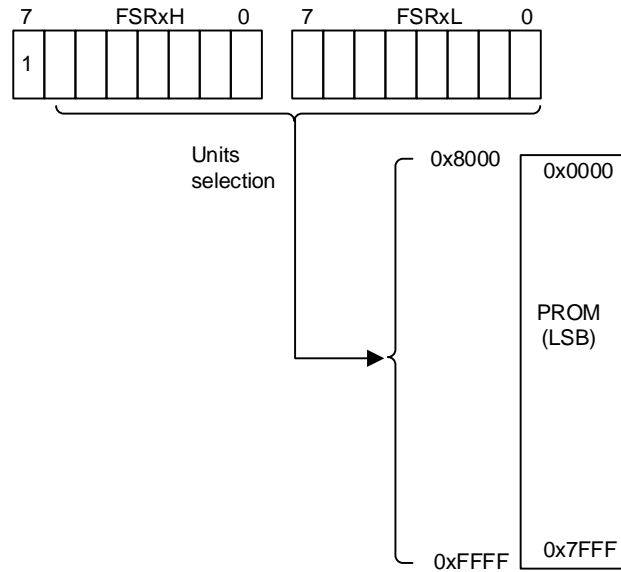


Figure 14-6 Program Memory Mapping

The constants in the program PROM memory can be accessed indirectly via FSR or read via the RETW instruction.

Program example for indirect access via FSR.

```

constants
RETW DATA0          ; Index0 data
RETW DATA1          ; Index1 data
RETW DATA2
RETW DATA3
my_function
...                  ; lots of code...
LDWI LOW constants
STR FSR1L
LDWI HIGH constants
STR FSR1H
MOVIW 0[FSR1]        ; The program memory is in W
    
```

Program Example to read the constant table with RETW and BRW instructions:

```

constants
BRW                  ;Add Index in W to program counter to ;select data
RETW DATA0          ; Index0 data
RETW DATA1          ; Index1 data
RETW DATA2
RETW DATA3
my_function
...                  ; lots of code...
LDWI DATA_INDEX
call constants        ; the constant is in W
    
```

15. INSTRUCTION SET

Assembly Syntax	Function	Operation	Instruction cycles	Status
NOP	No operation	None	1	NONE
SLEEP	Enter SLEEP mode	0 → WDT; Stop OSC	1	/PF, /TF
RESET	Software Reset	Reset register PCON	1	NONE
CLRWDT	Clear WDT	0 → WDT	1	/PF, /TF
LJUMP N	Unconditional long jump	N → PC	2	NONE
BRA k	Relative Branch (address range is limited)	PC + 1 + k → PC	2	NONE
BRW	Make a relative jump with the value of register W as an offset	PC + w → PC	2	NONE
LCALL N	Long CALL Subroutine	N → PC; PC + 1 → Stack	2	NONE
CALLW	Call subroutine whose address is specified by register W	W → PC; PC + 1 → Stack	2	NONE
RETW	Transmit immediate I to W and return	I → W, Stack → PC	2	NONE
RETI	Return from Interrupt	Stack → PC; 1 → GIE	2	NONE
RET	Return from Subroutine	Stack → PC	2	NONE
BCR R, b	Clear b bit in register R	0 → R(b)	1	NONE
BSR R, b	Set b bit in register R	1 → R(b)	1	NONE
CLRR R	Clear Register	0 → R	1	Z
LDR R, d (MOVf)	Load Register to d	R → d	1	Z
COMR R, d	Complement Register	/R → d	1	Z
INCR R, d	Increment Register	R + 1 → d	1	Z
INCRSZ R, d	Increment Register, Skip if 0	R + 1 → d	1	NONE
DECR R, d	Decrement Register	R-1 → d	1	Z
DECRSZ R, d	Decrement Register, Skip if 0	R-1 → d	1	NONE
SWAPR R, d	Swap Halves Register	R(0-3)R(4-7) → d	1	NONE
RRR R, d	R moves to the right with a carry loop	R(0) → C; R(n) → R(n-1); C → R(7);	1	C
RLR R, d	R moves to the left with a carry loop	R(7) → C; R(n) → R(n+1); C → R(0);	1	C
LSRF f, d	F Logical Right Shift	0 → f(7); f(n+1) → R(n); f(0) → C;	1	C, Z
LSLF f, d	F logical Left Shift	f(7) → C; f(n) → R(n+1); 0 → R(0);	1	C, Z
ASRF f, d	Arithmetic Right Shift	f(7) → R(7); f(n+1) → R(n); f(0) → C;	1	C, Z

Assembly Syntax	Function	Operation	Instruction cycles	Status
BTSC R, b	Bit Test, Skip if 0	Skip if R(b)=0	1	NONE
BTSS R, b	Bit Test, Skip if 1	Skip if R(b)=1	1	NONE
CLRW	Clear Working Register	$0 \rightarrow W$	1	Z
STR R (MOVWF)	Store W to Register	$W \rightarrow R$	1	NONE
ADDWR R, d	Add W and Register	$W + R \rightarrow d$	1	C, DC, Z
ADDWFC R, d	ADD W and R with CARRY bit	$W + R + C \rightarrow d$	1	C, DC, Z
SUBWR R, d	Subtract W from Register	$R - W \rightarrow d$	1	C, DC, Z
SUBWFB R, d	Subtract W from Register (with BORROW bit)	$R - W - (/B) \rightarrow d$	1	C, DC, Z
ANDWR R, d	AND W and Register	$R \& W \rightarrow d$	1	Z
IORWR R, d	OR W and Register	$W R \rightarrow d$	1	Z
XORWR R, d	XOR W and register	$W \wedge R \rightarrow d$	1	Z
LDWI I (MOVLW)	Load Immediate to W	$I \rightarrow W$	1	NONE
ANDWI I	AND W and imm	$I \& W \rightarrow W$	1	Z
IORWI I	OR W and imm	$I W \rightarrow W$	1	Z
XORWI I	XOR W and imm	$I \wedge W \rightarrow W$	1	Z
ADDWI I	Add imm to W	$I + W \rightarrow W$	1	C, DC, Z
SUBWI I	Subtract W from imm	$I - W \rightarrow W$	1	C, DC, Z
RETW I	Return, Place imm to W	Stack \rightarrow PC; $I \rightarrow W$		NONE
MOVLBk	Move imm I to BSR	$K \rightarrow BSR$	1	NONE
ADDFSR FSRn, k	Add imm k to FSRn	$FSRn + k \rightarrow FSRn$	1	NONE
MOVLP	Move k to PCLATH	$k \rightarrow PCLATH$	1	NONE
MOVIW mm	Move FSRn to W	$FSRn \rightarrow W$	1	Z
MOVWI mm	Move W to FSRn	$W \rightarrow FSRn$	1	NONE

Table 15-1 49 Instruction Commands

Field	Descriptions	
R(f)	SFR/SRAM Address	
W	Working Register	
b	Bit address within the 8-bit Register / RAM	
I/Imm (k)	Immediate data	
x	Don't care, may be 0 or 1	
d	<u>Destination select</u>	1 = Store result in Register / RAM 0 = Store result in W
mm	Pre/post increment/decrement mode selection (++FSRn, --FSRn, FSRn++, FSRn--,	

Field	Descriptions
	k[FSRn])
N	Absolute address of program
PC	Program Counter
/PD	Power-Down Flag
/TO	Time-Out Flag
C	Carry/Borrow bit
DC	Half Carry/Half Borrow bit
Z	Zero Flag

Table 15-2 OpCode Field

Name	Status	Register	Addr.	Reset
Z	<u>Zero Bit: Result of an arithmetic or logic operation is zero Flag</u> 1 = Yes 0 = No	STATUS[2]	Bank First address+0x03	RW-x
DC	<u>Half Carry (ADDWR, ADDWI, SUBWI, SUBWR): Digit Carry-Over or Borrow from the 4th low-order bit of the result</u> 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[1]		RW-x
C	<u>Carry (ADDWR, ADDWI, SUBWI, SUBWR): Digit Carry-Over or Borrow from MSB of the result</u> 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[0]		RW-x

Table 15-3 Computational Status Flags

15.1. Read-Modify-Write (RMW) Instructions

All instructions that need to use the file register (the instructions with the mnemonic R in [Table 15-1](#)) will perform the read-modify-write (RMW) operation, that is, first take out the contents of the target register, modify the data according to the instruction, and then write the data back to the target register or W (depending on d and specific instruction) .

For example:

```
BSR    FSR0L, 0;
```

The execution process of the above instructions in the CPU is as follows:

- 1) Read out FSR0L to the temporary register T;
- 2) Set register T or "0000 0001" to form new data;
- 3) Write the new data back to FSR0L;

15.2. Instruction details

ADDFSR	Add Immediate to FSRn
Syntax:	[label] ADDFSR FSRn, k
Operands:	-32 ≤ k ≤ 31 n ∈ [0,1]
Operation:	FSR(n)+k → FSR(n)
Status Affected:	None
Description:	The signed 6-bit immediate 'k' is added to the contents of the FSRnH:FSRnL register pair. FSRn is limited to the range 0000h - FFFFh. Moving beyond these bounds will cause the FSR to wrap-around..

ANDWI	AND Immediate with W
Syntax:	[label] ANDWI k
Operands:	0 ≤ k ≤ 255
Operation:	(W).AND.(k) → (W)
Status Affected:	Z
Description:	Perform a logical AND operation on the contents of the W register and the 8-bit immediate k. The result is stored in the W register.

ADDWI	Add Immediate to W
Syntax:	[label] ADDWI k
Operands:	0 ≤ k ≤ 255
Operation:	(W)+k → (W)
Status Affected:	C, DC, and Z
Description:	The contents of the W register are added to the 8-bit immediate 'k' and the result is placed in the W register.

ANDWR	AND W with f
Syntax:	[label] ANDWR f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W).AND.(f) → (destination register)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ADDWR	Add W and f
Syntax:	[label]ADDWR f,d
Operands:	0≤f≤127 d ∈ [0,1]
Operation:	(W)+(f)→(destination register)
Status Affected:	C, DC, and Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ASRF Arithmetic Right Shift

Syntax: [label] ASRF f {,d}
 Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
 Operation: $(f[7]) \rightarrow \text{dest}[7]$
 $(f[7:1]) \rightarrow \text{dest}[6:0]$,
 $(f[0]) \rightarrow C$
 Status Affected: C and Z
 Description: The contents of register 'f' are shifted one bit to the right through the Carry flag. The MSb remains unchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



BRA Relative Branch

Syntax: [label] BRA label
 Operands: [label] BRA \$+k
 Operands: $-256 \leq \text{label} - \text{PC} + 1 \leq 255$
 $-256 \leq k \leq 255$
 Operation: $(\text{PC}) + 1 + k \rightarrow \text{PC}$
 Status Affected: None
 Description: Add the signed 9-bit immediate 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $\text{PC} + 1 + k$. This instruction is a 2-cycle instruction. This branch has a limited range.

ADDWFC Add W to f (with Carry bit)

Syntax: [label] ADDWFC f {,d}
 Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
 Operation: $(W) + (f) + (C) \rightarrow \text{destination register}$
 Status Affected: C, DC, and Z
 Description: Add the content of W, the carry bit and the content of register f. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored in register f.

BRW Relative Branch with W

Syntax: [label] BRW
 Operands: none
 Operation: $(\text{PC}) + (W) \rightarrow \text{PC}$
 Status Affected: None
 Description: Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $\text{PC} + 1 + (W)$. This instruction is a 2-cycle instruction.

BCR Bit Clear f

Syntax: [label] BCR f, b
 Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$
 Operation: $0 \rightarrow (f[b])$
 Status Affected: None
 Description: Bit 'b' in register 'f' is cleared.

BSR Bit Set f

Syntax: [label] BSR f, b
 Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$
 Operation: $1 \rightarrow (f[b])$
 Status Affected: None
 Description: Bit 'b' in register 'f' is set.

BTSC Bit Test f, Skip if Clear

Syntax: [label] BTSC f,b
 Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$
 Action: Skip if (f[b])=0
 Status Affected: None
 Description: If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

Syntax: [label] LCALL k
 Operands: $0 \leq k \leq 2047$
 Operation: $(PC)+1 \rightarrow TOS$,
 $k \rightarrow PC[10:0]$,
 $(PCLATH[4:3]) \rightarrow PC[12:11]$
 Status Affected: None
 Description: Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. LCALL is a 2-cycle instruction.

BTSS Bit Test f, Skip if 1

Syntax: [label] BTSS f,b
 Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$
 Action: Skip if (f[b])=1
 Status Affected: None
 Description: If bit b of register f is 0, execute the next instruction. If bit b is 1, the next instruction is discarded and a NOP is executed instead, making the instruction a two-cycle instruction.

CLRR Clear f

Syntax: [label] CLRR f
 Operands: $0 \leq f \leq 127$
 Operation: $00h \rightarrow (f)$
 $1 \rightarrow Z$
 Status Affected: Z
 Description: The contents of register 'f' are cleared and the Z bit is set.

CLRW Clear W

Syntax: [label] CLRW
 Operands: none
 Operation: $00h \rightarrow (W)$
 $1 \rightarrow Z$
 Status Affected: Z
 Description: W register is cleared. Zero bit (Z) is set.

LCALL Long CALL Subroutine

CALLW Subroutine Call With W

Syntax: [label] CALLW
Operands: none
Operation: (PC)+1→TOS,
(W)→PC[7:0],
(PCLATH[6:0])→PC[14:8]
Status Affected: None
Description: Subroutine call with W. First, the return address (PC + 1) is pushed onto the return stack. Then, the contents of W is loaded into PC<7:0>, and the contents of PCLATH into PC<14:8>. CALLW is a two-cycle instruction.

Syntax: [label] DECR f,d
Operands: 0≤f≤127
d ∈ [0,1]
Operation: (f)-1→(destination register)
Status Affected: Z
Description: Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

CLRWDT Clear Watchdog Timer

Syntax: [label] CLRWDT
Operands: none
Operation: 00h→WDT
0→WDT prescaler
1→/TO
1→/PD
Status Affected: /TO and /PD
Description: CLRWDT instruction resets the Watchdog Timer and its prescaler. Status bits /TO and /PD are both set.

DECRSZ Decrement f, Skip if 0

Syntax: [label]DECRSZ f,d
Operands: 0≤f≤127
d ∈ [0,1]
Operation: (f)-1→(destination register);
skip if result = 0
Status Affected: None
Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

COMR Complement f

Syntax: [label] COMR f,d
Operands: 0≤f≤127
d ∈ [0,1]
Operation: \bar{f} →(destination register)
Status Affected: Z
Description: The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

DECR Decrement f

LJUMP Unconditional Long JUMP

Syntax: [label] LJUMP k
Operands: $0 \leq k \leq 2047$
Operation: $k \rightarrow PC[10:0]$
 $PCLATH[4:3] \rightarrow PC[12:11]$
Status Affected: None
Description: LJUMP is an Long JUMP of N instruction. Loads bits[10:0] of the PC with an 11-bit immediate value. The upper bits of the PC are loaded from PCLATH[4:3]. LJUMP is a 2-cycle instruction.

Syntax: [label] IORWI k
Operands: $0 \leq k \leq 255$
Operation: $(W).OR.k \rightarrow (W)$
Status Affected: Z
Description: The contents of the W register are OR'ed with the 8-bit immediate 'k'. The result is placed in the W register.

INCR Increment f

Syntax: [label] INCR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f)+1 \rightarrow (\text{destination register})$
Status Affected: Z
Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

IORWR Inclusive OR W with f

Syntax: [label] IORWR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(W).OR.(f) \rightarrow (\text{destination register})$
Status Affected: Z
Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCRSZ Increment f, Skip if 0

Syntax: [label] INCRSZ f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f)+1 \rightarrow (\text{destination register}),$
 $\text{result}=0 \text{ skip}$
Status Affected: None
Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction..

LSLF Logical Left Shift

Syntax: [label] LSLF f {,d}
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f[7]) \rightarrow C$
 $(f[6:0]) \rightarrow \text{dest}[7:1]$
 $0 \rightarrow \text{dest}[0]$
Status Affected: C and Z
Description: The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



IORWI Inclusive OR immediate with W

LSRF Logical Right Shift

Syntax: [label] LSRF f {,d}
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $0 \rightarrow$ destination register[7]
 $(f[7:1]) \rightarrow$ destination register[6:0]
 $(f[0]) \rightarrow C$
Status Affected: C and Z
Description: The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



LDR Move f

Syntax: [label] LDR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f) \rightarrow$ (destination register)
Status Affected: Z
Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.
Words: 1
Cycles: 1
Example: LDR FSR, 0
 After Instruction
 W = value in FSR register
 Z = 1

Syntax: [label] MOVIW ++FSRn
 [label] MOVIW --FSRn
 [Label] MOVIW FSRn++
 [Label] MOVIW FSRn--
 [label] MOVIW k[FSRn]
Operands: $n \in [0,1]$
 $mm \in [00,01,10,11]$
 $-32 \leq k \leq 31$
Operation: $INDFn \rightarrow W$
 Valid address is determined by
 • FSR + 1 (preincrement)
 • FSR - 1 (predecrement)
 • FSR + k (relative offset)
 After the Move, the FSR value will be either:
 • FSR + 1 (all increments)
 • FSR - 1 (all decrements)
 • Unchanged

Status Affected: Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers(INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing /decrementing it beyond these bounds will cause it to wrap-around.

MOVIW Move INDFn to W

MOVWI Move INDFn to W

Syntax: [label] MOVWI ++FSRn
 [label] MOVWI --FSRn
 [label] MOVWI FSRn++
 [Label] MOVWI FSRn--
 [label] MOVWI k[FSRn]

Operands: n ∈ [0,1]
 mm ∈ [00,01,10,11]
 -32 ≤ k ≤ 31

Operation: W → INDFn
 Valid address is determined by:

- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:

- FSR + 1 (all increments)
- FSR - 1 (all decrements)
- Unchanged

Status Affected: None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

MOVLB Move Immediate to BSR

Syntax: [label] MOVLB k
Operands: 0 ≤ k ≤ 15
Operation: k → BSR
Status Affected: None
Description: The 5-bit immediate 'k' is loaded into the Bank Select Register (BSR).

MOVLP Move Immediate to PCLATH

Syntax: [label] MOVLP k
Operands: 0 ≤ k ≤ 127
Operation: k → PCLATH
Status Affected: None
Description: The seven-bit immediate 'k' is loaded into the PCLATH register.

LDWI Move Immediate to W

Syntax: [label] MOVWLW k
Operands: 0 ≤ k ≤ 255
Operation: k → (W)
Status Affected: None
Description: The eight-bit immediate 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1
Cycles: 1
Example: LDWI 0x5A
 After Instruction
 W = 0x5A

NOP No operation

Syntax: [label] NOP
Operands: none
Action: no-op
Status Affected: None
Description: No operation.
Words: 1
Cycles: 1
Example: NOP

STR Move W to f

Syntax: [label] STR f
Operands: $0 \leq f \leq 127$
Operation: (W) →(f)
Status Affected: None
Description: Transmit the data of the W register to the register f.
Words: 1
Cycles: 1
Example: STR OPTION
 Before Instruction
 OPTION = 0xFF
 W = 0x4F
 After Instruction
 OPTION = 0x4F
 W = 0x4F

Syntax: [label] RETI
Operands: none
Operation: TOS→PC,
 1→GIE
Status Affected: None
Description: Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words: 1 **Cycles:** 2
Example: RETI
 After interruption
 PC = TOS
 GIE = 1

RESET Software Reset

Syntax: [label] RESET
Operands: none
Action: Execute a device Reset. Resets the nRI flag of the PCON register.
Status Affected: None
Description: This instruction provides a way to execute a hardware Reset by software.

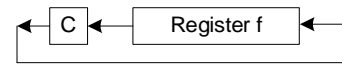
RLR Rotate Left f through Carry

Syntax: [label] RLR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: See description below
Status Affected: C
Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.

RET Return from Subroutine

Syntax: [label] RET
Operands: none
Operation: TOS→PC
Status Affected: None
Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

Words: 1 **Cycles:** 1
Example: RLF REG1,0
 Before Instruction:
 REG1 = 1110 0110
 C = 0
 After Instruction:
 REG1 = 1110 0110
 W = 1100 1100
 C = 1



RETI Return from Interrupt

RETW Return with Immediate in W

Syntax: [label] RETW k
Operands: $0 \leq k \leq 255$
Operation: $k \rightarrow (W)$;
 $TOS \rightarrow PC$
Status Affected: None
Description: The W register is loaded with the 8-bit immediate 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words: 1
Cycles: 2
Example:

```

LCALL TABLE;W contains table
;offset value
• ;W now has table value
•
TABLE
ADDWR PC ;W = Offset
RETW k1 ;Begin table
RETW k2 ;
•
•
RETW kn ;End of table
Before Instruction
W = 0x07
After Instruction
W = value of k8
    
```

Syntax: [label] SLEEP
Operands: none
Operation: $00h \rightarrow WDT$,
 $0 \rightarrow WDT$ prescaler,
 $1 \rightarrow /TO$,
 $0 \rightarrow /PD$
Status Affected: $/TO$ and $/PD$
Description: The power-down status bit, $/PD$ is cleared. Time-out Status bit, $/TO$ is set. Watchdog Timer and its prescaler are cleared. The processor enters Sleep mode with the oscillator stopped.

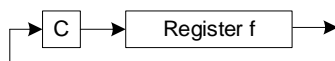
SUBWI Subtract W from literal

Syntax: [label] SUBWI k
Operands: $0 \leq k \leq 255$
Operation: $k - (W) \rightarrow (W)$
Status Affected: C, DC, and Z
Description: The W register is subtracted (2's complement method) from the 8-bit immediate 'k'. The result is placed in the W register.

C=0	$W > k$
C=1	$W \leq k$
DC=0	$W[3:0] > k[3:0]$
DC=1	$W[3:0] \leq k[3:0]$

RRR Rotate Right f through Carry

Syntax: [label] RRR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: See description below
Status Affected: C
Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SUBWFB Subtract W from f with Borrow

Syntax: SUBWFB f {,d}
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f) - (W) - (/B) \rightarrow$ destination register
Status Affected: C, DC, and Z
Description: Subtract W and the BORROW flag (CARRY) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

SLEEP Enter Sleep mode

SWAPR Swap two half bytes in f

Syntax: [label] SWAPR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f[3:0]) \rightarrow (\text{destination}[7:4]),$
 $(f[7:4]) \rightarrow (\text{destination}[3:0])$
Status Affected: None
Description: The upper and lower half bytes of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORWI Exclusive OR immediate with W

Syntax: [label] XORWI k
Operands: $0 \leq k \leq 255$
Operation: $(W).XOR.k \rightarrow (W)$
Status Affected: Z
Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SUBWR Subtract W from f

Syntax: [label] SUBWR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f)-(W) \rightarrow (\text{destination register})$
Status Affected: C, DC, and Z
Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result's stored back in register 'f'.

C=0	$W > f$
C=1	$W \leq f$
DC=0	$W[3:0] > f[3:0]$
DC=1	$W[3:0] \leq f[3:0]$

XORWR Exclusive OR W with f

Syntax: [label] XORWR f,d
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(W).XOR.(f) \rightarrow (\text{destination register})$
Status Affected: Z
Description: Perform a logical XOR operation on the contents of the W register and the contents of the register f. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register f.

16. ELECTRICAL SPECIFICATIONS

16.1. Limit Parameters

Operation temperature Grade.....	-40 – +85°C
Storage temperature.....	-40 – +125°C
Junction operation temperature (Tj)	-40 – +150°C
Power supply voltage.....	V _{SS} -0.3V – V _{SS} +6.0V
PAD input voltage.....	V _{SS} -0.3V – V _{DD} +0.3V

Notes:

1. Stresses above “Limit Parameters” may cause permanent damages to the device.
2. All characterizations are at 25°C, V_{DD} =1.9 – 5.5V unless otherwise stated.
3. Values and ranges indicated are from characterizations, and are not indicative of the final shipping criteria.
4. Production test are at 25°C unless otherwise stated. Performance at temperature outside of above operation temperature are not guaranteed as high temperature screening is not part of normal production procedure.
5. Typical unstressed memory data retention @ 150°C > 10 years.

16.2. Operation Characteristics

Parameters		Min	Typical	Max	Units	Conditions
Fsys (SysClk)	2T /4T	-	-	8	MHz	-40~85°C, V _{DD} = 1.9~5.5V
		-	-	16	MHz	-40~85°C, V _{DD} = 2.7~5.5V
Instruction Cycle (T _{INSTRCLK})	2T	-	125	-	ns	SysClk = HIRC
	4T	-	250	-	ns	
	2T	-	61	-	µs	SysClk = LIRC
	4T	-	122	-	µs	
Power-On-Reset hold time (T _{DRH})		-	4.2	—	ms	25°C, PWRT disable
Ext. Reset pulse width (T _{MCLRB})		2000	-	-	ns	25°C
WDT period (T _{WDT})		-	1	-	ms	No prescaler, WDTPS[3:0]=0000

16.3. POR, LVR, LVD

Power-On Reset (POR)

Parameters	Min	Typical	Max	Units	Conditions
I_{POR} Operating Current	–	0.14	–	μA	25°C, $V_{DD} = 3.3\text{V}$
V_{POR}	–	1.65	–	V	25°C

Low Voltage Reset (LVR)

Parameters	Min	Typical	Max	Units	Conditions
I_{LVR} Operating Current	–	15.9	–	μA	25°C, $V_{DD} = 3.3\text{V}$
V_{LVR} , LVR threshold	1.94	2.0	2.06	V	25°C
	2.13	2.2	2.27		
	2.42	2.5	2.58		
	2.72	2.8	2.88		
	3.01	3.1	3.19		
	3.49	3.6	3.71		
	3.98	4.1	4.22		
LVR delay	94	–	125	μs	25°C, $V_{DD} = 1.9 - 5.5\text{V}$

Low Voltage Detection (LVD)

Parameters	Min	Typical	Max	Units	Conditions
I_{LVD} Operating Current	–	22.7	–	μA	25°C, $V_{DD} = 3.3\text{V}$
V_{LVD} , LVD threshold	1.94	2.0	2.06	V	25°C
	2.33	2.4	2.47		
	2.72	2.8	2.88		
	2.91	3.0	3.09		
	3.49	3.6	3.71		
	3.88	4.0	4.12		
LVD delay	94	–	125	μs	25°C, $V_{DD} = 1.9 - 5.5\text{V}$

16.4. I/O PORTS

Parameters		Min	Typical	Max	Units	Conditions
V_{IL}		0	—	$0.3 * V_{DD}$	V	
V_{IH}		$0.7 * V_{DD}$	—	V_{DD}	V	
Leakage current		-1	—	1	μA	$V_{DD} = 5V$
Source Current	L0	—	-4	—	mA	25°C, $V_{DD} = 5V$, $V_{OH} = 4.5V$
	L1	—	-8	—		
	L2	—	-26	—		
Sink Current	L0	—	53	—	mA	25°C, $V_{DD} = 5V$, $V_{OL} = 0.5V$
	L1	—	62	—		
Pull-up resistance		—	20	—	k Ω	
Pull-down resistance		—	20	—	k Ω	

16.5. Operating Current (I_{DD})

Parameters	Sysclk	Typical @ V_{DD}			Units
		2.0V	3.0V	5.5V	
Normal mode (2T) - I_{DD}	16MHz	—	2.181	2.286	mA
	8MHz	1.078	1.522	1.592	
	4MHz	0.826	1.178	1.214	
	2MHz	0.624	0.716	0.719	
	1MHz	0.400	0.460	0.461	
	500kHz	0.294	0.361	0.369	
	250kHz	0.244	0.317	0.327	
	125kHz	0.219	0.295	0.306	
	32kHz	0.034	0.046	0.048	
Sleep mode (WDT OFF , LVR OFF), I_{SB}	—	0.211	0.274	0.423	μA
Sleep mode (WDT ON, LVR OFF)	—	1.383	2.499	3.062	
Sleep mode (WDT OFF , LVR ON)	—	11.618	15.951	21.956	
Sleep mode (WDT ON, LVR ON)	—	12.793	18.156	24.469	
Sleep mode (WDT OFF , LVR OFF , LVD ON)	—	18.621	22.774	28.738	

Note: Test conditions for I_{SB} in sleep mode with all I/Os set to input mode and external pull-down to GND.

16.6. Internal Oscillators

Internal Low Frequency Oscillator (LIRC)

LIRC is set at 32 kHz during measurement (LFMOD=0).

Parameters	Min	Typical	Max	Units	Conditions
Range	30.4	32	33.6	kHz	25°C, V _{DD} = 2.5V
temperature dependence	-3.0%	-	2.0%	-	-40 ~ 85°C, V _{DD} = 2.5V
supply voltage variation	-4.5%	-	2.0%	-	25°C, V _{DD} = 1.9 ~ 5.5V
I _{LIRC} Operating Current	-	1.3	-	μA	25°C, V _{DD} = 3.0V
Start up Time	-	4.6	-	μs	25°C, V _{DD} = 3.0V

Internal High Frequency Oscillator (HIRC)

Parameters	Min	Typical	Max	Units	Conditions
Range	15.84	16	16.16	MHz	25°C, V _{DD} = 2.5V
temperature dependence	-2.0%	-	2.0%	-	-40 ~ 85°C, V _{DD} = 2.5V
supply voltage variation	-0.5%	-	0.5%	-	25°C, V _{DD} = 1.9 ~ 5.5V
I _{HIRC} Operating Current	-	40	-	μA	25°C, V _{DD} = 3.0V
Start up time	-	2.5	-	μs	25°C, V _{DD} = 3.0V

16.7. ADC (12bit) and ADC VREF

ADC (12bit)

Parameters	Min	Typical	Max	Units	Conditions
Operating Voltage V _{DD}	2.7	-	5.5	V	
Operating Current I _{VDD}	-	100	-	μA	V _{REF+} = V _{DD} = 2.7V
	-	110	-	μA	V _{REF+} = V _{DD} = 3.0V
	-	140	-	μA	V _{REF+} = V _{DD} = 5.5V
Analog input voltage V _{AIN}	V _{REF-}	-	V _{REF+}	V	
External Reference Voltage V _{REF}	-	-	V _{DD}	V	
Resolution	-	-	12	位	
Integral error E _{IL}	-	±1.5	-	LSB	V _{REF+} = V _{DD} = 5.0V, V _{REF-} = GND, F _{ADCLK} = 250kHz
Differential error E _{DL}	-	±1.0	-	LSB	
Offset error E _{OFF}	-	±3.0	-	LSB	V _{REF+} = V _{DD} = 5.0V, V _{REF-} = GND, F _{ADCLK} = 250kHz
Gain error E _{GN}	-	±5.0	-	LSB	
Conversion clock cycle T _{AD}	-	2	-	μs	V _{REF+} > 3.0V, V _{DD} > 3.0V
Conversion clock cycles	-	17	-	T _{AD}	
Settling time (T _{ST})	-	15	-	μs	
Sample time (T _{ACQ})	-	≥ 2	-	μs	
Analog Voltage Source Impedance (ZAI)	-	-	10	kΩ	(recommend)

Differential Error DNL

typical DNL Error (LSB) @ $V_{DD} = 5\text{ V}$				
$\frac{V_{REF+}}{F_{ADCLK}}$	0.5	2	3	V_{DD-}
$\leq 500\text{kHz}$	± 3.0	± 1.5	± 1.0	± 1.0
1 MHz	± 3.0	± 1.5	± 1.0	± 1.0
2 MHz	± 6.0	± 2.0	± 1.5	± 1.5
4 MHz	–	–	–	± 4.0

Integral Error INL

typical INL Error (LSB) @ $V_{DD} = 5\text{ V}$				
$\frac{V_{REF+}}{F_{ADCLK}}$	0.5	2	3	V_{DD-}
$\leq 500\text{kHz}$	± 3.0	± 1.5	± 1.5	± 1.5
1 MHz	± 3.5	± 2.0	± 2.0	± 2.0
2 MHz	± 7.0	± 2.5	± 2.5	± 2.5
4 MHz	–	–	–	± 4.5

ADC V_{REF}

Parameters		Min	Typical	Max	Units	Conditions
Internal reference voltage $V_{ADC-REF}$	$V_{ADC-REF} = 0.5\text{V}$	0.492	0.5	0.508	V	
	$V_{ADC-REF} = 2.0\text{V}$	1.990	2	2.010	V	
	$V_{ADC-REF} = 3.0\text{V}$	2.985	3	3.015	V	
Settling time T_{VRINT}	$V_{ADC-REF} = 0.5\text{V}$	–	400	–	μs	
		–	600	–	μs	$C_{EXT} = 1\mu\text{F}$
	$V_{ADC-REF} = 2.0\text{V}$	–	450	–	μs	
		–	800	–	μs	$C_{EXT} = 1\mu\text{F}$
$V_{ADC-REF} = 3.0\text{V}$	–	450	–	μs		
	–	1200	–	μs	$C_{EXT} = 1\mu\text{F}$	

Note:

1. Typical values are tested at 25°C , $V_{DD} = 5.0\text{V}$, unless otherwise noted.
2. C_{EXT} is the external capacitor connected to the internal reference voltage $V_{ADC-REF}$ (when ADPREF or ADNREF is configured to 10, see [Table 11 -3](#)).

16.8. Program and Data EEPROM

Parameters		Min	Typical	Max	Units	Conditions
$V_{DD-READ}$	Program/Data EE read voltage	V_{POR}	-	5.5	V	-40 – 85 °C
$V_{DD-WRITE}$	Program EE write voltage	2.7	-	5.5	V	-40 – 85 °C
	Data EE write voltage	1.9	-	5.5		
N_{END}	Program EE erase/write cycles	100k	-	-	cycle	25 °C
		40k	-	-		85 °C
	Data EE erase/write cycles	100k	-	-		25 °C
		40k	-	-		85 °C
T_{RET}	Program EE data retention	20	-	-	year	After 1k cycles @ 85 °C
	Data EE data retention	20	-	-		After 10k cycles @ 85 °C
T_{WRITE}	Data EE write time	-	4.0	-	ms	Auto-Erase enabled
		-	2.0	-		Auto-Erase disabled
I_{PROG}	Data EE programming current	-	350	-	μA	25 °C, $V_{DD} = 3 V$, 16MHz / 2T

16.9. EMC characteristics

ESD

Parameters		Min	Typical	Max	Units	Conditions
V_{ESD}	HBM	7000	-	-	V	MIL-STD-883H Method 3015.8
V_{ESD}	MM	400	-	-	V	JESD22-A115

Latch-up

Parameters	Min	Typical	Max	Units	Conditions
LU, static latch-up	200	-	-	mA	EIA/JESD78

EFT

Parameters	Min	Typical	Max	Units	Conditions
V_{EFT}	5.5	-	-	kV	$V_{DD} (5V)$ and GND: 1 μF

17. Characterization Graphs

Note: The characterization graphs are based on the feature values and are for reference only and have not been tested in production.

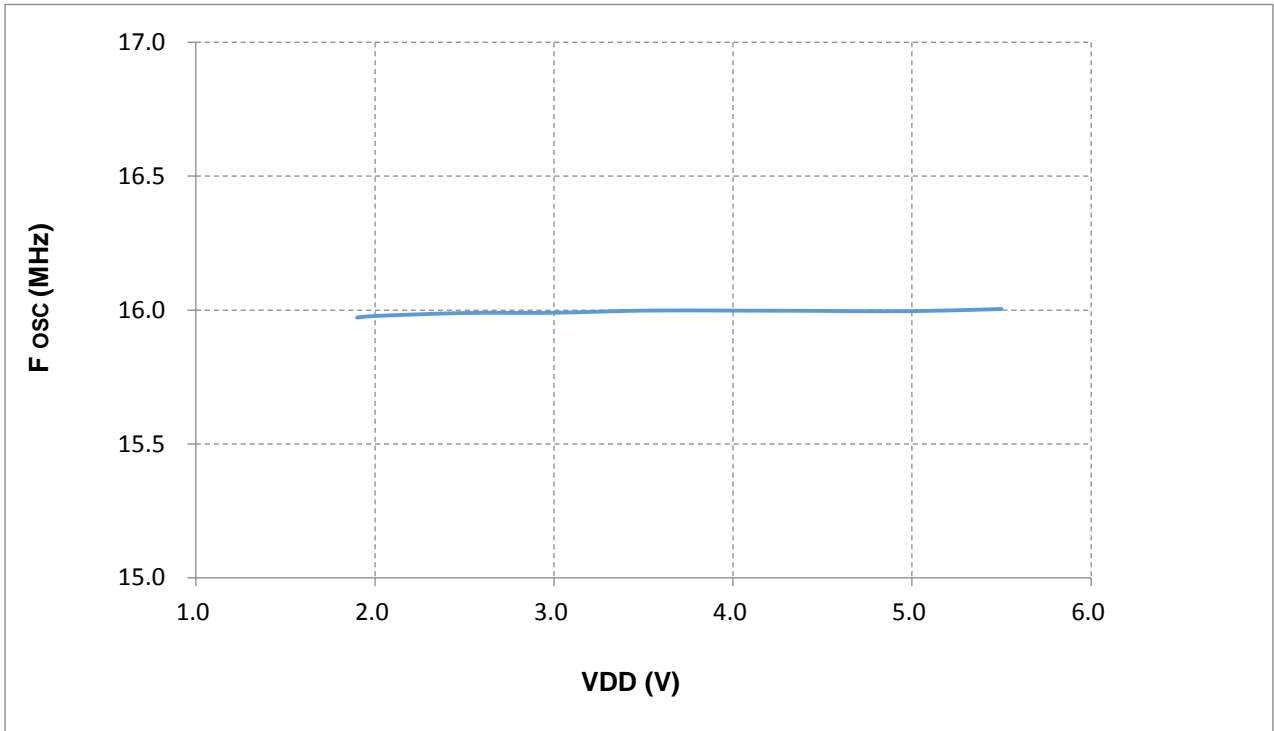


Figure 17-1 HIRC vs. V_{DD} (T_A = 25°C)

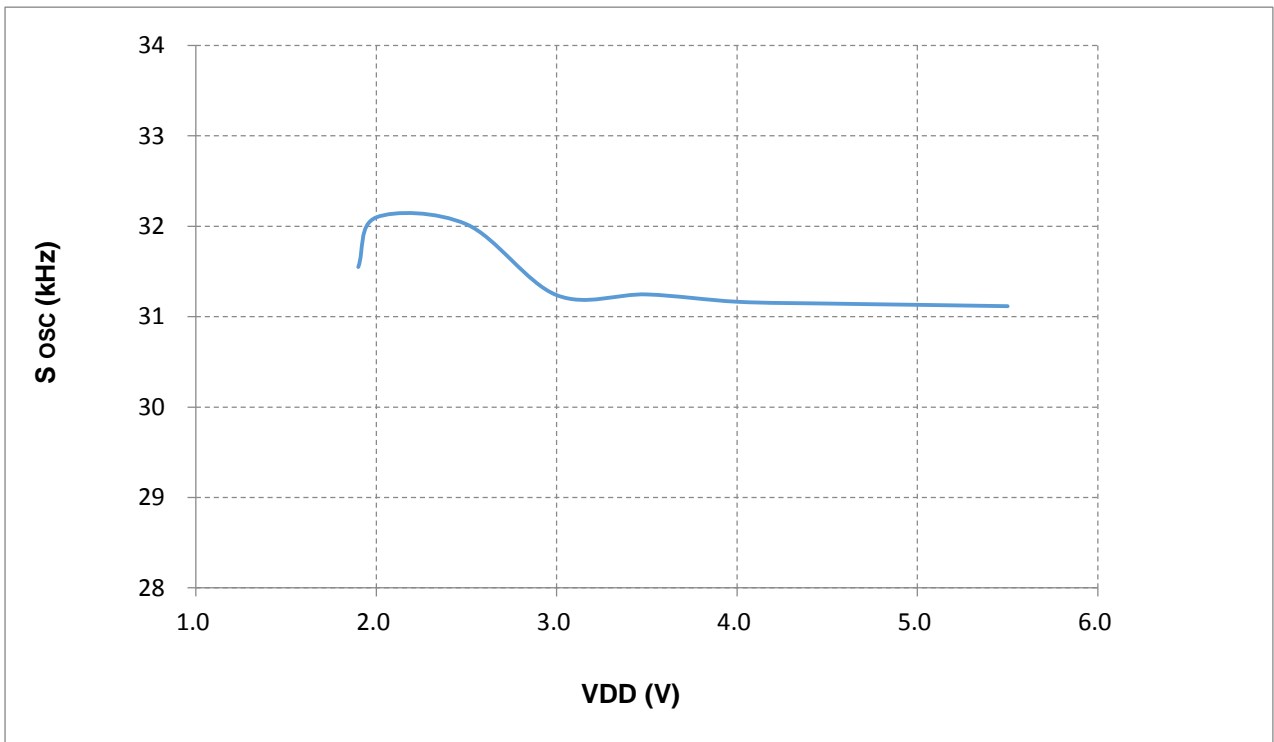


Figure 17-2 LIRC vs. V_{DD} (T_A = 25°C)

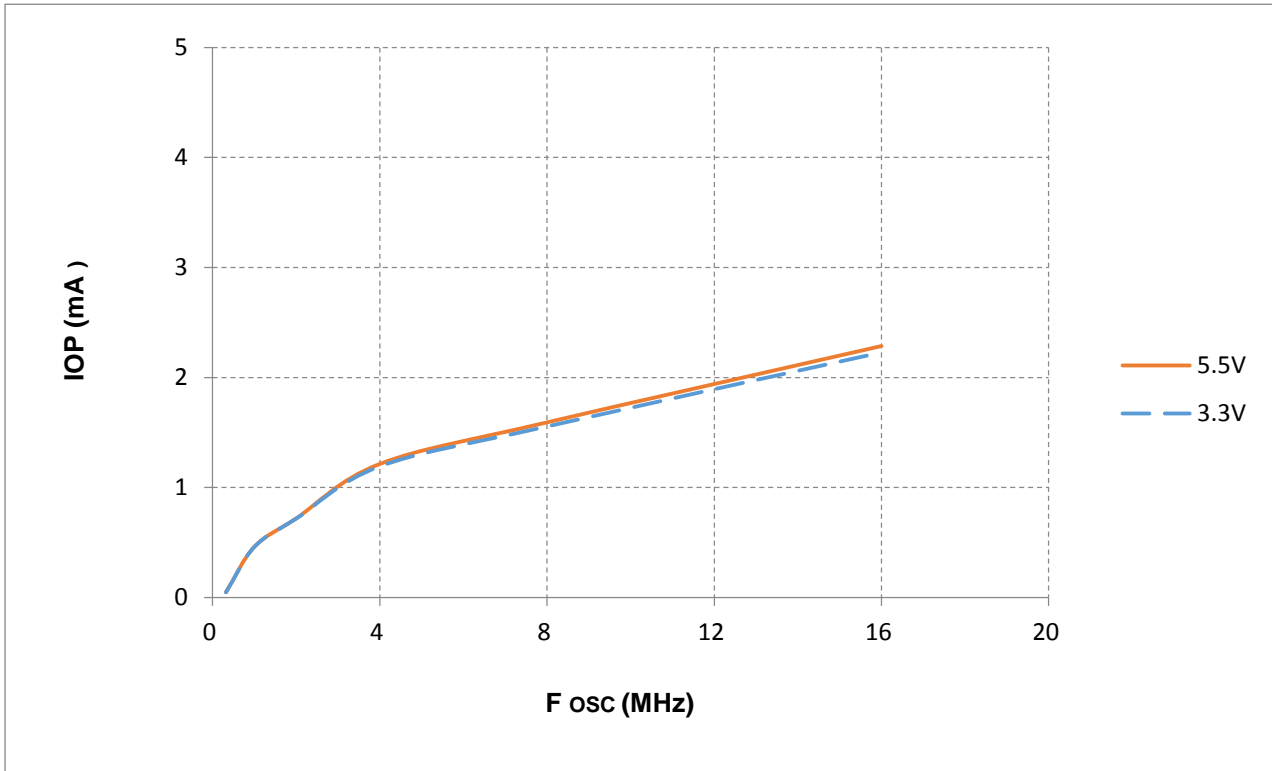


Figure 17-3 I_{DD} vs Freq (2T, T_A=25°C)

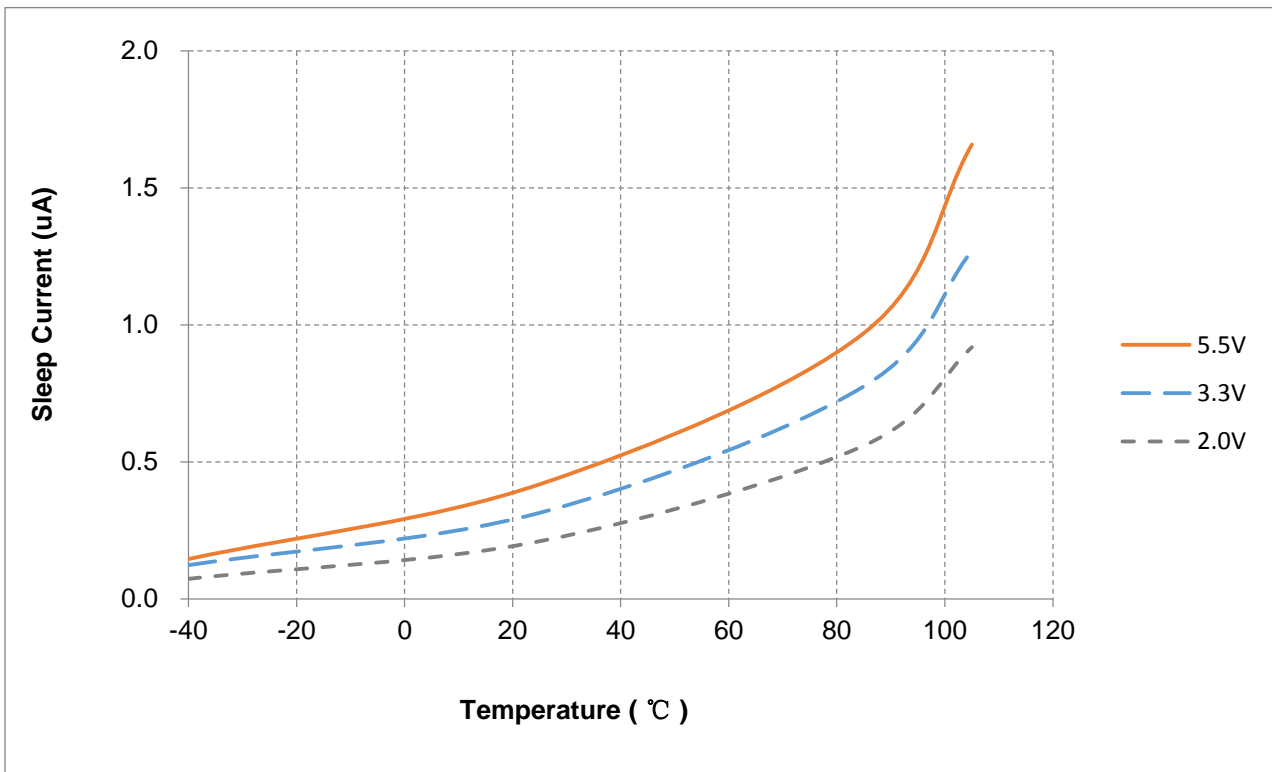


Figure 17-4 Sleep Current (I_{SB}) vs. Temperature

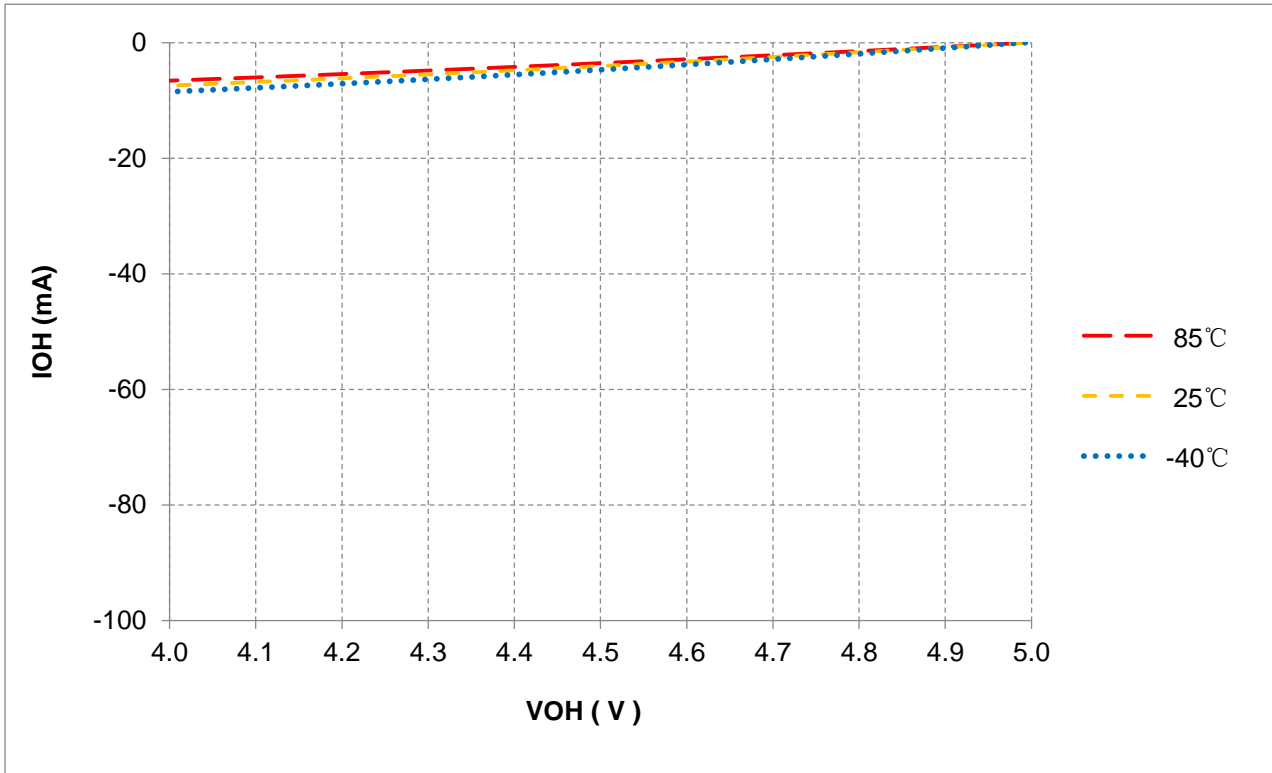


Figure 17-5 I_{OH} vs V_{OH} @L0 = -4mA, V_{DD} = 5V

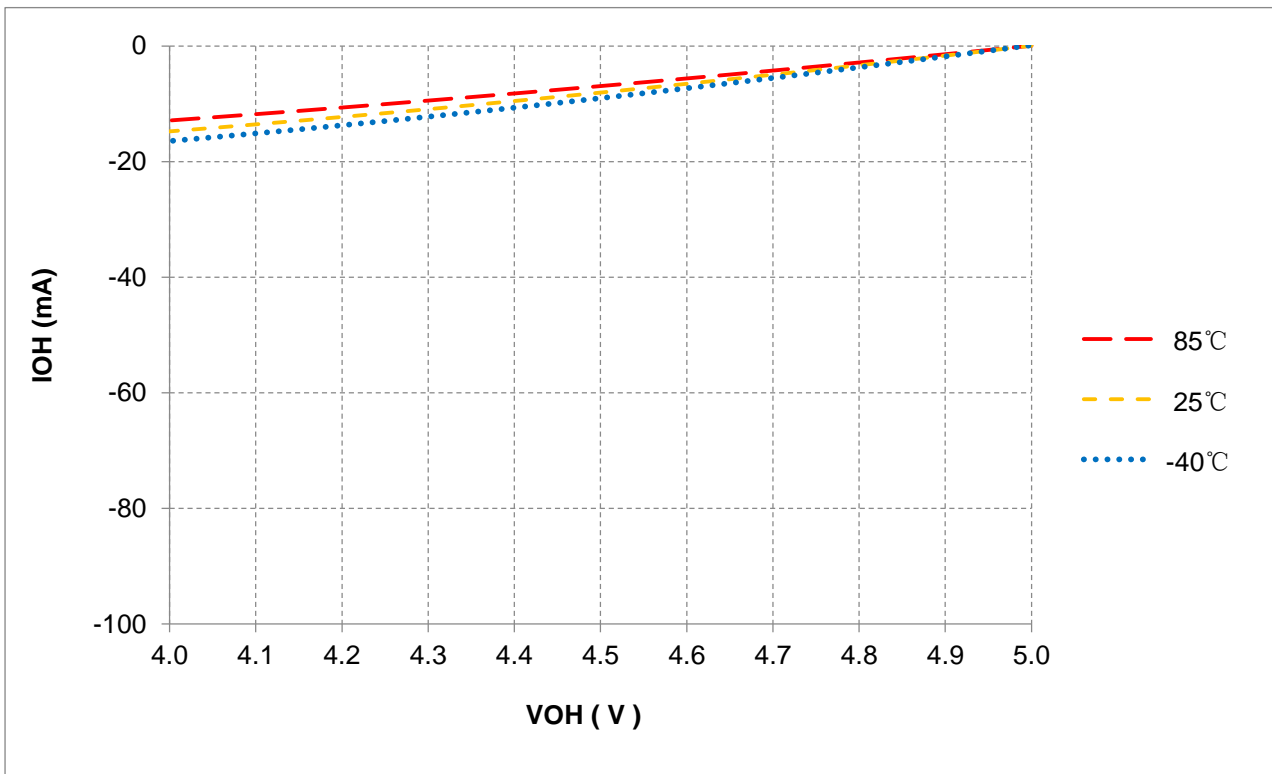


Figure 17-6 I_{OH} vs V_{OH} @L1 = -8mA, V_{DD} = 5V

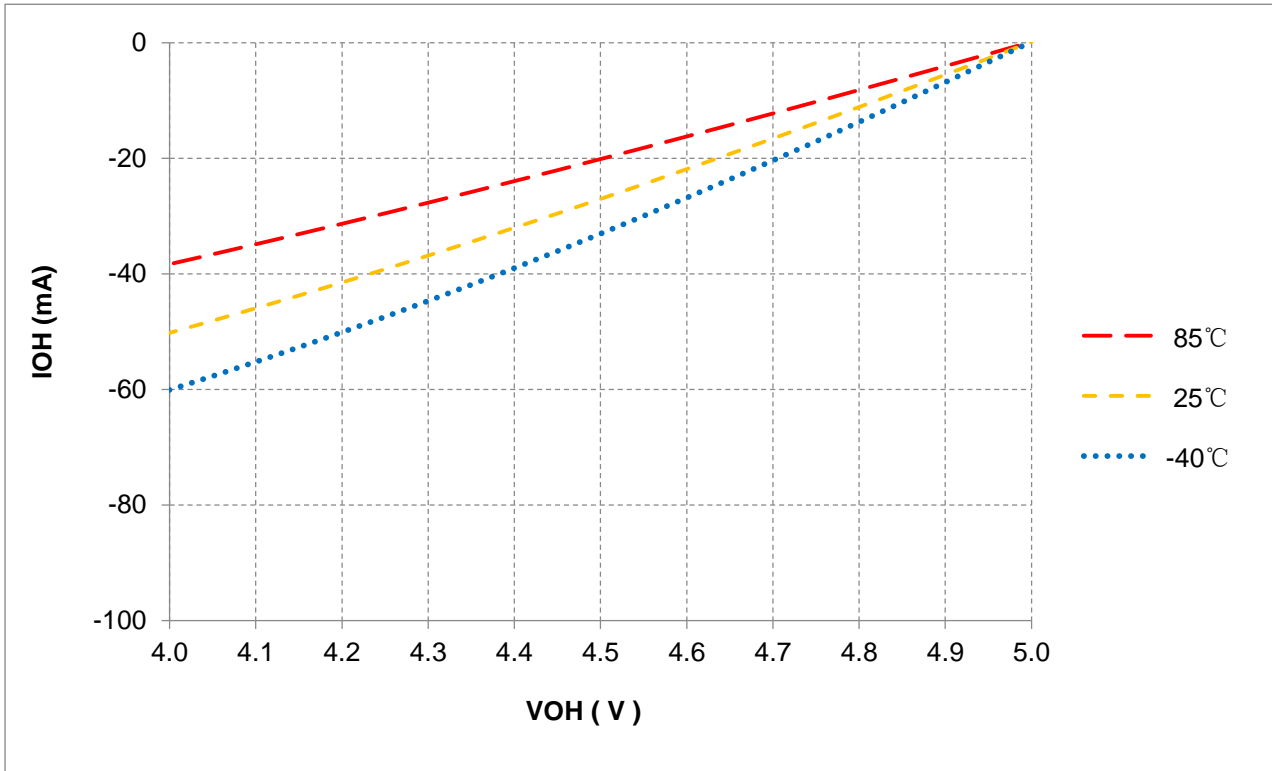


Figure 17-7 I_{OH} vs V_{OH} @L2 = -26mA, $V_{DD} = 5\text{V}$

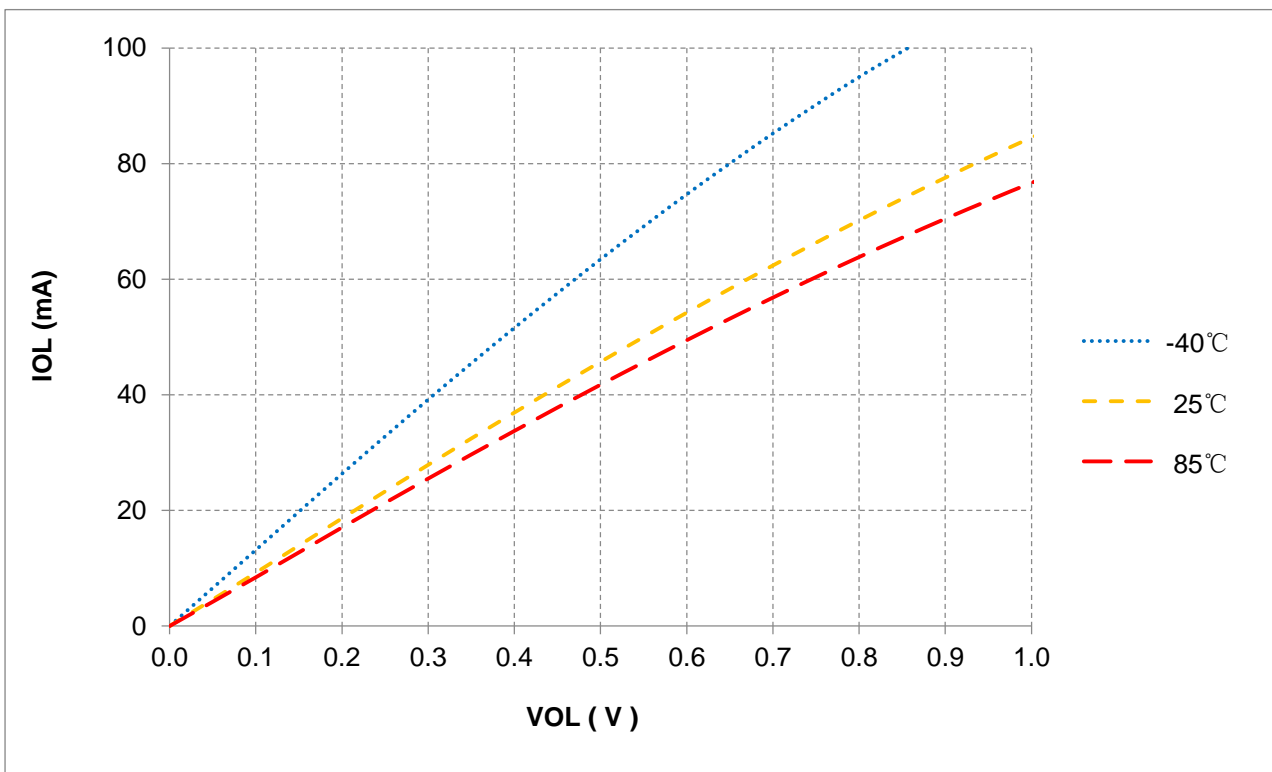


Figure 17-8 I_{OL} vs V_{OL} @L0 = 53mA, $V_{DD} = 5\text{V}$

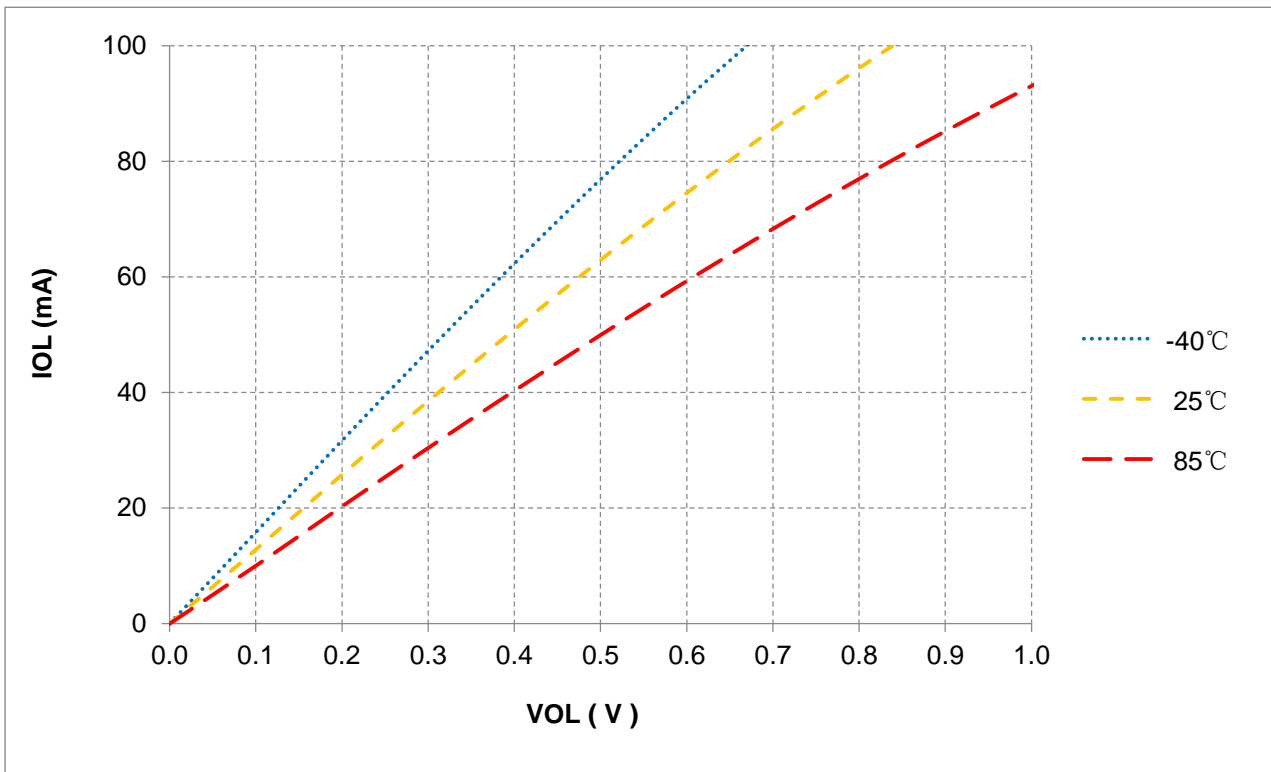
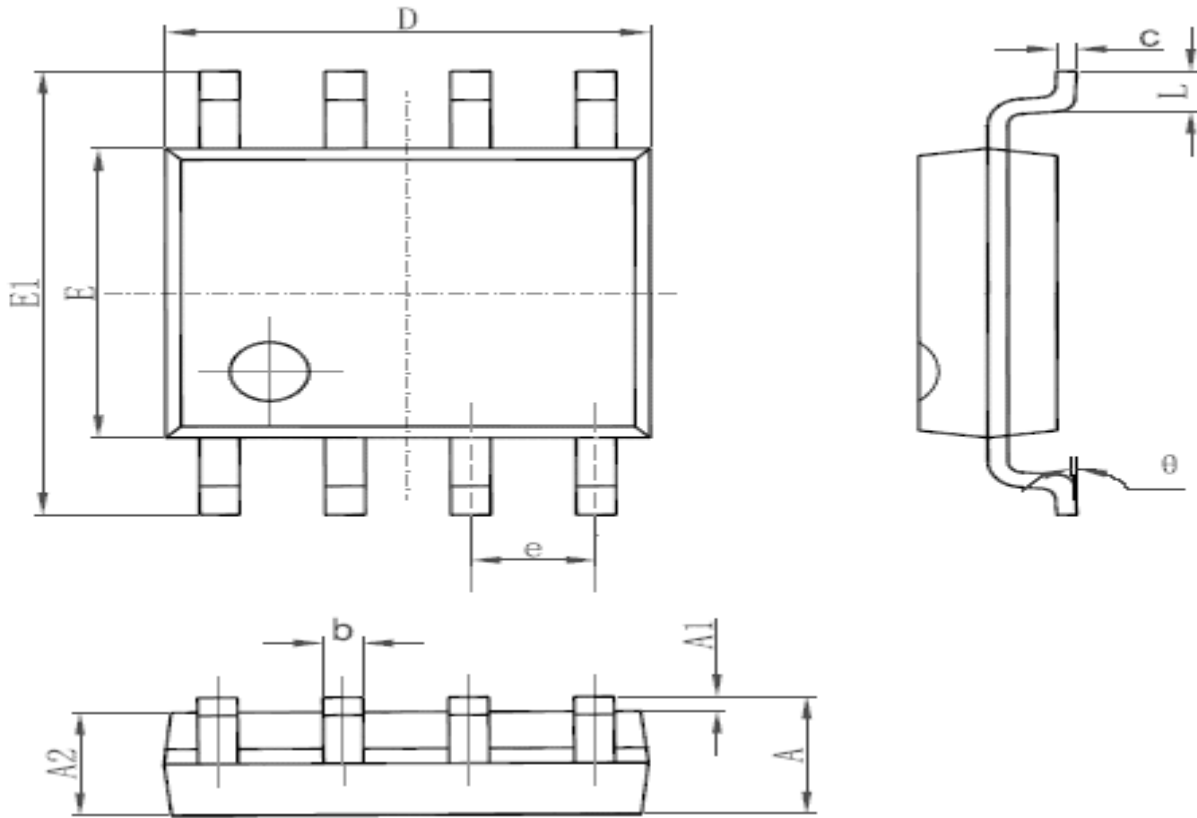


Figure 17-9 I_{OL} -vs V_{OL} @L01 = 62mA, V_{DD} = 5V

18. PACKAGING INFORMATION

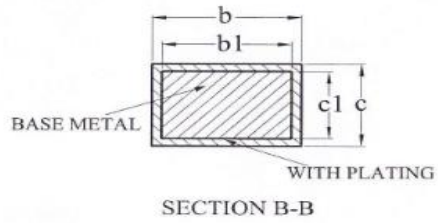
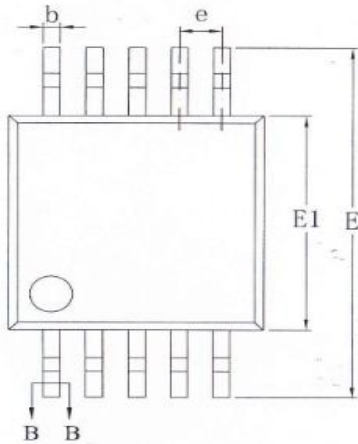
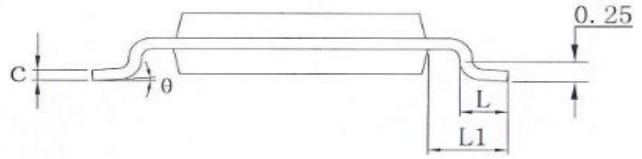
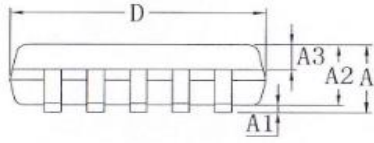
The device is available in SOP8, MSOP10, SOP14, SOP16, SOP20, QFN20 and TSSOP20 packages. The specific package size information is shown below:

SOP8



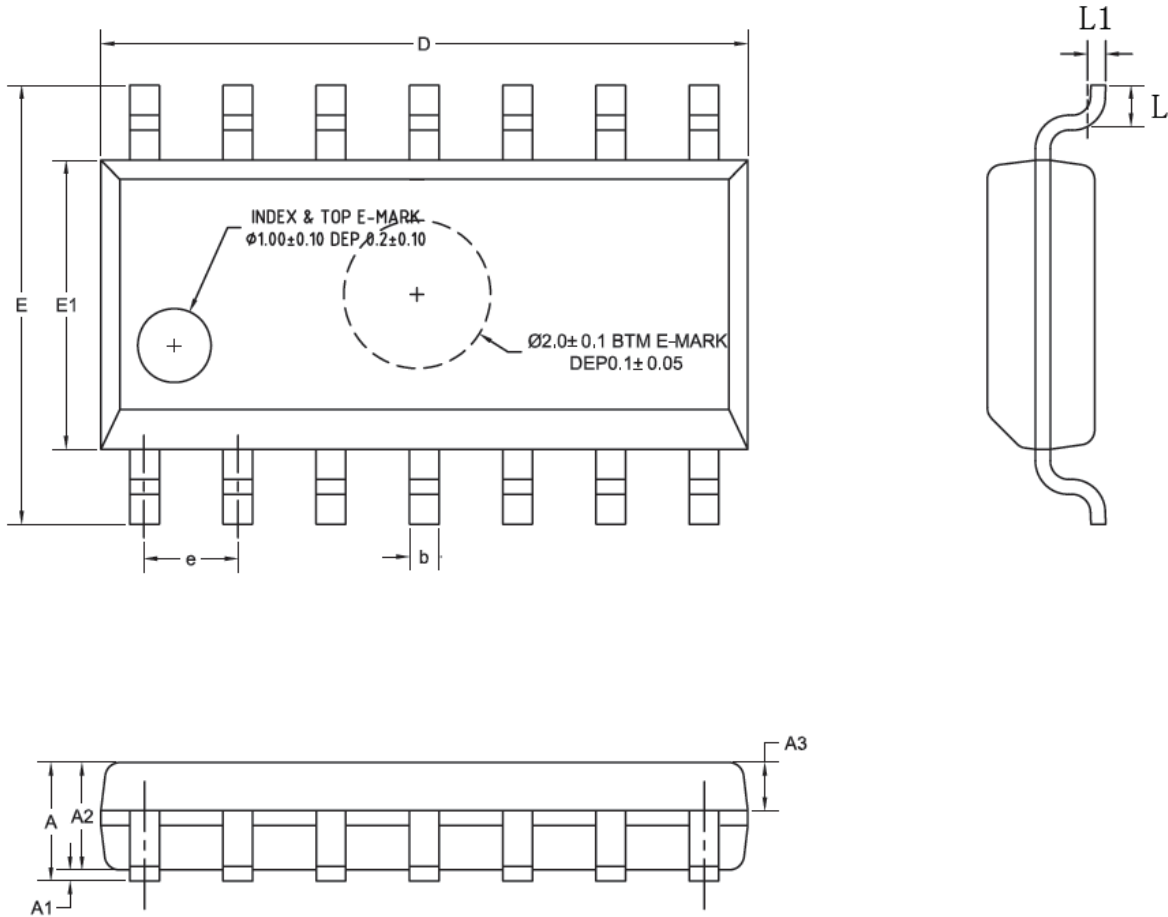
Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

MSOP10



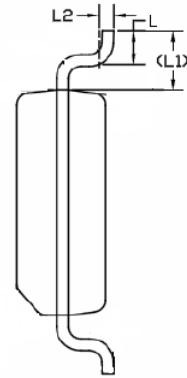
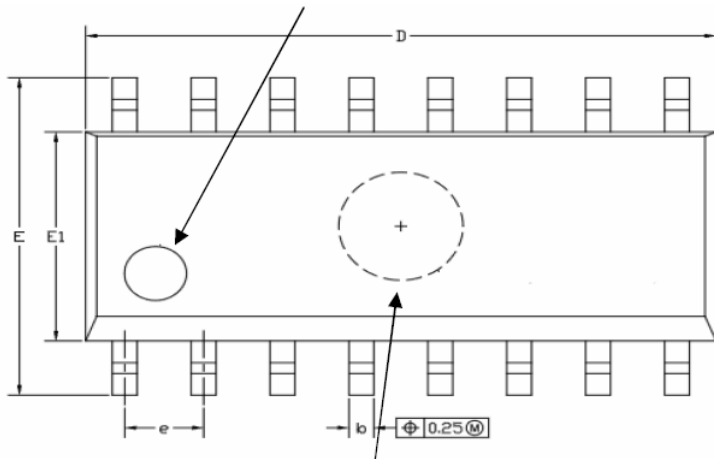
Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	-	1.100	-	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.180	0.260	0.007	0.010
b1	0.170	0.230	0.007	0.009
c	0.150	0.190	0.006	0.007
c1	0.140	0.160	0.006	0.006
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500(BSC)		0.020 (BSC)	
L	0.400	0.700	0.016	0.028
L1	0.950(REF)		0.037(REF)	
theta	0	8°	0	8°

SOP14

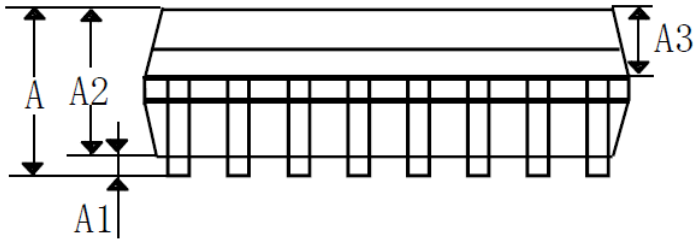


Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	-	1.700	-	0.066
A1	0.100	0.200	0.004	0.008
A2	1.400	1.500	0.055	0.059
A3	0.620	0.680	0.024	0.027
b	0.370	0.420	0.015	0.016
D	8.710	8.910	0.343	0.347
E	5.900	6.100	0.232	0.238
E1	3.800	3.950	0.150	0.156
e	1.270 (BSC)		0.050 (BSC)	
L	0.500	0.700	0.020	0.027
L1	0.250 (BSC)		0.010 (BSC)	

SOP16

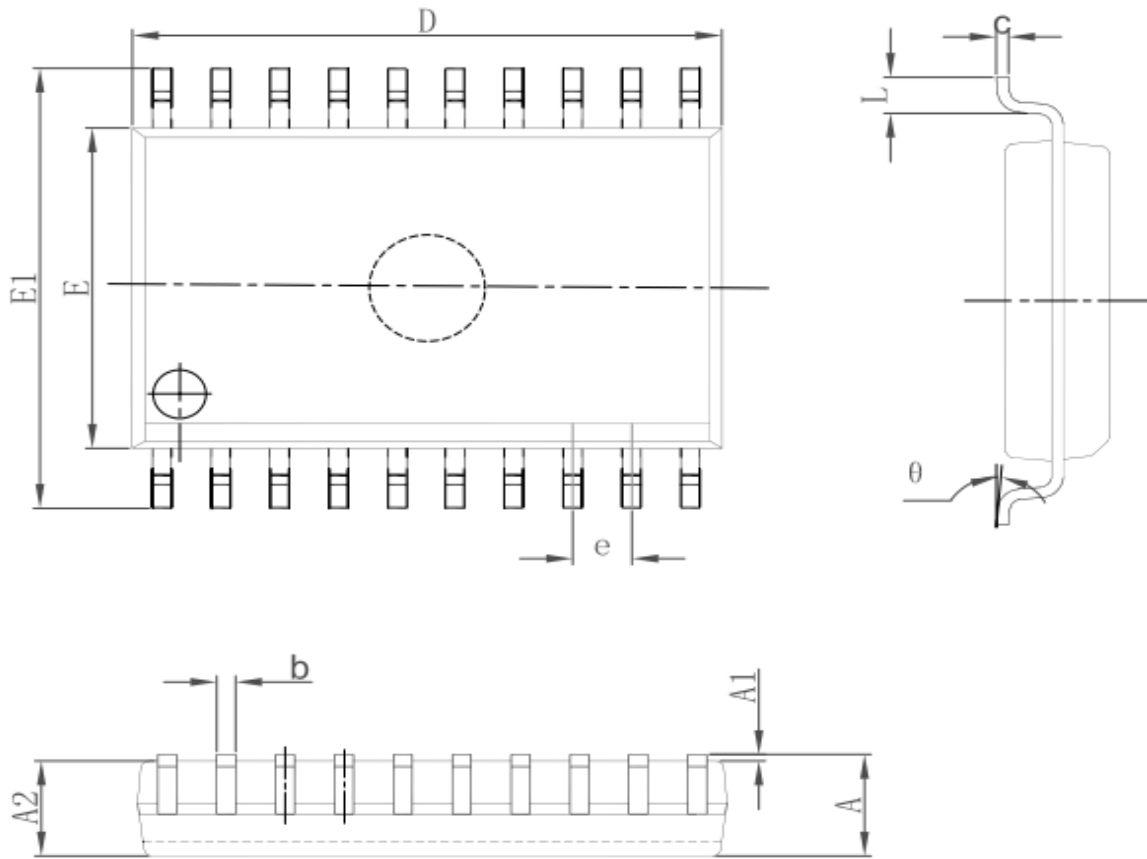


$\Phi 2.0 \pm 0.05$ DEP $0.1 + 0.03 / -0.05$



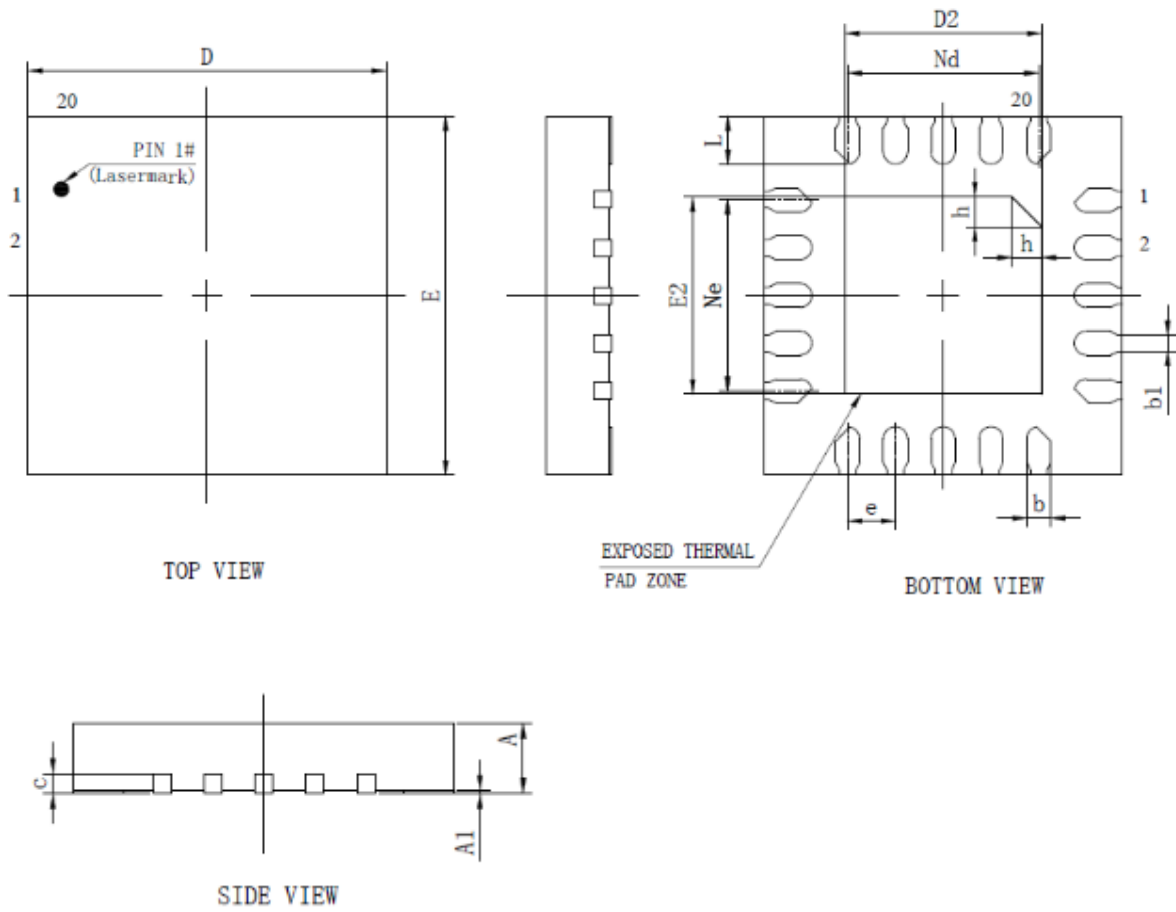
Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	-	1.700	-	0.066
A1	0.100	0.200	0.004	0.008
A2	1.420	1.480	0.056	0.058
A3	0.620	0.680	0.024	0.027
D	9.960	10.160	0.392	0.396
E	5.900	6.100	0.232	0.238
E1	3.870	3.930	0.152	0.153
b	0.370	0.430	0.015	0.017
e	1.240	1.300	0.048	0.051
L	0.500	0.700	0.020	0.027
L1	1.050 (REF)		0.041(REF)	
L2	0.250 (BSC)		0.010 (BSC)	

SOP20



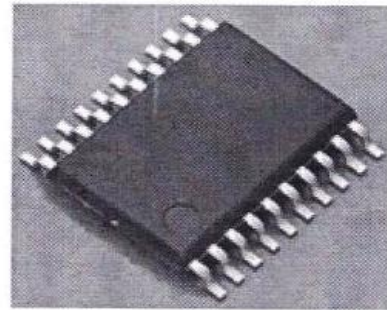
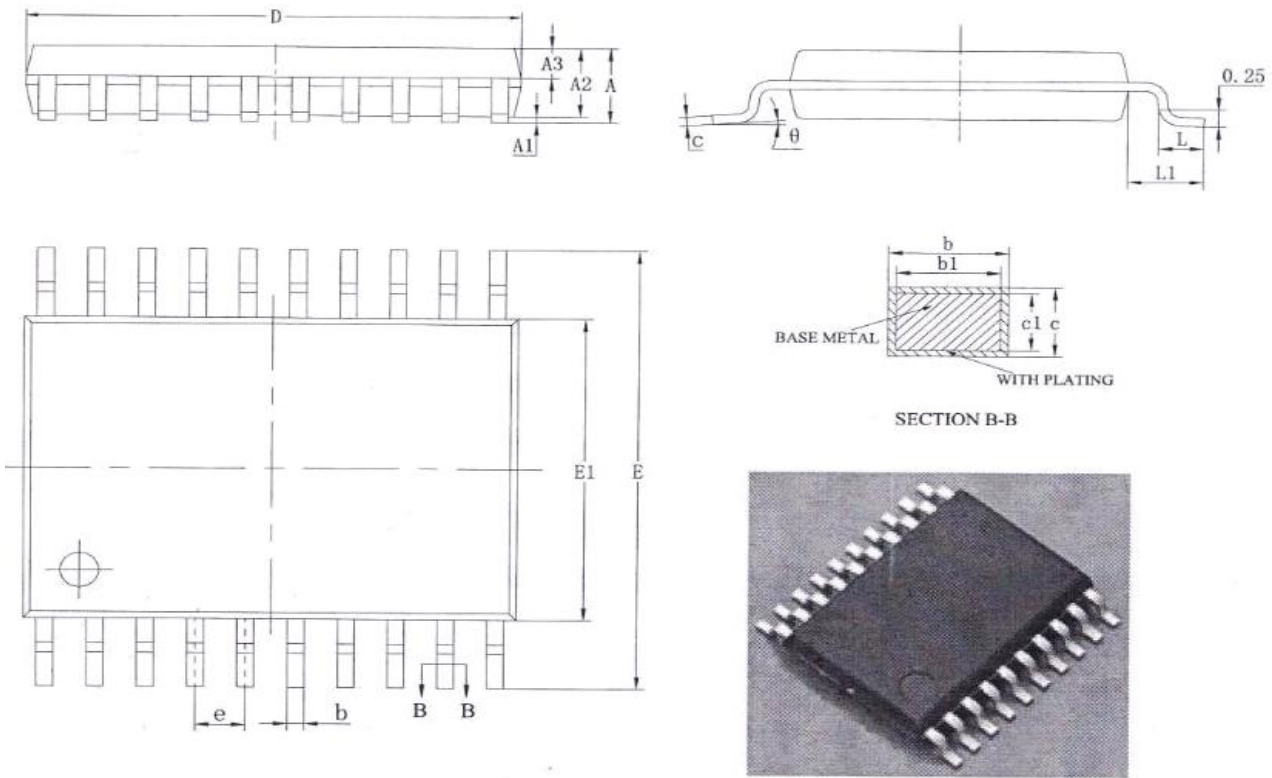
Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

QFN20



Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	-	0.050	-	0.002
b	0.150	0.250	0.006	0.010
b1	0.140 (REF)		0.006 (REF)	
c	0.100	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
D2	1.550	1.750	0.061	0.069
e	0.400 (BSC)		0.016 (BSC)	
Ne	1.600 (BSC)		0.063 (BSC)	
Nd	1.600 (BSC)		0.063 (BSC)	
E	2.900	3.100	0.114	0.122
E2	1.550	1.750	0.061	0.069
L	0.350	0.450	0.014	0.018
h	0.200	0.300	0.008	0.012

TSSOP20



Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	-	1.20	-	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
A3	0.39	0.49	0.015	0.019
b	0.20	0.28	0.008	0.011
b1	0.19	0.25	0.007	0.010
c	0.13	0.17	0.005	0.007
c1	0.12	0.14	0.005	0.006
D	6.40	6.60	0.252	0.260
E1	4.30	4.50	0.169	0.177
E	6.20	6.60	0.244	0.259
e	0.65 (BSC)		0.026 (BSC)	
L	0.45	0.75	0.018	0.030
L1	1.00REF		0.039REF	
θ	0	8°	0	8°

19. Appendix : Register Types

Abbr.	Description	Illustration
WO	Write Only, read "0"	Write only, read as 0
RO	Read Only	Read only
RW	Read, Write	Readable, writable
RW0	Read, Write "0" only	Readable, only write 0, write 1 is invalid
RW1	Read, Write "1" only	Readable, only write 1, write 0 is invalid
R_W1C	Read, Cleared by Writing "1"	Readable, write 1 to clear, and writing '0' has no effect on the bit
Res	Reserved, read "0"	Reserved bit, read only, read as 0

Contact Information**Fremont Micro Devices Corporation**

#5-8, 10/F, Changhong Building
Ke-Ji Nan 12 Road, Nanshan District,
Shenzhen, Guangdong, PRC 518057

Tel: (+86 755) 8611 7811

Fax: (+86 755) 8611 7810

Fremont Micro Devices (HK) Limited

#16, 16/F, Block B, Veristrong Industrial Centre,
34-36 Au Pui Wan Street, Fotan, Shatin, Hong Kong SAR

Tel: (+852) 2781 1186

Fax: (+852) 2781 1144

<http://www.fremontmicro.com>

* Information furnished is believed to be accurate and reliable. However, Fremont Micro Devices Corporation assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent rights of Fremont Micro Devices Corporation. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. Fremont Micro Devices Corporation products are not authorized for use as critical components in life support devices or systems without express written approval of Fremont Micro Devices Corporation. The FMD logo is a registered trademark of Fremont Micro Devices Corporation. All other names are the property of their respective owners.