PowerPCB with BlazeRouter 5.0.1 Release Highlights

Welcome to the latest release of PowerPCB with BlazeRouter. New features and functionality address many of the challenges faced by electronic design professionals.

PowerPCB with BlazeRouter 5.0.1 and 5.0 include major new functionality and enhancements in the following areas:

- ePD Link

  PowerPCB 5.0.1 introduces the ePD Link to pass design data to and from DxDesigner and PowerPCB. Data that is passed include parts and net list data, Design Rules, Assembly Variances, Test Points, and General Attributes. The ePD Link also maintains the synchronicity of part, net and design rule data. **If you use ePD 3.0, you must use the new ePD Link.**

- ECOGEN

  The ECOGEN utility has been updated in PowerPCB 5.0.1 to include the comparison of net scheduling data and the comparison of part placement information. There is now more control over renaming of parts and nets. You can raise or lower the cost of such operations using controls on the Compare/ECO Tools dialog box or by using ECOGEN command line switches.

- FIRE

  Fast Interactive Route Editor, or FIRE, is introduced in this release. FIRE represents a major leap forward in interactive routing that is unmatched in the industry. FIRE takes advantage of many of the powerful algorithms that differentiate BlazeRouter from other routers, including push and shove, smoothing, pad entry quality, and robust hierarchical rules support. Coupled with BlazeRouter HSD, FIRE offers unique aids for interactive routing of length-constrained nets and differential pairs, making it the industry's leading interactive routing environment for today's difficult designs.

- BlazeRouter

  BlazeRouter has been significantly enhanced for version 5.0. The user now has greater control of vias at SMD, advanced vias, device fanout, and pad entry quality. This control is at the decal or individual component level. BlazeRouter now adheres to component clearance and routing rules, which are unique trace widths and clearances assigned to components that help route from fine pitch devices, again at the decal or individual component level. Centering also has been introduced to maximize the clearance of traces between pads.

- BlazeRouter High-Speed Design

  PowerPCB 5.0 introduces BlazeRouter High-Speed Design (HSD), which delivers automatic routing to minimum and maximum length constraints, as well as to matched length constraints. BlazeRouter HSD also routes differential pairs to the most precise constraints provided in the industry. With net rescheduling the user can set and fix the topology to which a net is routed. A tuning routing pass has been added which automatically adjusts traces to meet these high-speed constraints.

- Design Verification

  Many new rules can now be set and routed to automatically by BlazeRouter. New design verification utilities assure you that all design rules set in PowerPCB, including high-speed constraints and component entry rules, are followed.

- GUI Customization

  You can customize the BlazeRouter environment to meet your specific needs. You can define personalized shortcuts (hot keys), menus, and toolbars for all system commands. You can create and assign macros to any of these items. You can also save and reuse or share your customizations with others.

- Advanced Packaging Toolkit

  Many PowerPCB users have designs with bare die, such as chip on board (COB), single chip packages, or multi-chip packages. The new Advanced Packaging Toolkit option provides significant functionality to aid in these designs. Features included aid in the definition of die components, wirebond placement, routing, and die flag definition.

ePD Link

The ePD Link in PowerPCB 5.0.1 replaces the ViewDraw Link, and must be used with DxDesigner 3.0. The ePD Link passes data to and from DxDesigner and PowerPCB, allowing you to compare design data including parts, nets, and scheduling information. You can also update the PowerPCB library with new library content from the DxDesigner schematic.

The ePD Link represents a change in procedure for ViewDraw Link users. For more information, see the following topics in *PowerPCB Help*:

- Updating DxDesigner with Changes from PowerPCB
- Updating PowerPCB with Changes from DxDesigner
- Cross-probing between DxDesigner and PowerPCB

ECOGEN

The ECOGEN utility has been updated in PowerPCB 5.0.1 to include the comparison of net scheduling data and the comparison of part placement information.

If a net has the system hidden attribute, Planning.Scheduled, which indicates the net schedule has been set in ePlanner, ECOGEN compares the pin pairs for this net and reports the minimum differences.

The part placement information now includes part X, Y placement, orientation, glue status, and mirror status. New ECO commands are defined for part placement updates in the ECO file format. ECOGEN compares this information and reports differences unless you choose to ignore this information.

There is now more control over renaming of parts and nets. You can raise or lower the cost of such operations using the Name Comparison options on the Compare/ECO Tools dialog box. Or you can use the -q and -g ECOGEN command line switches.

FIRE

FIRE (Fast Interactive Route Editor) is an all-new route editing tool. FIRE is truly "interactive BlazeRouter". Now you can complete all your routing – automatic *and* interactive – in BlazeRouter.

- **Dynamics** – FIRE can route with Dynamics on or off. With Dynamics off (manual mode), each mouse click adds one trace segment. With Dynamics on, FIRE adds all necessary segments as you guide the trace's path with the pointer, adhering to all design rules, and pushing and shoving other traces if necessary, to complete the connection.
- **Multiple DRC Modes** – Historically most PCB layout systems have two DRC modes, either all on or all off, for all types of rules. FIRE introduces multiple DRC modes, giving you control over which objects or rules to check during interactive routing. You can set DRC checking to Prevent, never allow this violation to occur; Explain, where FIRE temporarily pauses, allowing you to inspect the violation or warning; or Warn, where FIRE adds the violation, but warns you about it. You can set DRC to check different objects and rules, each of which can be set to its own DRC mode. For example, you can set FIRE to prevent clearance violations but only warn about length violations. You can set FIRE's reactions to clearance, routing, same net, placement, and length individually. You now have unsurpassed control of your interactive routing DRC environment so you can route the way you want.

- **Plowing Controls** – FIRE has unsurpassed push and shove capabilities, which let you achieve high trace densities on designs. You can set the amount of effort (Low, Medium, or High) for plowing to use to push and shove traces. The Plower has multiple operation modes. *Plow by cursor* is the traditional method, where traces are pushed and shoved out of the way of new traces as you move the pointer. Using *plow by click* you can preview where the trace will go, then, as you select a point on the design, or click to add the connection, the Plower pushes and shoves the traces out of the way. *Plow by ripup* dynamically rips up existing traces, maintaining the specified trace-to-trace clearance, as a new trace is added. The different plowing modes let you add traces the way you want, with no DRC violations to clean up afterward.
- **Automatic Necking into Pads** – If merely starting from a pad would cause a clearance violation while interactively adding traces, FIRE automatically tries to neck the trace down to a smaller legal width. It will first neck down to the pad width. If this is too large, it will neck down to the minimum trace width as defined in the design rule editor. FIRE uses this width until the first click, when it reverts back to the recommended width setting. This reduces routing time by automating what is typically a manual, and error prone, process.
- **Guard Bands** – You can display guard bands, special shapes that graphically show required clearances around obstacles, while adding or editing traces. The clearances around pads, traces, copper, and other obstacles will be displayed, showing you exactly how close you can add or move a trace to another object. This helps minimize route and route editing time. Unlike other systems that display a single guard band around the trace being routed, FIRE shows the individual guard bands around all other objects in the vicinity. In this way the entire rules hierarchy, including conditional rules, is accurately displayed.
- **Complete** – FIRE can automatically complete a connection while interactively routing, vastly speeding routing completion times. If necessary, BlazeRouter is automatically called in the background to complete even complex, multi-layer connections. Having the power of BlazeRouter available at a single click is one of the unique benefits of this routing environment.
- **Arcs** – With FIRE you can add arcs interactively. The routing angle mode is maintained, for example, in orthogonal mode arcs will be added in 90 degree increments, and in diagonal mode arcs will be added in 45 degree increments. You can also specify a radius for an arc you are adding. These features provide you with total control over all arcs added to your designs
- **Protect While Routing** – The ability to protect traces as they are added was introduced in PowerPCB 4.0. This is extended in FIRE by providing even more control. You can enable or disable *protect while routing* at any time during routing. This lets you protect the whole net or just portions of it. Even when *protect while routing* is enabled, you can use the Backspace key to "backup" on the routed trace.

- **Interactive Component Placement** – With FIRE you can move components within BlazeRouter without returning to PowerPCB. In addition to the basic operations of moving, rotating, flipping, and spinning a component, with BlazeRouter you can reroute connections to a component either during a move or after the move is complete. This saves design time by minimizing the need to return to PowerPCB to move components and eliminates the need to manually reroute traces after moving a component.
- **Differential Pairs** – FIRE lets you interactively route differential pairs. During interactive routing, when one pin of a differential pair is selected, the pair is automatically selected and routed simultaneously. FIRE tries to equalize the shoulder length of the differential pair. When you want more control of the shoulder length, you can route them separately. Once the gathering point is reached, the differential gap will be maintained. If you want the differential pair to diverge, or separate temporarily around an obstacle such as a via, you can use the split command. For length-constrained differential pairs, you can use the length monitor to display the current length, and add accordions to increase the length if desired. FIRE's differential pair routing capabilities help users improve productivity, reduce design time, and meet all differential pair rules.
- **Accordions** – FIRE introduces unique aids for routing length-constrained signals. You can easily add accordions using your preferred parameters to add length to a trace. You can either set the amplitude and gap beforehand or define them as you are routing with the pointer.
- **Advanced Trace Length Monitor** – FIRE includes an advanced trace length monitor. As you add connections, the trace length monitor displays the minimum and/or maximum trace length on a graphic attached to the pointer. As the trace is routed, the estimated length to completion and actual trace length is updated dynamically. A progress indicator bar gives more graphical feedback before you complete the connection. The trace length monitor changes color: yellow when the trace length is less than the minimum length, green when the connection would meet the length constraints, and red if the trace exceeds the maximum length. You can display the complete net length or pin pair length, whichever is more important for you to monitor.
- **Navigation Window Enhancements** – Enhancements have been made to the BlazeRouter navigation window that provide graphical aids while routing length-constrained nets and matched length groups.

  Length-constrained nets in the vicinity of the pointer appear in color in the navigator window: yellow when less than the minimum; green when meeting the constraints; and red when exceeding the maximum. These colors are updated as nets are pushed and shoved in the vicinity of the net, providing up-to-the-minute feedback. Length constraints are also monitored while moving components.

  Graphical feedback is also given for all matched length groups: red when the estimated length is above the maximum length; green when it is within range; and yellow if the length is below the minimum length.

BlazeRouter

BlazeRouter has been a companion to PowerPCB since version 3.5. This version of the core autorouter includes many significant enhancements.

- **Vias at SMD** – Many of today's dense designs require vias to be drilled in surface mount pads. BlazeRouter now provides far more control of the placement of vias within pads, such as Center, End, and Fit.
- **Component Clearance and Routing Rules** – BlazeRouter 5.0 introduces Component Clearance and Routing rules – unique trace width and clearance rules associated with a component that allow better routability of today's high pin count, fine-pitched devices. You can set component clearance and routing rules to decals or individual components. Typically the trace width or clearance will be set tighter than the rules for the rest of the board. As BlazeRouter attempts to route out of a fine-pitch device where the recommended trace width and clearance do not allow routing without a violation, BlazeRouter automatically uses the new component clearance and routing rules. As the trace exits the component boundary it reverts back to the recommended width and clearance for the completion of the connection. This allows higher completion rates on today's dense designs, and shorter routing times by eliminating manual routing to these components.
- **Fanout Controls** – Control of the fanout of surface mount devices has been extended. Fanout can now be controlled by decal or by individual component.
- **Pad Entry Controls** – Automatic control of pad entry has also been extended. You can now control pad entry by decal or by individual component.
- **Center** – A new routing pass type, Center, has been added to BlazeRouter 5.0. Center adjusts traces between pads (component and adjacent via pads) equalizing the space between the pads and traces. This maximizes the space between these objects, minimizing the possibility of a short and increasing the yield in manufacturing.
- **Performance Improvements** – BlazeRouter performance has been significantly enhanced for large designs.
- **Prerouting Analysis** – You can now use BlazeRouter 5.0 to run a prerouting analysis of your design at any time. The prerouting analysis performs over 30 checks of settings that could effect the routability of a board, including grid settings, plane nets, pad entry controls, thermal status, disabled layers, and maximum lengths. This prevents time wasted from trying to route designs with setup errors or unroutable constraints.

BlazeRouter HSD

New to PowerPCB 5.0, BlazeRouter High-Speed Design (HSD) allows the automatic batch routing of geometric high-speed constraints.

- **Minimum, Maximum, and Matched Length** – BlazeRouter HSD automatically routes nets and pin pairs that have minimum and/or maximum length constraints assigned to them. If the router needs to add length to meet a minimum length requirement, accordions (a specific trace geometry, where the user can set the amplitude and the minimum gap) will be added. BlazeRouter HSD also automatically routes matched length nets and pin pairs. You can define a group of nets or pin pairs to automatically route to the same, or matched, length. For further control of matched lengths, you can set a tolerance, as well as assign minimum and/or maximum length requirements. The automatic routing of these length-constrained nets significantly reduces routing times and improves the quality of a design by meeting all length requirements of the design.
- **Differential Pairs** – BlazeRouter HSD automatically routes differential pairs – two signals that must be routed together from source pins to destination pins at a fixed gap. You can set the route gap and assign minimum and maximum length constraints. Differential pairs can also have matched lengths. If you allow differential pairs to separate around obstacles such as vias or component pins, you can control the number of obstacles, as well as the maximum obstacle size. Previously, routing differential pairs was a manual, therefore time-consuming and potentially error prone, process. Automatic routing of differential pairs not only reduces routing times, but also improves the quality of designs by meeting all differential pair constraints.
- **Tune** – A new routing pass type, Tune, has been added to BlazeRouter HSD. Tune looks at routed traces with length rules. If the trace does not meet the length constraint, or if the constraint has changed, Tune adjusts the trace length accordingly. This saves the designer time from manually adjusting the trace to within tolerance, and eliminates the potential for signal integrity problems due to trace length errors.
- **Net Rescheduling** – Now with BlazeRouter you can manually define the net topology, specifying the exact order in which to connect a net. You can select a signal and set the pins in the order in which they should be routed. The connections update according to the new topology and are automatically protected, insuring that BlazeRouter connects the net in the specified order, meeting all net scheduling requirements.

Design Verification

The ability to do batch design rule checking of all the new rules introduced in PowerPCB 5.0 is included. Verification of all physical rules in your design gives you the confidence that the design meets all your constraints. You can verify the design from either BlazeRouter or PowerPCB.

- **Clearance** – Full edge-to-edge clearance checking is done including net-to-all objects, board outline, off board text, keepouts, and same net clearance checking.
- **Length Constraints** – All length constraints are verified including minimum and maximum lengths and matched lengths.
- **Differential Pair Checking** – Complete and customizable checking of differential pairs is included. You can specify a minimum percentage that the routed differential pair must be at the specified gap, and then review the reported errors graphically. Design Verification also checks the maximum length of irregular trace segments. This detects differential pairs whose two signals vary in length by a specified amount. This verifies that differential pairs meet your specifications.
- **Fabrication** – Fabrications checks include acid trap detection, sliver detection, component checking (body-to-body, maximum top height, and maximum bottom height), drill-to-drill spacing checks, minimum pad and trace sizes, and vias at SMD.
- **Testability** – Extensive test point checking is included in Design Verification. Checks include probe clearances, minimum via and pad sizes for probing, SMD pin probing, test points on component pins on the component side, test point count per net settings and nail diameter settings.
- **Ignore Errors** – A long-standing customer enhancement request has been addressed with the new error checking in PowerPCB 5.0. Because error markers are selectable database objects in BlazeRouter, the user can assign an “ignore” status to an error marker, allowing Design Verification to disregard violations during subsequent checking, allowing 100% clean verification runs once these errors are identified as false errors. Also included is a switch to “turn on” all these ignored errors at any time for validation that they should be ignored.
- **Spreadsheet View** – Errors discovered by design verification appear in the new spreadsheet view. In the spreadsheet view you can expand these error messages for more detailed information including highlighting the related objects, linking to the related rules, and linking to the dialog boxes where you can correct the error condition.

GUI Customization

The user now has more control of the BlazeRouter graphical user interface. This includes the ability to customize existing toolbars, shortcut keys, and menus, or to define entirely new ones. You can define unique icons. You can also create and access macros from toolbars, shortcuts, and menus. You can share your customizations with coworkers by saving them as an XML file. This increased control of your environment lets you work more efficiently and customize BlazeRouter to the unique needs of your work environment.

Advanced Packaging Toolkit

PowerPCB users now have all the tools and utilities available to optimize their design process when bare die are required. The new Advanced Packaging Toolkit option provides significant functionality to aid in the design of chip-on-board, single chip, and multi-chip modules. This option includes all the functionality that was previously available in only the PowerBGA product.

- **Die Wizard** – PowerPCB's Die Wizard provides the flexibility to construct die part models using the die description data contained in GDSII or ASCII files as output from IC design systems. Importing the native GDSII or ASCII die files directly into PowerPCB streamlines the design process, simplifies data transfer, and eliminates translation errors.

  In cases where the GDSII file contains additional data above and beyond the die description, die-specific data can be extracted easily. Missing information is easily augmented and existing data can be modified using the parameters contained in the Wizard's construction templates. When GDSII or ASCII data is unavailable for import, the Die Wizard's parametric construction capability can be used to craft a die part. The Die Wizard is launched from the Advanced Packaging Toolkit and presents the three options for creating a die part: importing from an ASCII text file, importing from a GDSII file, and parametric construction.

- **Wire Bond Wizard** – The Wire Bond Wizard provides one-stop definition for all constraints and parameters necessary to automatically generate wire bond fanout patterns within PowerPCB. Once you select a die part in the layout editor, you can launch the Wire Bond Wizard from the Advanced Packaging Toolkit. Parameters and constraints are presented in logical groups enabling simplified setup and iterative exploration. As you make net assignments and specify wire bond strategies, dynamic previewing provides immediate feedback on your selections.

  The Wire Bond Wizard supports both symmetrical and asymmetrical wire bond fanouts enabling mixed strategies on the same die. The Wire Bond Wizard tries to place substrate bond pads in compliance with the specified assembly rules. In the event of insufficient area, substrate bond pads are placed and violations reported enabling you to easily experiment with different strategies and visualize the results.
- **Die Flag Wizard** – Once you select a die part in the layout editor, you can launch the Die Flag Wizard from the Advanced Packaging Toolkit. The Die Flag Wizard presents all the parameters necessary to construct die flags and rings. The layout window dynamically updates as you enter the parameters.

  To save time and streamline the design process, parameters to define the solder mask openings for the die flag and rings are also included in the Die Flag Wizard. Once you are satisfied with the parameters, the die flag and rings are automatically constructed on their assigned layers using copper shapes. Once these shapes are created, you can modify them using standard editing functions.
- **Route Wizard** – PowerPCB offers new automatic routing functions that complete the any-angle interconnects for a wire-bonded die within BGA/CSP packages. This eliminates considerable time and effort by following the designer's methodology and providing high completion rates. Many package substrates require electroplating connections for fabrication. If not considered up front, a design may prove to be an unfeasible fit for the integrated circuit very late in the design cycle. The Route Wizard integrates plating tail autorouting into initial connection optimization. This maximizes feasibility feedback, ensuring proper package selection, and eliminates tedious, time-consuming manual efforts.

P.N. 216037

PowerLogic 5.0
Release Highlights

Welcome to the latest release of PowerLogic. PowerLogic 5.0 is a new release that provides compatibility with PowerPCB 5.0 and addresses issues frequently requested by our customers and Partners.

Below is a brief list of the new and enhanced PowerLogic 5.0 functionality.

- **PDF output to Adobe® Acrobat™ Writer** – PowerLogic now supports output of multiple schematic sheets into a single PDF document. This happens automatically in the Print/Plot command when Adobe Acrobat Writer is the selected printer and multiple sheets are selected for printing.
- **PowerLogic Installation** – The PowerLogic installation program has been upgraded to match PowerPCB 5.0 and provide increased compatibility with Windows 2000 and Windows XP.
- **Clearance Rules** – PowerLogic's Clearance Rules dialog box has been updated to support PowerPCB 5.0. A new Drill-to-Copper clearance has been added to the Clearance rules matrix. The Text row was removed and the Drill row added to the Conditional rules matrix for consistency with PowerPCB 5.0.
- **Routing Rules** – PowerLogic's Routing Rules dialog box has been updated to support PowerPCB 5.0. The Copper Sharing option has been replaced with separate options for Trace Sharing and Via Sharing. The Horizontal and Vertical Length Minimization controls have been removed for consistency with PowerPCB 5.0. Designs with horizontal or vertical length minimization will be converted to Total Length when loaded into PowerLogic 5.0.
- **Group Operations** – Defect fixes have been made to help preserve existing reference designators, gate suffixes, and pin numbers where possible. When a group is copied within a sheet, the new component reference designators are maintained in the same numerical order. When a paste from a group or group file is performed, the pin order and pin numbers on connectors are now preserved.
- **Defect Fixes** – Many other defect fixes have been resolved – see the file **customer_fixes.txt** located on the root of the distribution CD-ROM.