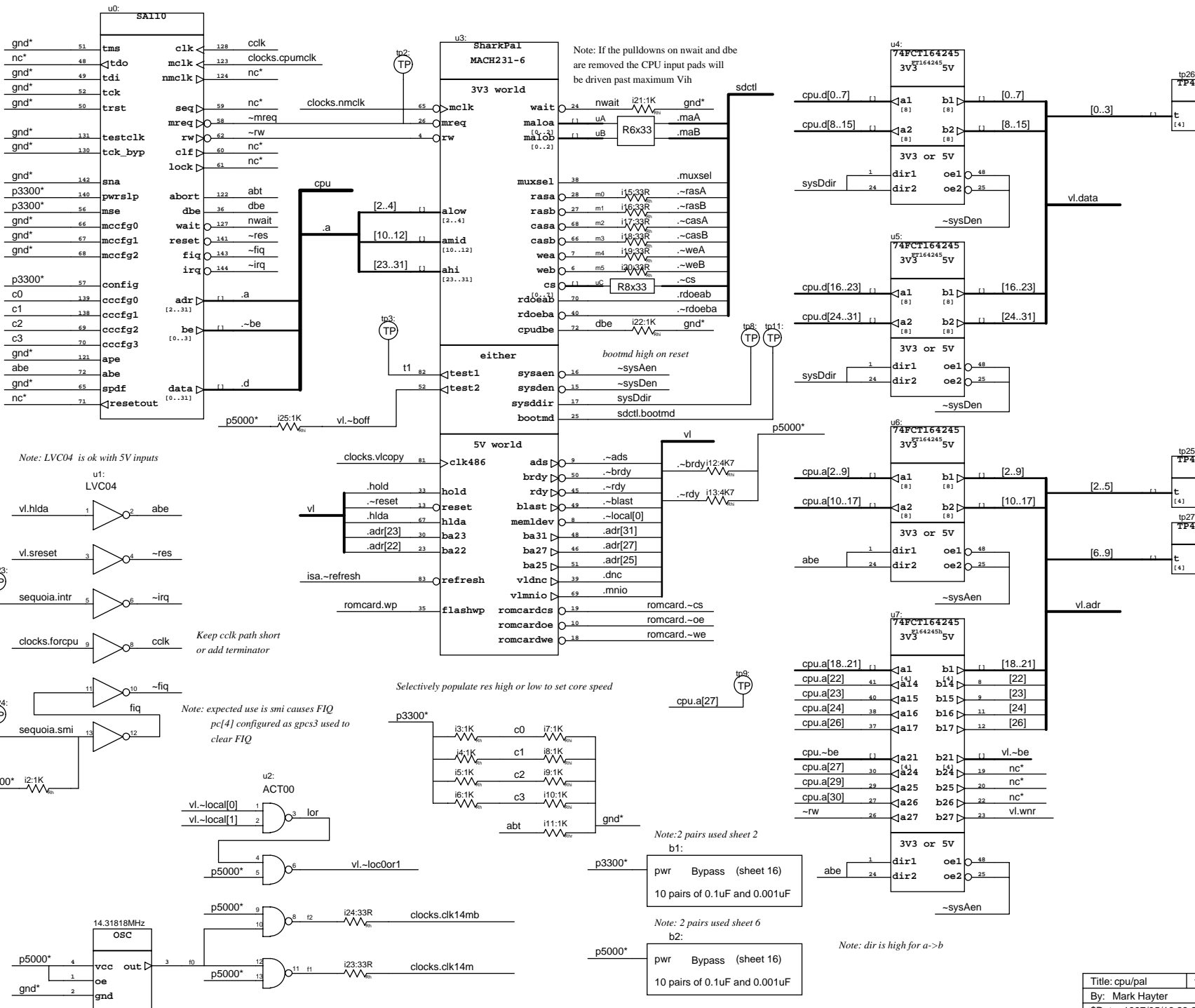


Sheets 13 to 16 show the bypass capacitors and are included as required by the other sheets



Note: If the pulldowns on nwait and dbc are removed the CPU input pads will be driven past maximum Vih

bootmd high on reset

Selectively populate res high or low to set core speed

Note: 2 pairs used sheet 2

Note: 2 pairs used sheet 6

Note: dir is high for a->b

Note: LVC04 is ok with 5V inputs

Note: expected use is smi causes FIQ  
pc[4] configured as gpes3 used to clear FIQ

ACT00

b1:  
pwr Bypass (sheet 16)  
10 pairs of 0.1uF and 0.001uF

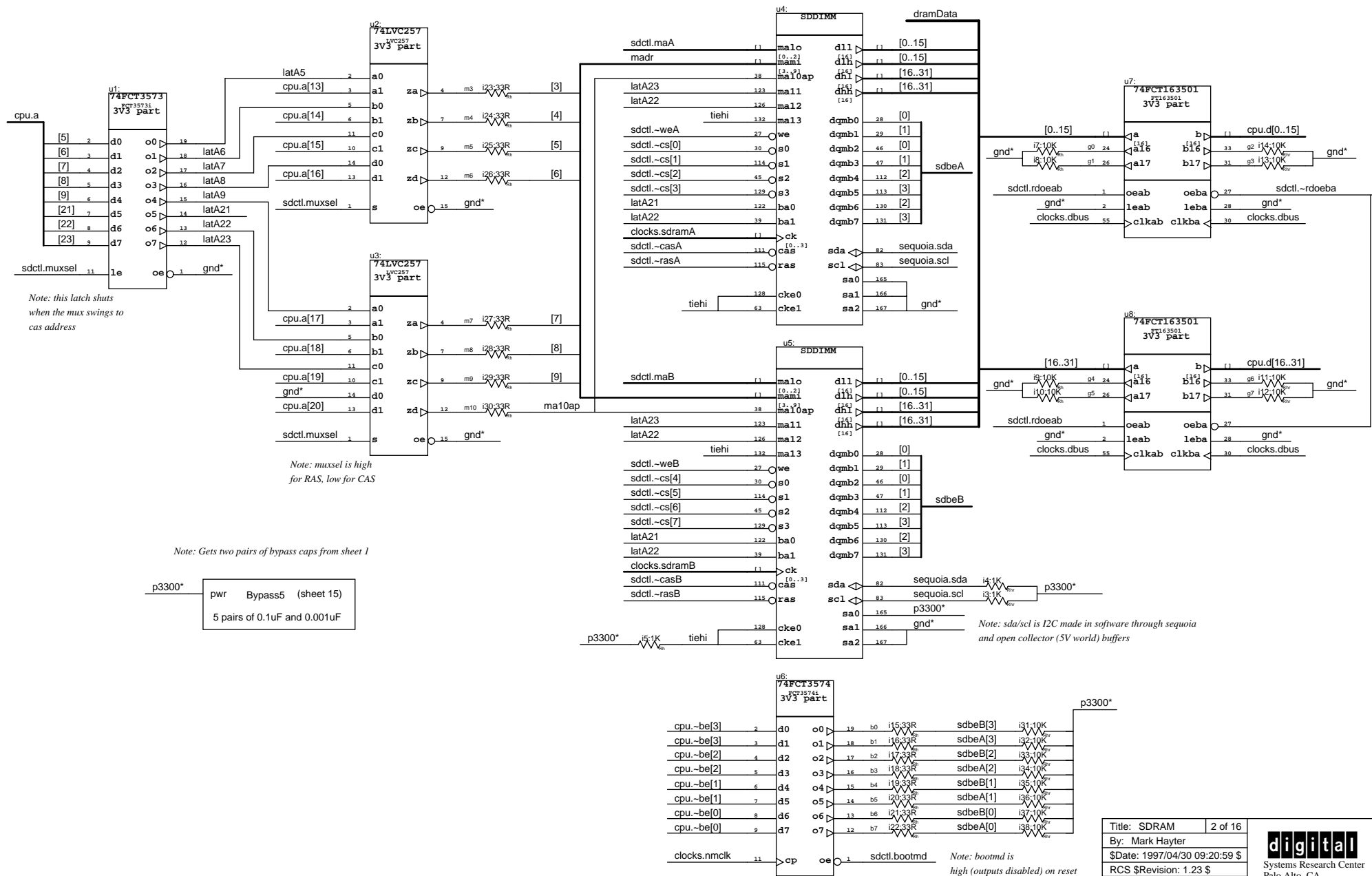
b2:  
pwr Bypass (sheet 16)  
10 pairs of 0.1uF and 0.001uF

Title: cpu/pal	1 of 16
By: Mark Hayter	
\$Date: 1997/05/16 23:22:15 \$	
RCS \$Revision: 1.36 \$	
Version: Rev 4	



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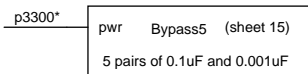
Note: the slightly perverse assignment of the 32 data bits to the 64 sdrAm bits results from the way CS0 and CS2 are connected on the module



Note: this latch shuts when the mux swings to cas address

Note: muxsel is high for RAS, low for CAS

Note: Gets two pairs of bypass caps from sheet 1



Note: sda/scl is I2C made in software through sequoia and open collector (5V world) buffers

Note: bootmd is high (outputs disabled) on reset

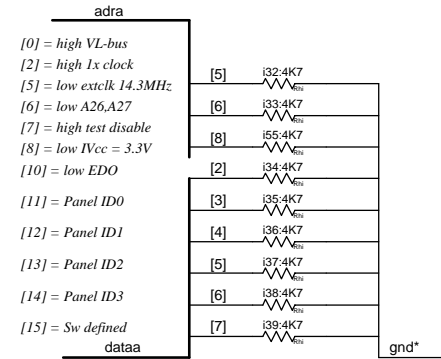
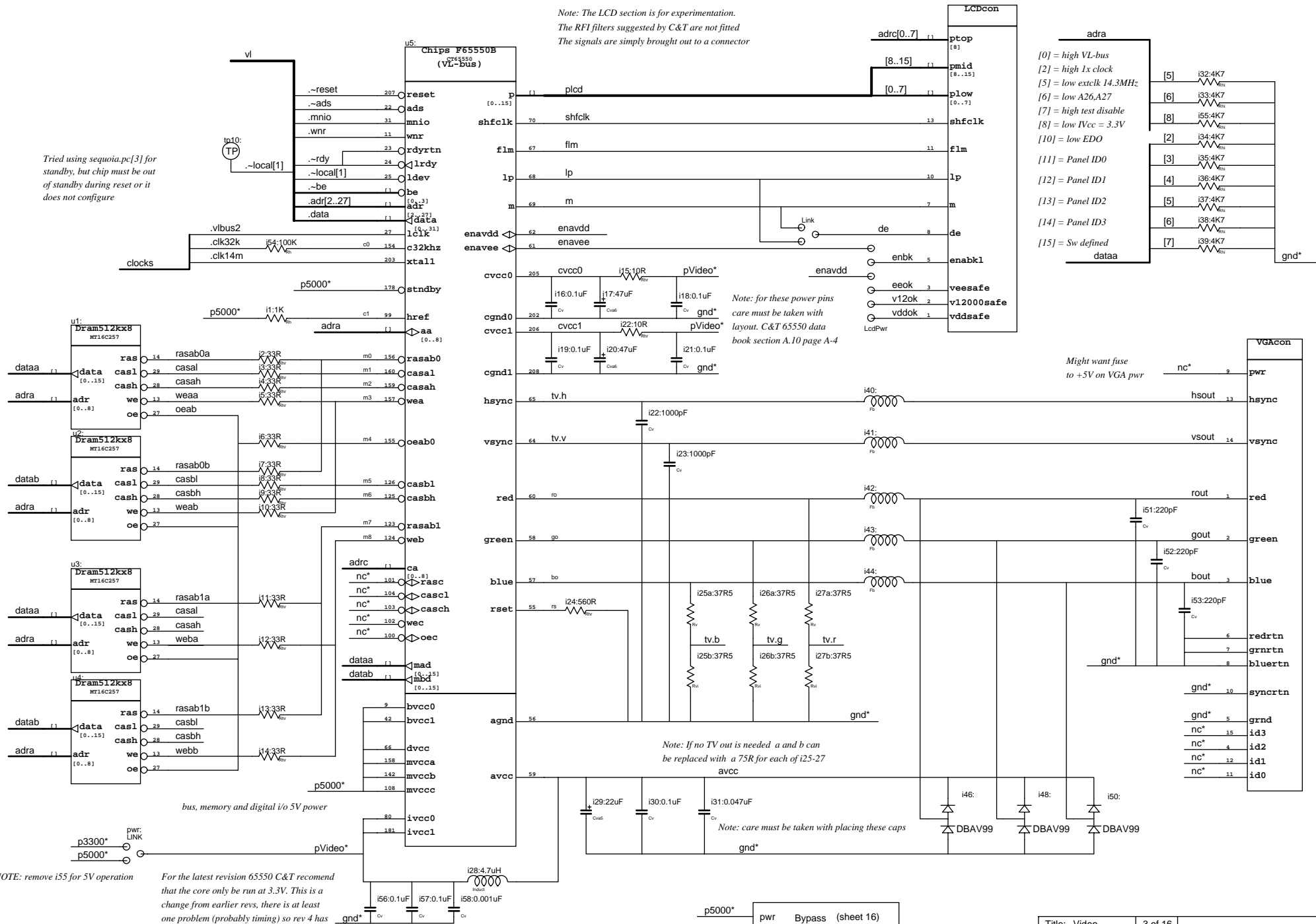
Title: SDRAM	2 of 16
By: Mark Hayter	
\$Date: 1997/04/30 09:20:59 \$	
RCS \$Revision: 1.23 \$	
Version: Rev 4	



Note: This connector has the same pinout as the C&T development kit connector

Note: The LCD section is for experimentation.  
The RFI filters suggested by C&T are not fitted  
The signals are simply brought out to a connector

Tried using sequoia.pc[3] for standby, but chip must be out of standby during reset or it does not configure



Might want fuse to +5V on VGA pwr

Note: If no TV out is needed a and b can be replaced with a 75R for each of i25-27

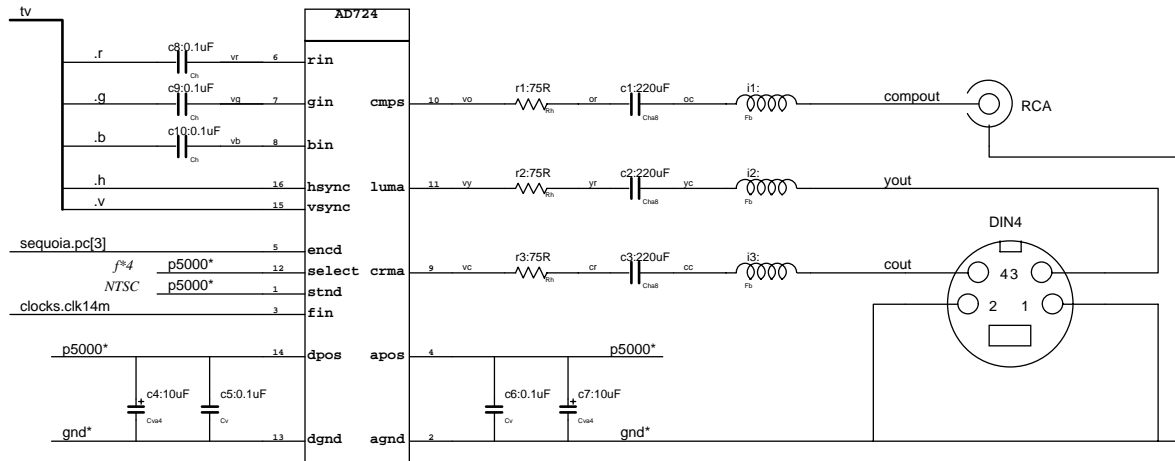
Note: care must be taken with placing these caps

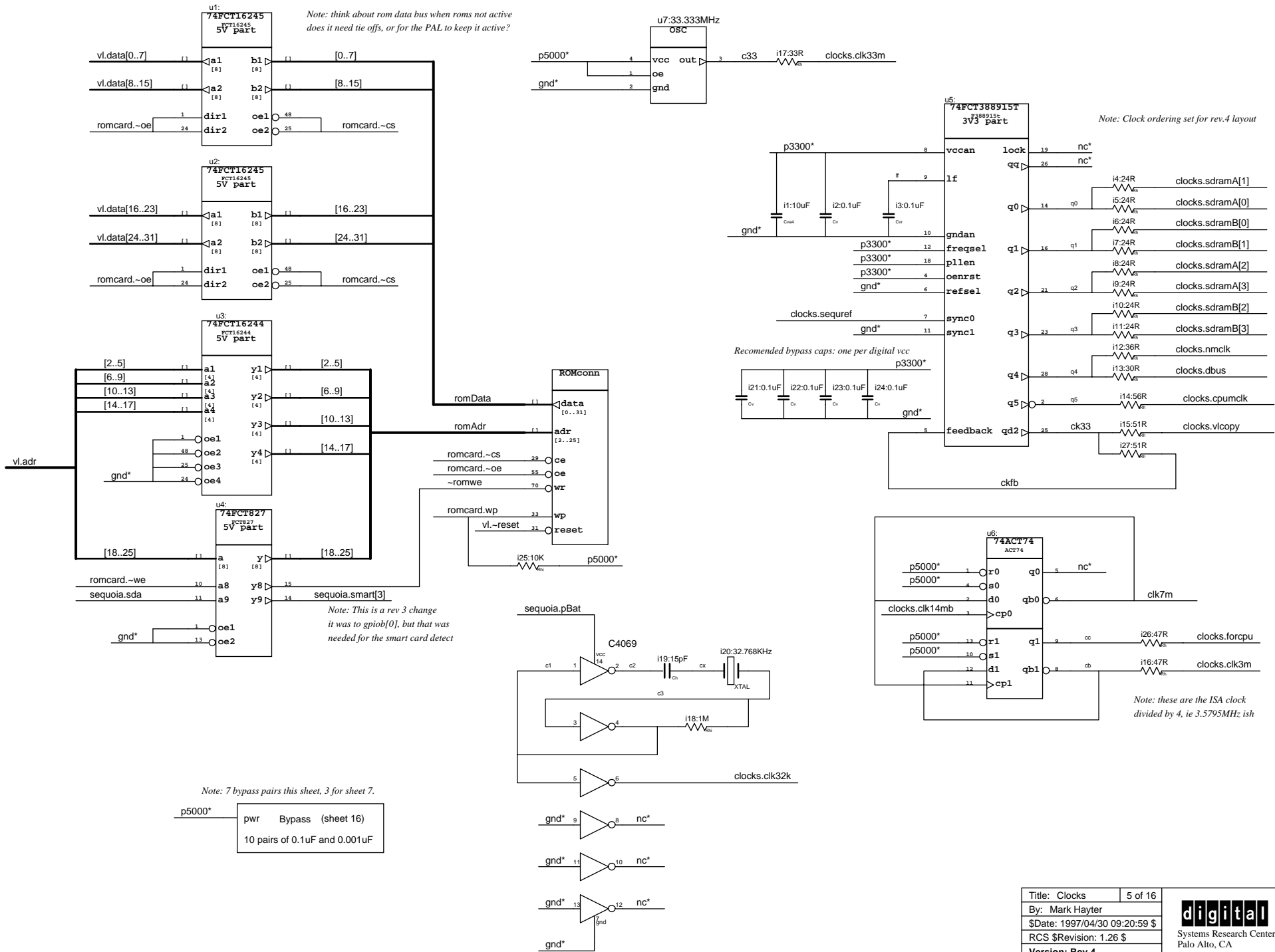
NOTE: remove i55 for 5V operation

For the latest revision 65550 C&T recomend that the core only be run at 3.3V. This is a change from earlier revs, there is at least one problem (probably timing) so rev 4 has a link to allow both voltages

Note: i24, the 560R res on rset must be 1% or better  
i25, i26 and i27 pulldowns must be 2% or better

p5000\* pwr Bypass (sheet 16)  
10 pairs of 0.1uF and 0.001uF





Note: think about rom data bus when roms not active does it need tie offs, or for the PAL to keep it active?

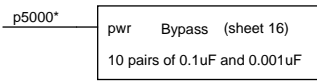
Note: Clock ordering set for rev.4 layout

Recommended bypass caps: one per digital vcc p3300\*

Note: This is a rev 3 change it was to spiob[0], but that was needed for the smart card detect

Note: 7 bypass pairs this sheet, 3 for sheet 7.

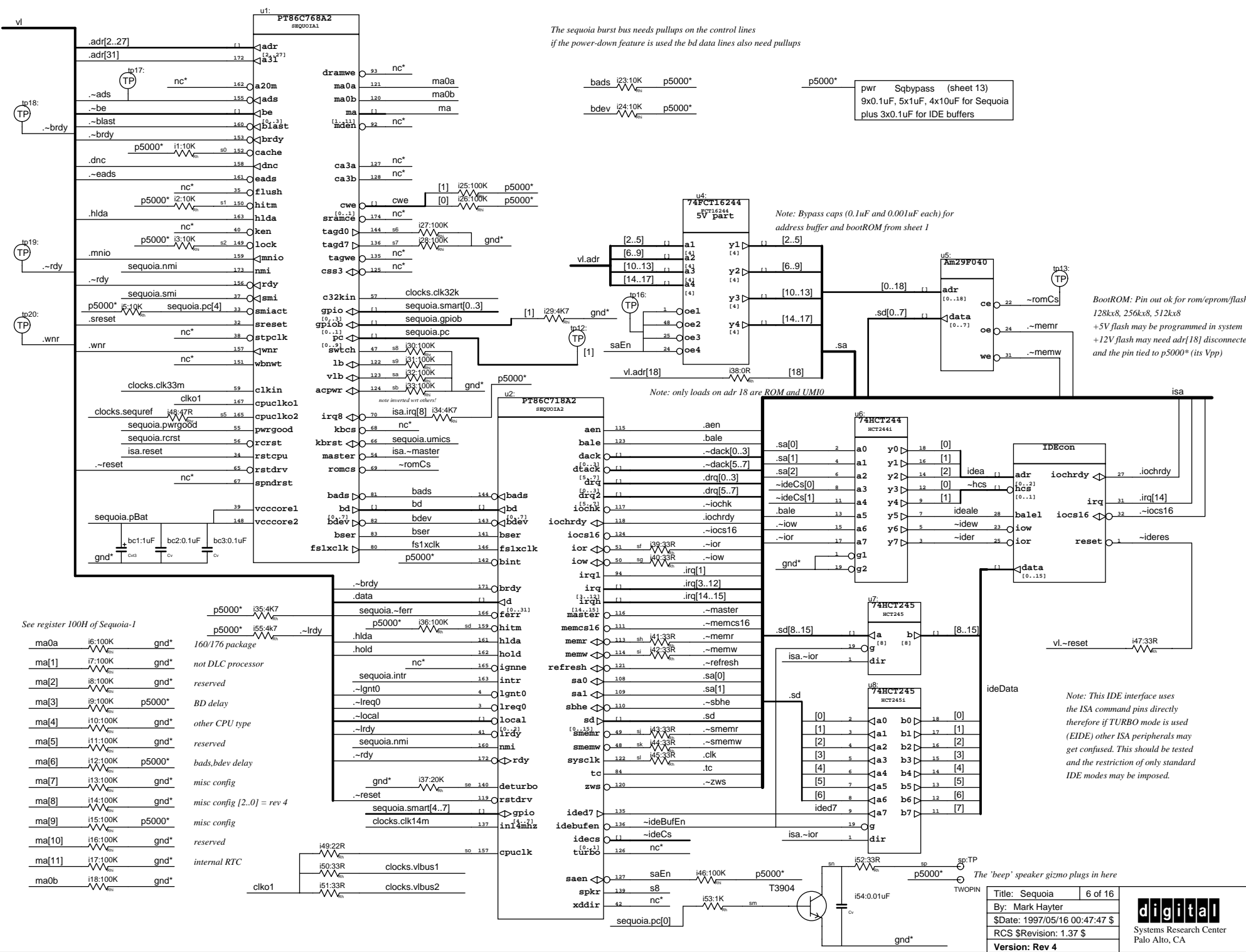
Note: these are the ISA clock divided by 4, ie 3.3795MHz: ish



Title: Clocks	5 of 16
By: Mark Hayter	
\$Date: 1997/04/30 09:20:59 \$	
RCS \$Revision: 1.26 \$	
Version: Rev 4	



The sequoia burst bus needs pullups on the control lines  
if the power-down feature is used the bd data lines also need pullups



p5000\* pwr Sqbypass (sheet 13)  
9x0.1uF, 5x1uF, 4x10uF for Sequoia  
plus 3x0.1uF for IDE buffers

Note: Bypass caps (0.1uF and 0.001uF each) for  
address buffer and bootROM from sheet 1

BootROM: Pin out ok for rom/eprom/flash  
128Kx8, 256Kx8, 512Kx8  
+5V flash may be programmed in system  
+12V flash may need adr[18] disconnected  
and the pin tied to p5000\* (its Vpp)

Note: only loads on adr 18 are ROM and UM10

See register 100H of Sequoia-1

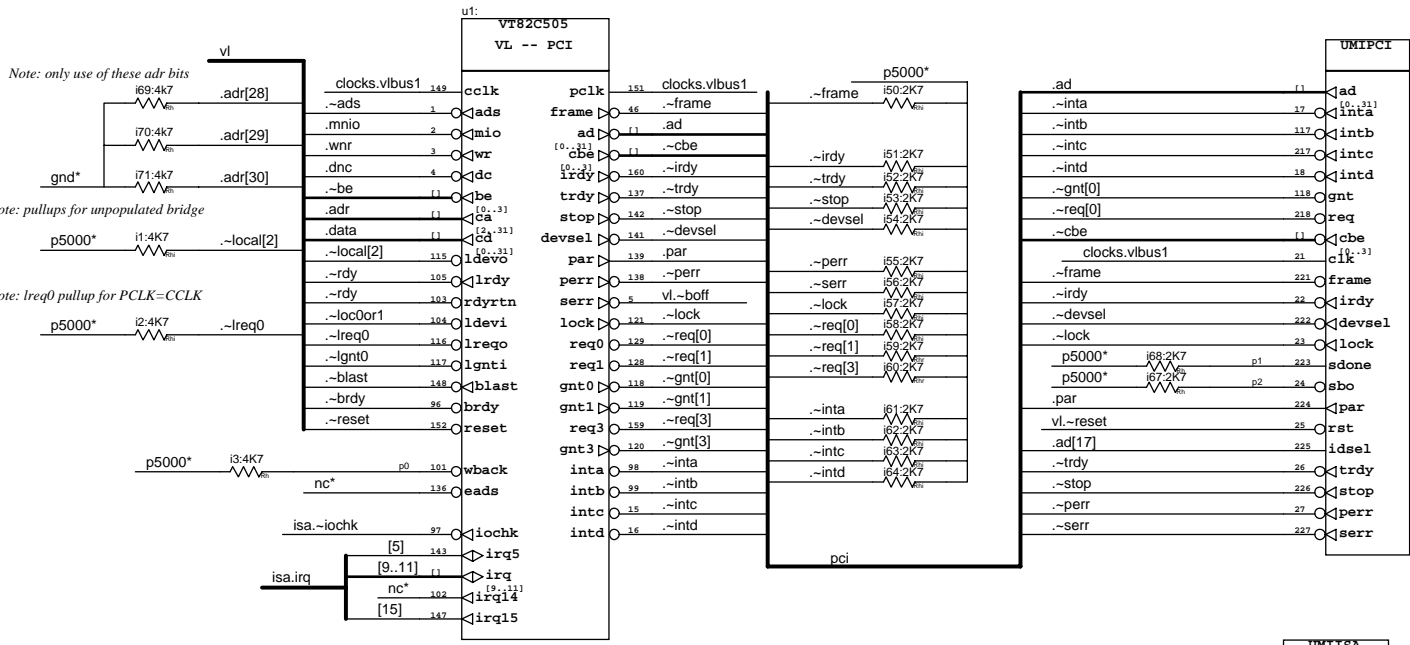
ma0a	i6:100K	gnd*	160/176 package
ma[1]	i7:100K	gnd*	not DLC processor
ma[2]	i8:100K	gnd*	reserved
ma[3]	i9:100K	p5000*	BD delay
ma[4]	i10:100K	gnd*	other CPU type
ma[5]	i11:100K	gnd*	reserved
ma[6]	i12:100K	p5000*	bads,bdev delay
ma[7]	i13:100K	gnd*	misc config
ma[8]	i14:100K	gnd*	misc config [2..0] = rev 4
ma[9]	i15:100K	p5000*	misc config
ma[10]	i16:100K	gnd*	reserved
ma[11]	i17:100K	gnd*	internal RTC
ma0b	i18:100K	gnd*	

Title: Sequoia 6 of 16  
By: Mark Hayter  
\$Date: 1997/05/16 00:47:47 \$  
RCS \$Revision: 1.37 \$  
Version: Rev 4



Configuration links

p5000\* i73:4K7 pci.-gnt[0] *clk synchronous*  
 p5000\* i17:4K7 pci.-gnt[1] *Select IRQ14,15 not req/gnt2*  
 p5000\* i18:4K7 pci.-gnt[3] *Select blast not hiaddr*



Note: only use of these adr bits

Note: pullups for unpopulated bridge

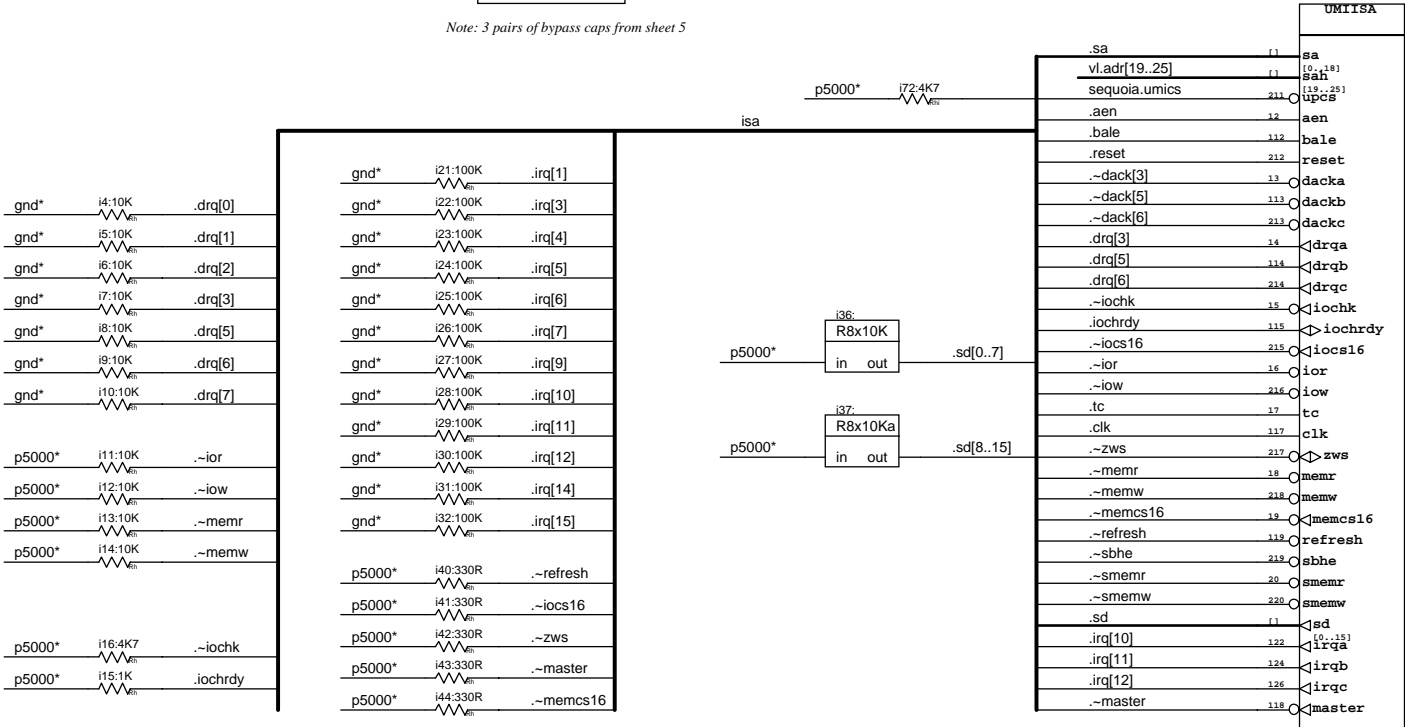
Note: lreq0 pullup for PCLK=CCLK

Note: idsel comes from ad[17]. Don't care about loading since there is only one UMI slot. Additional PCI devices could use ad[18..31] but then loading might become an issue.

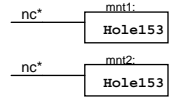
This selection makes the UMI slot be PCI config device 6

Note: Only config type 0 cycles supported by VIA chip, so no bridges on the UMI

Note: 3 pairs of bypass caps from sheet 5



These are two holes for standoffs to fix the umi cards. Basically 0.153 hole with min .180 clearance

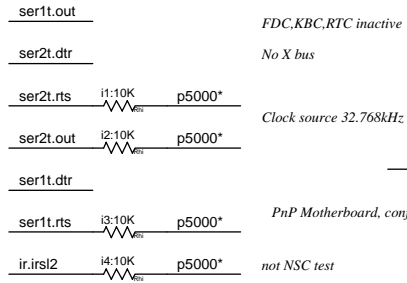


Note: umics may be useful for upper address bit decoding  
 Note: address lines 19..25 are not used on internal isa nor by most networking chips, so they come unbuffered from the vl bus



Note: National recommend six 0.1uF bypass caps

Note: Internal 30k pulldown



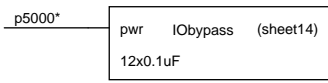
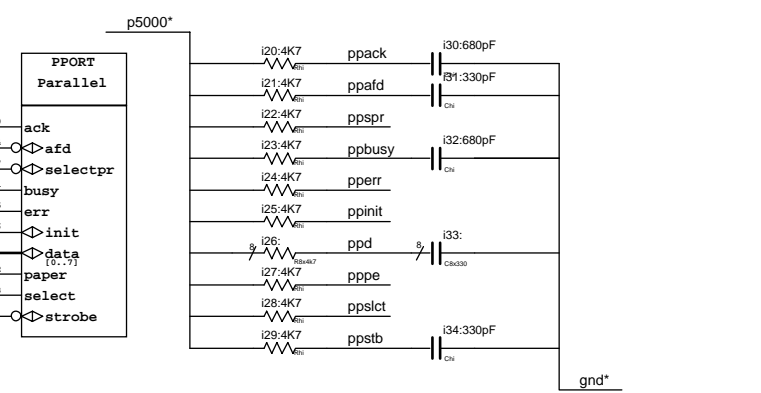
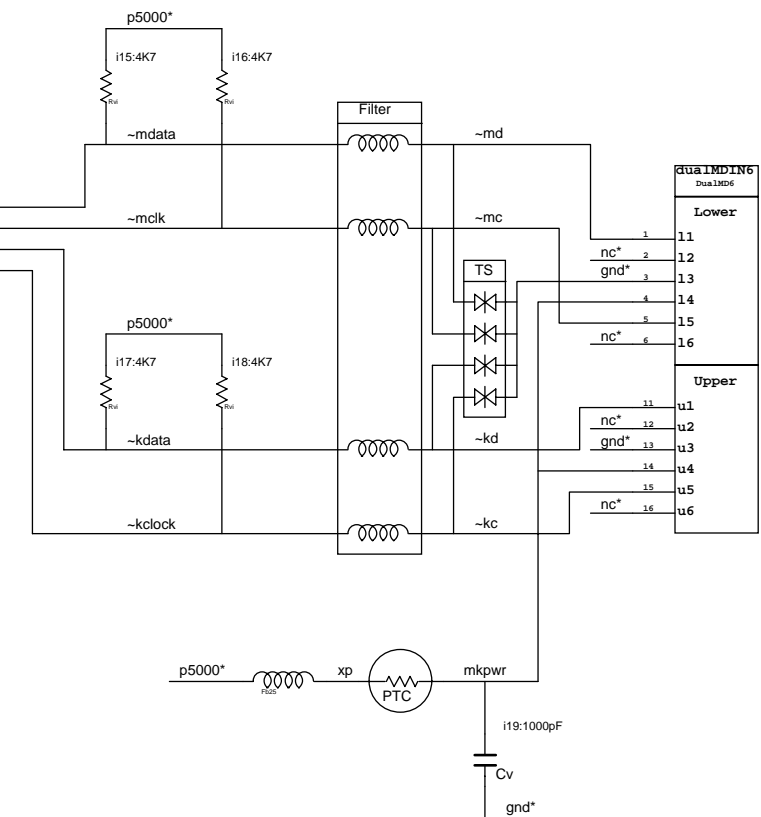
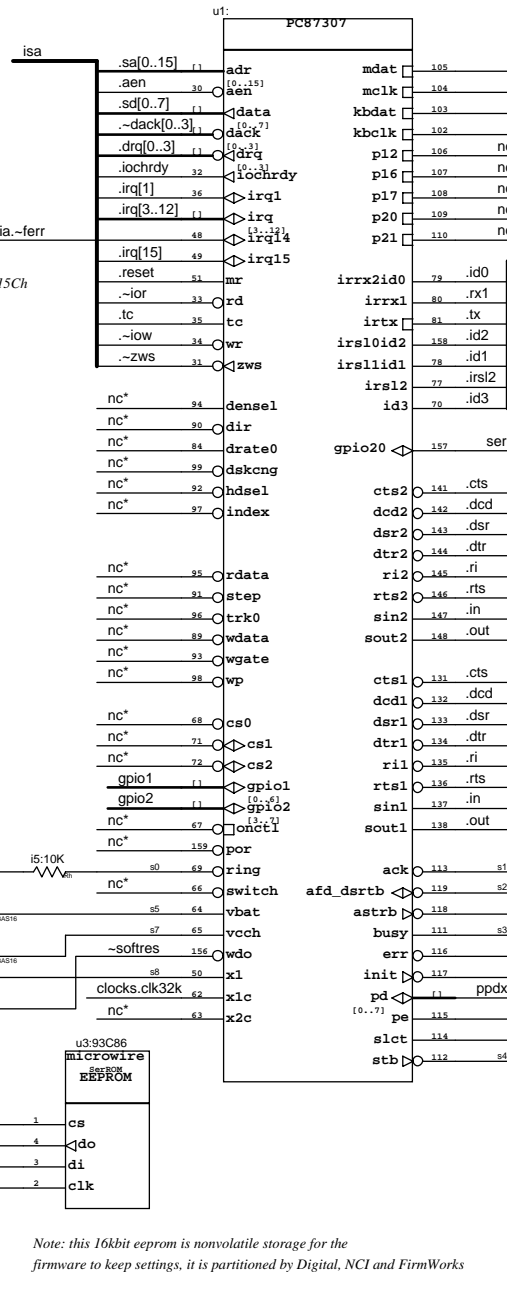
FDC,KBC,RTC inactive

No X bus

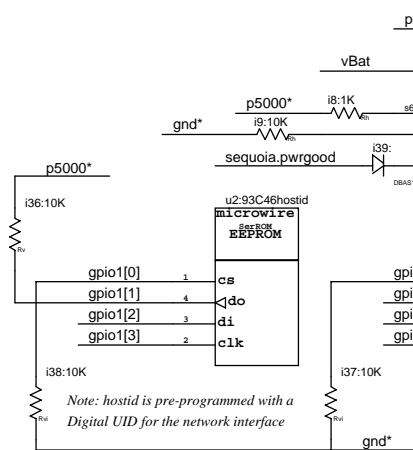
Clock source 32.768kHz

PnP Motherboard, config @015Ch

not NSC test

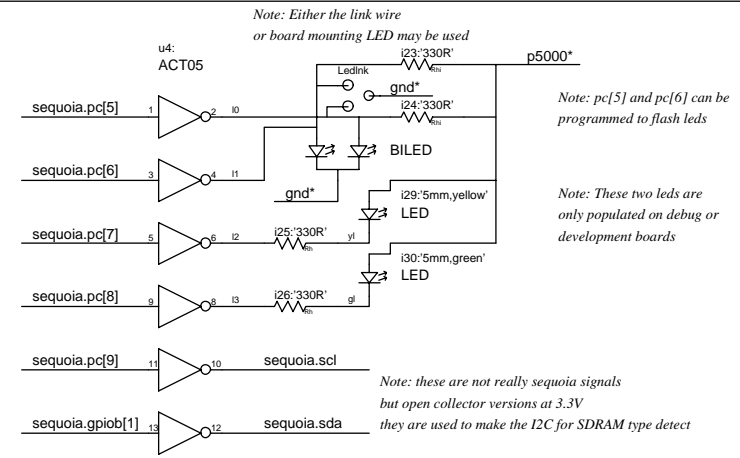
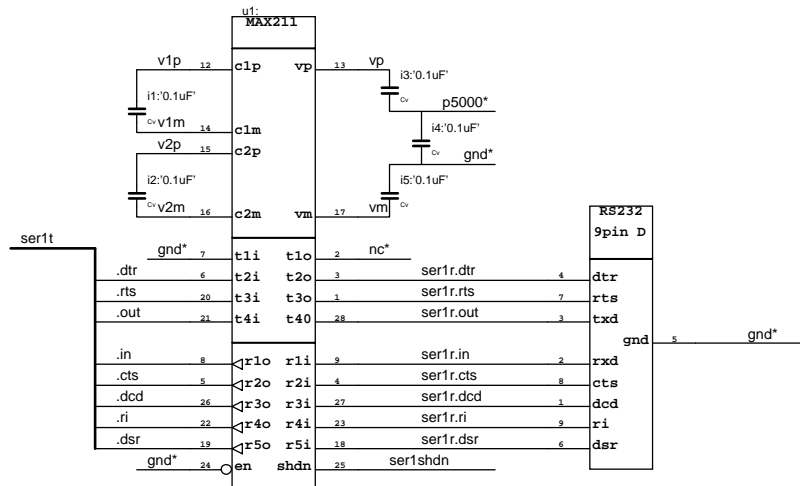


Note: Six of these go to sheet 9



Note: hostid is pre-programmed with a Digital UID for the network interface

Note: this 16kbit eeprom is nonvolatile storage for the firmware to keep settings, it is partitioned by Digital, NCI and FirmWorks



Note: Either the link wire or board mounting LED may be used

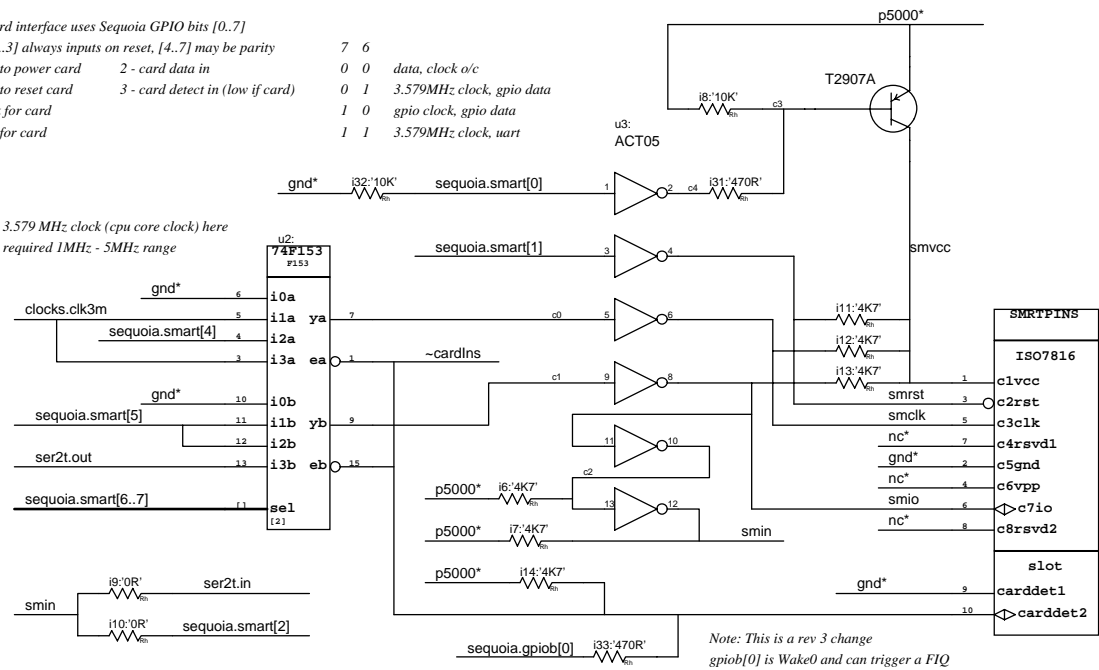
Note: pc[5] and pc[6] can be programmed to flash leds

Note: These two leds are only populated on debug or development boards

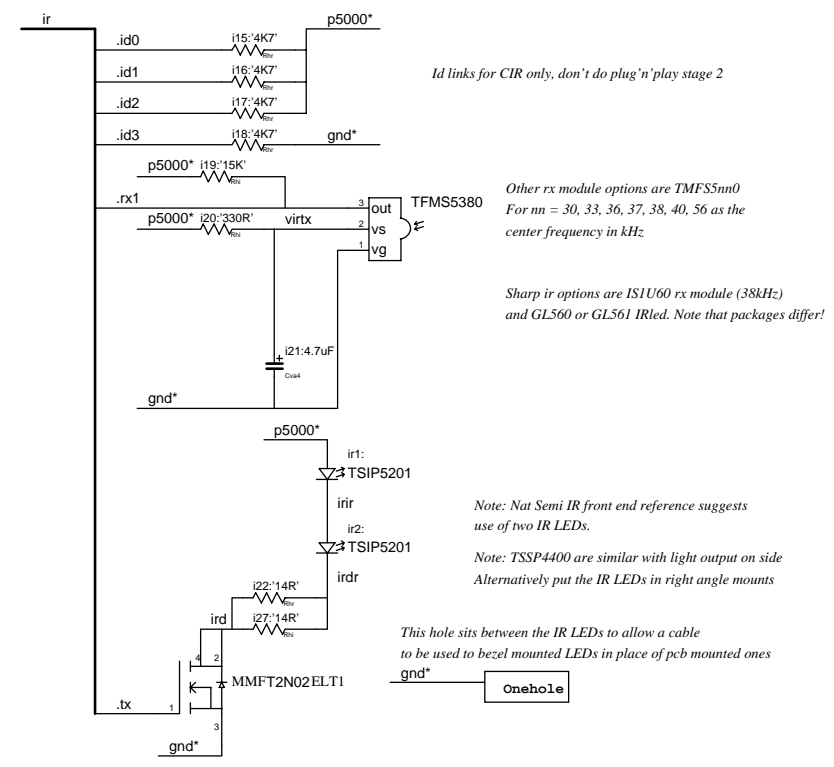
Note: these are not really sequoia signals but open collector versions at 3.3V they are used to make the I2C for SDRAM type detect

Smartcard interface uses Sequoia GPIO bits [0..7]  
 Smart[0..3] always inputs on reset, [4..7] may be parity  
 0 - high to power card    2 - card data in  
 1 - high to reset card    3 - card detect in (low if card)  
 4 - clock for card  
 5 - data for card

Note: Use 3.579 MHz clock (cpu core clock) here  
 It is in the required 1MHz - 5MHz range



Note: This is a rev 3 change  
 gpio[0] is Wake0 and can trigger a FIQ  
 both on card insert and card removal



Id links for CIR only, don't do plug'n'play stage 2

Other rx module options are TMFS5m0  
 For nn = 30, 33, 36, 37, 38, 40, 56 as the center frequency in kHz

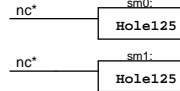
Sharp ir options are IS1U60 rx module (38kHz)  
 and GL560 or GL561 IRled. Note that packages differ!

Note: Nat Semi IR front end reference suggests use of two IR LEDs.

Note: TSSP4400 are similar with light output on side  
 Alternatively put the IR LEDs in right angle mounts

This hole sits between the IR LEDs to allow a cable to be used to bezel mounted LEDs in place of pcb mounted ones

These holes are for supports for the smartcard reader when a bare board is used

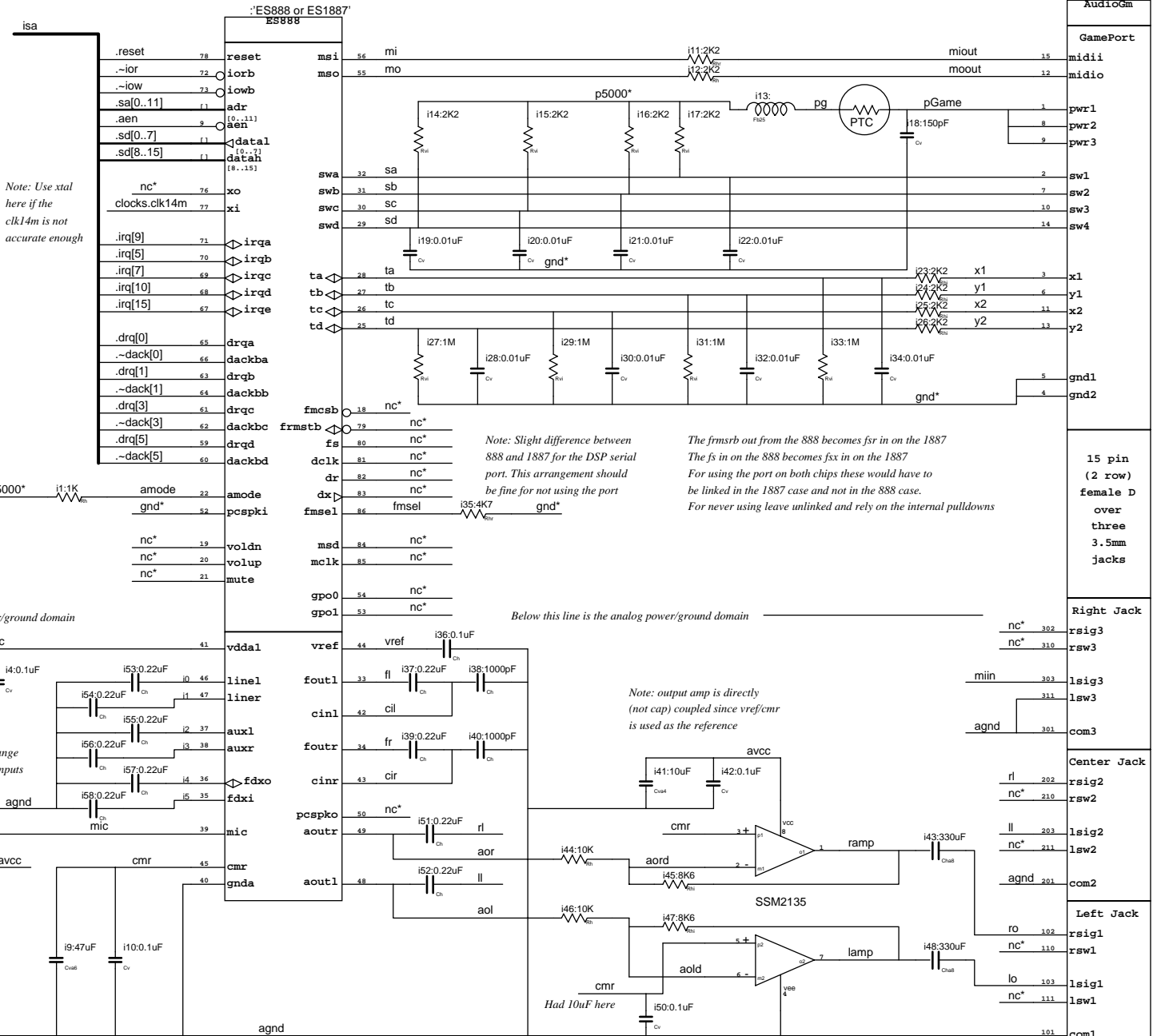


Title: Serial I/O	9 of 16
By: Mark Hayter	
\$Date: 1997/05/12 00:28:29 \$	
RCS \$Revision: 1.29 \$	
Version: Rev 4	

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The audio is designed to use either the ES888 or ES1887 codec  
 The main difference is that the 1887 includes FM synth, it is also more expensive (about \$3 more)  
 The 1887 is also slightly more configurable  
 Software for the 888 should work with the 1887 apart from a few lines of setup code (and the lack of synth)

Note: four 0.1uF bypass capacitors (as suggested by ESS) shown on sheet 11



Note: Use xtal here if the clk14m is not accurate enough

Note: Slight difference between 888 and 1887 for the DSP serial port. This arrangement should be fine for not using the port

The fmsrb out from the 888 becomes fsr in on the 1887  
 The fs in on the 888 becomes fsx in on the 1887  
 For using this port these would have to be linked in the 1887 case and not in the 888 case.  
 For never using leave unlinked and rely on the internal pulldowns

Below this line is the analog power/ground domain

Below this line is the analog power/ground domain

Note: Care with layout  
 Need single connection point for agnd to gnd

Note: rev 4 change tie off unused inputs

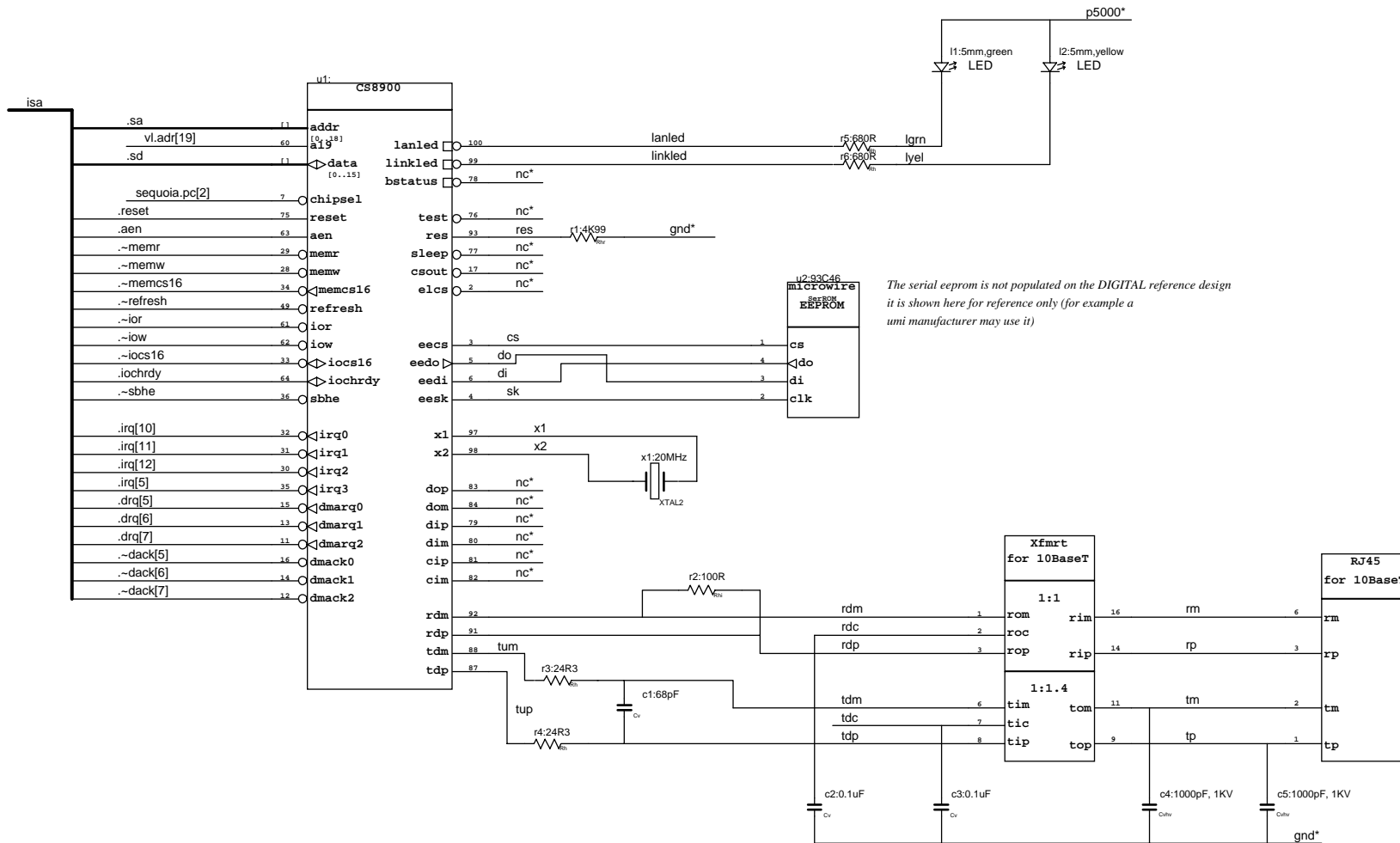
Note: output amp is directly (not cap) coupled since vref/cmr is used as the reference

Mike input is on combo connector on right of this page

Had 10uF here

Title: Audio	10 of 16
By: Mark Hayter	
\$Date: 1997/05/17 00:51:49 \$	
RCS \$Revision: 1.32 \$	
Version: Rev 4	

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 Palo Alto, CA

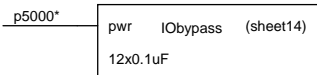


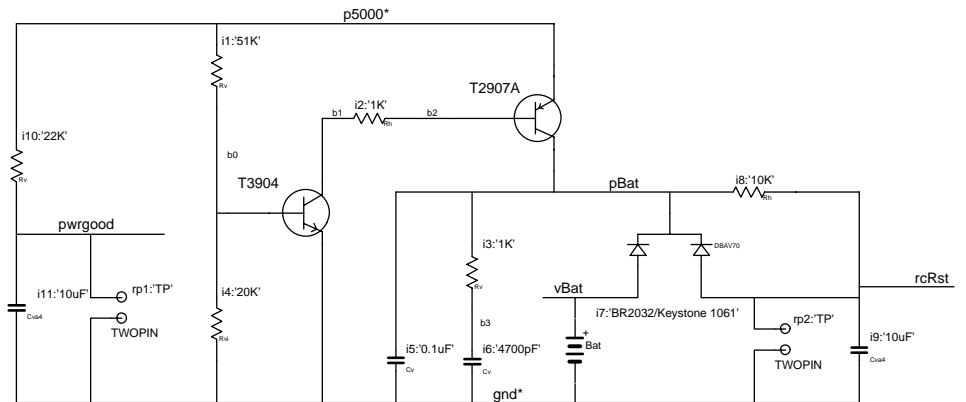
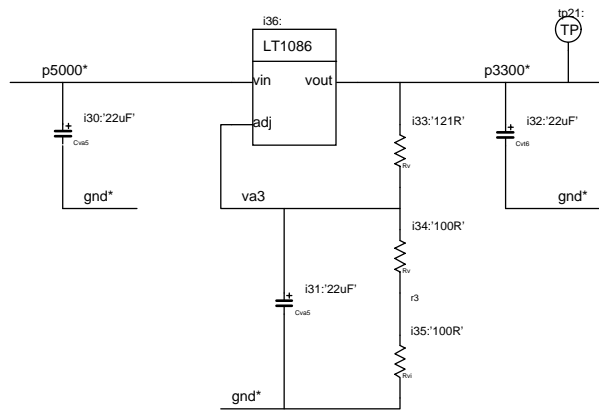
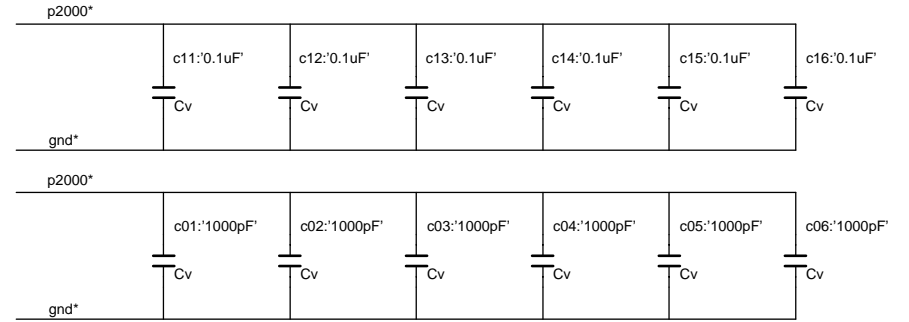
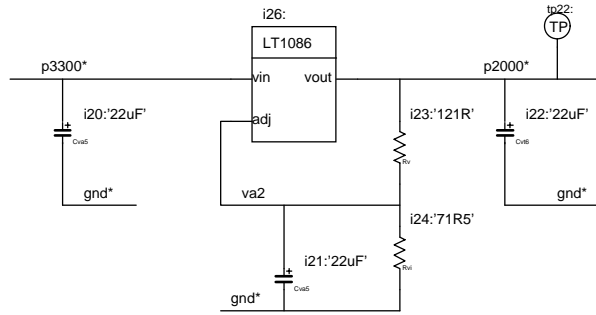
The serial eeprom is not populated on the DIGITAL reference design  
 it is shown here for reference only (for example a  
 uni manufacturer may use it)

Four digital, three analog recommended by Crystal  
 One for serial eeprom, four for audio (sheet 10)

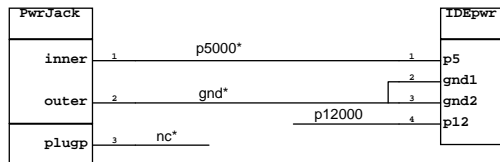
R2, R3, and R4 are setup for 100 ohm twisted pair.  
 Other values are possible. See CS8900 data sheet, page 123.

Note: Changed these caps from 10n to 1n

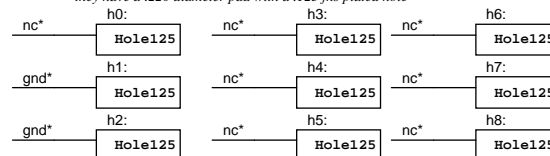




Note: Battery is 3V Li coin cell BR2032 in a smt holder

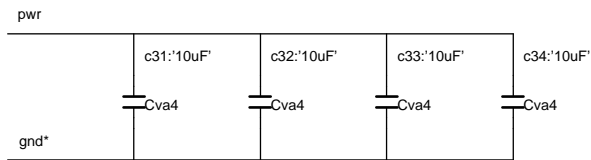
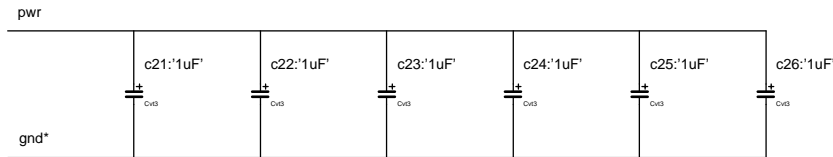
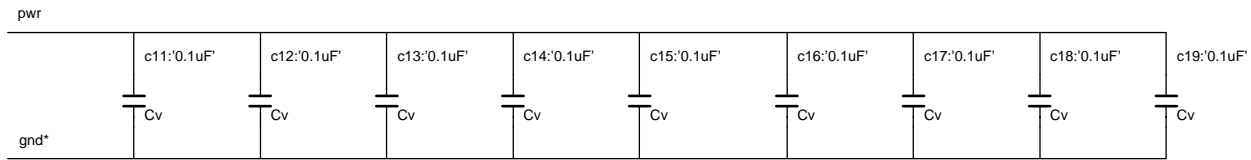


Note: These are the mounting holes, with the two near the connectors grounded they have a .220 diameter pad with a .125 fls plated hole



Title: Power	12 of 16
By: Mark Hayter	
\$Date: 1997/05/14 03:07:47 \$	
RCS \$Revision: 1.28 \$	
Version: Rev 4	

Note: Sequoia1 gets 0.1uF + 1uF for each of the five power groups plus 1uF extra  
 Note: Sequoia2 gets 0.1uF + 10uF for each of the four power groups



Note: Three 0.1uF for the IDE buffers

