

M74ALS244AP

6249827 MITSUBISHI (DGT L LOGIC)

91D 12476 D

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

T-52-07

DESCRIPTION

The M74ALS244AP is a semiconductor integrated circuit consisting of two blocks of buffer with 3-state noninverted outputs and independent output control for each block.

FEATURES

- In-phase output control inputs ($\overline{1OC}$, $\overline{2OC}$)
- High fan-out, 3-state output ($I_{OL} = 24mA$, $I_{OH} = -15mA$)
- Wide operating temperature range ($T_a = -20 \sim +75^\circ C$)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

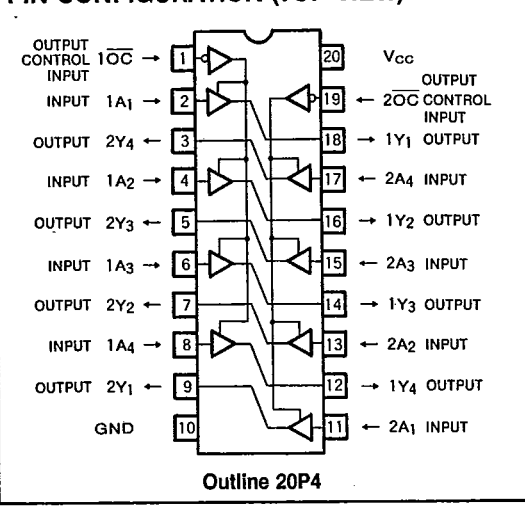
FUNCTIONAL DESCRIPTION

When output control input \overline{OC} is low-level, and if input A is low, then output Y is low. If A is high, Y is high. When \overline{OC} is high, $Y_1 \sim Y_4$ are in high-impedance state irrespective of the status of A.

The outputs of all eight buffers can be controlled simultaneously by connecting $\overline{1OC}$ and $\overline{2OC}$. The outputs can be terminated with a load resistor of not less than 133Ω .

The low-power version of M74ALS244AP, the M74ALS1244AP, is also available.

PIN CONFIGURATION (TOP VIEW)

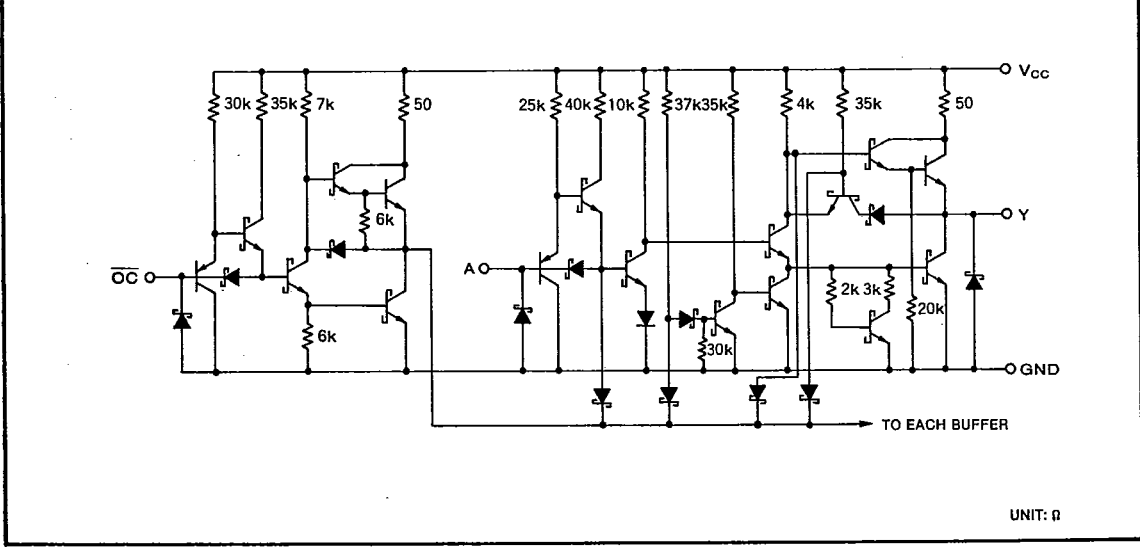


FUNCTION TABLE (Note 1)

Inputs		Output
A	\overline{OC}	Y
L	L	L
H	L	H
X	H	Z

Note 1: Z : High-impedance state
X : Irrelevant

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT: μ

MITSUBISHI ALSTTLs
M74ALS244AP

6249827 MITSUBISHI (DGLT LOGIC)

91D 12477 DT-52-07

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7	V
V_I	Input voltage		-0.5~+7	V
V_O	Output voltage	High-level state or high impedance state	-0.5~+5.5	V
T_{opr}	Operating free-air ambient temperature range		-20~+75	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65~+150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		-15	mA
I_{OL}	Low-level output current	0		24	mA
T_{opr}	Operating free-air ambient temperature range	-20		+75	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IC}	Input clamp voltage	$V_{CC}=4.5\text{V}, I_{IC}=-18\text{mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC}=4.5\sim 5.5\text{V}, I_{OH}=-0.4\text{mA}$	$V_{CC}-2$			V
		$V_{CC}=4.5\text{V}$				
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}$				V
			$I_{OH}=-3\text{mA}$	2.4	3.2	
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}$				V
			$I_{OH}=-15\text{mA}$	2.0		
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}$				V
			$I_{OL}=12\text{mA}$		0.25	
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}$				V
			$I_{OL}=24\text{mA}$		0.35	
I_{OZH}	Off-state high-level output current	$V_{CC}=5.5\text{V}, V_O=2.7\text{V}$			20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.5\text{V}, V_O=0.4\text{V}$			-20	μA
I_I	Input current at maximum voltage	$V_{CC}=5.5\text{V}, V_I=7\text{V}$			0.1	mA
I_{IH}	High-level input current	$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$			20	μA
I_{IL}	Low-level input current	$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$			-0.1	mA
I_O	Output current	$V_{CC}=5.5\text{V}, V_O=2.25\text{V}$	-30		-112	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.5\text{V}$		9	15	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.5\text{V}$		15	24	mA
I_{CCZ}	Supply current, all outputs disabled	$V_{CC}=5.5\text{V}$		17	27	mA

* : All typical values are at $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$.

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M74ALS244AP

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91D 12478 DT-52-07

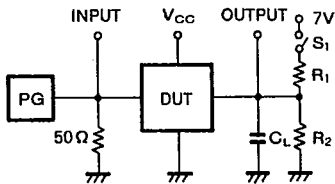
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test conditions/Limits (Note 2)									Unit		
		Input	Output	V _{CC} =5V C _L =15pF R ₁ =R ₂ =500Ω T _a =25°C			V _{CC} =4.5~5.5V C _L =50pF R ₁ =R ₂ =500Ω T _a =0~70°C			T _a =-20~+75°C			
				Typ	Min	Typ *	Max	Min	Typ *	Max			
t _{PLH}	Propagation time	A	Y	5	3	6.5	10	3	6.5	11	ns		
t _{PHL}				5	3	7	10	3	7	11			
t _{PZH}	Output enable time	$\overline{\text{OC}}$	Y	9.5	7	11	20	7	11	21	ns		
t _{PZL}				9.5	7	12	20	7	12	21			
t _{PHZ}	Output disable time	$\overline{\text{OC}}$	Y	3	2	6.5	10	2	6.5	11	ns		
t _{PLZ}				7	3	8	13	3	8	14			

* : All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: Measurement circuit



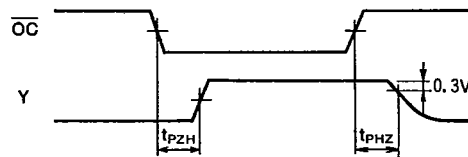
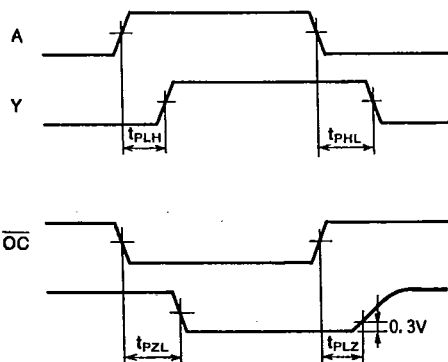
(1) The pulse generator (PG) has the following characteristics:

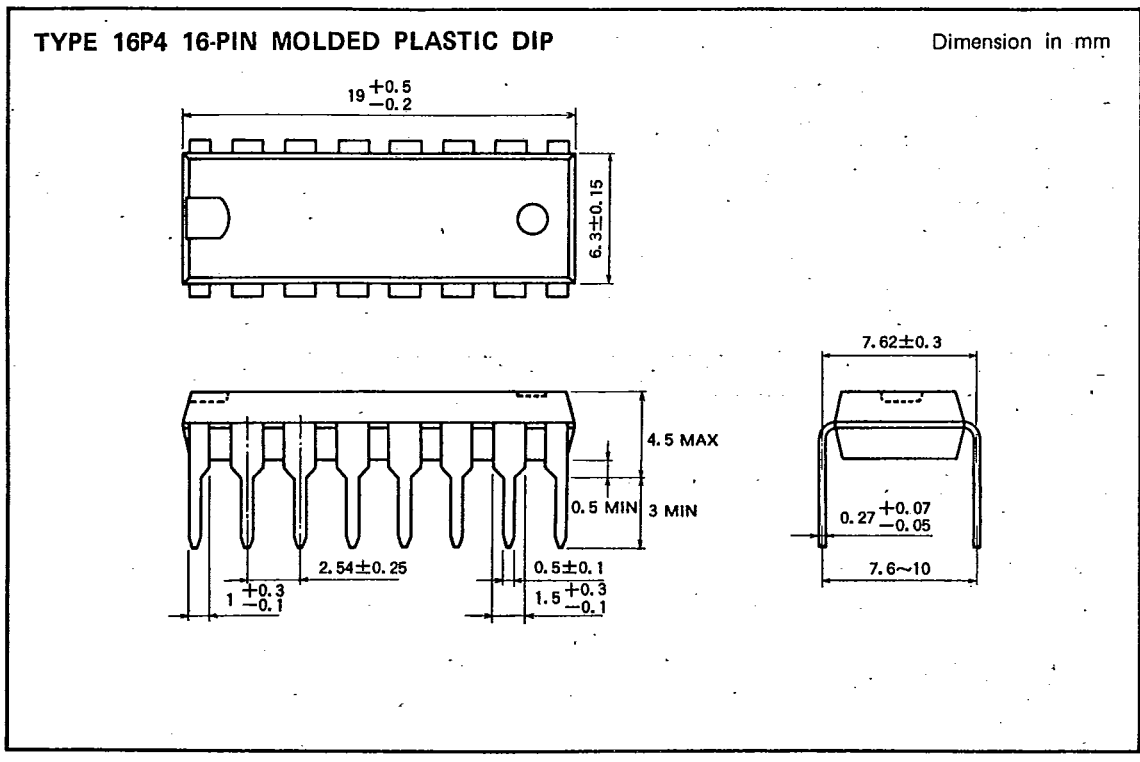
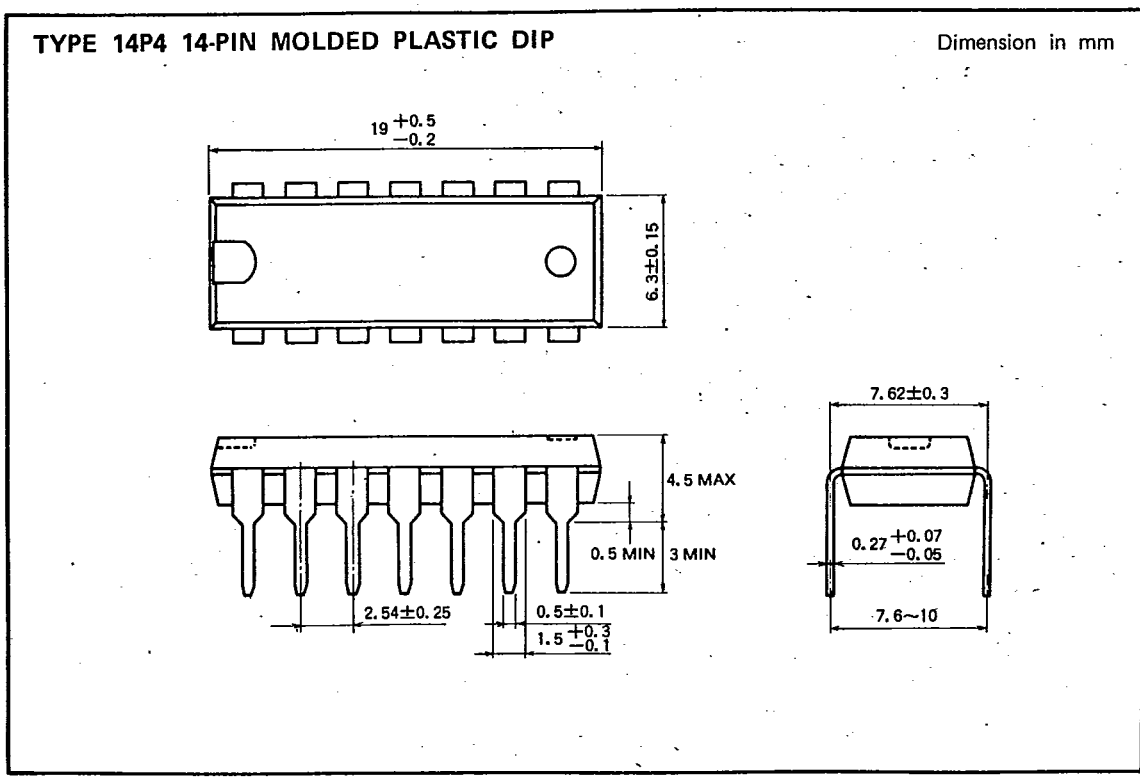
- PRR ≤ 1MHz
- t_r = 2ns, t_f = 2ns
- V_{IH} = 3.5V, V_{IL} = 0.3V
- duty cycle = 50%
- Z_o = 50Ω

Parameter	S ₁
t _{PLH}	Open
t _{PHL}	Open
t _{PZH}	Open
t _{PZL}	Closed
t _{PHZ}	Open
t _{PLZ}	Closed

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

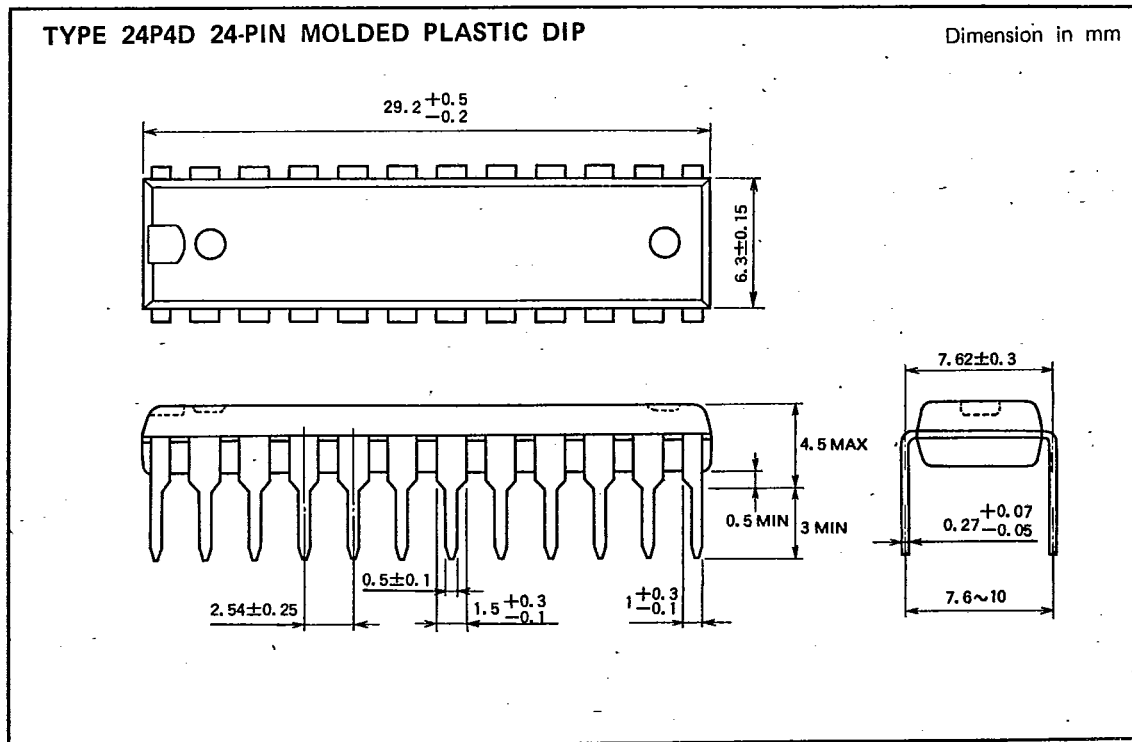
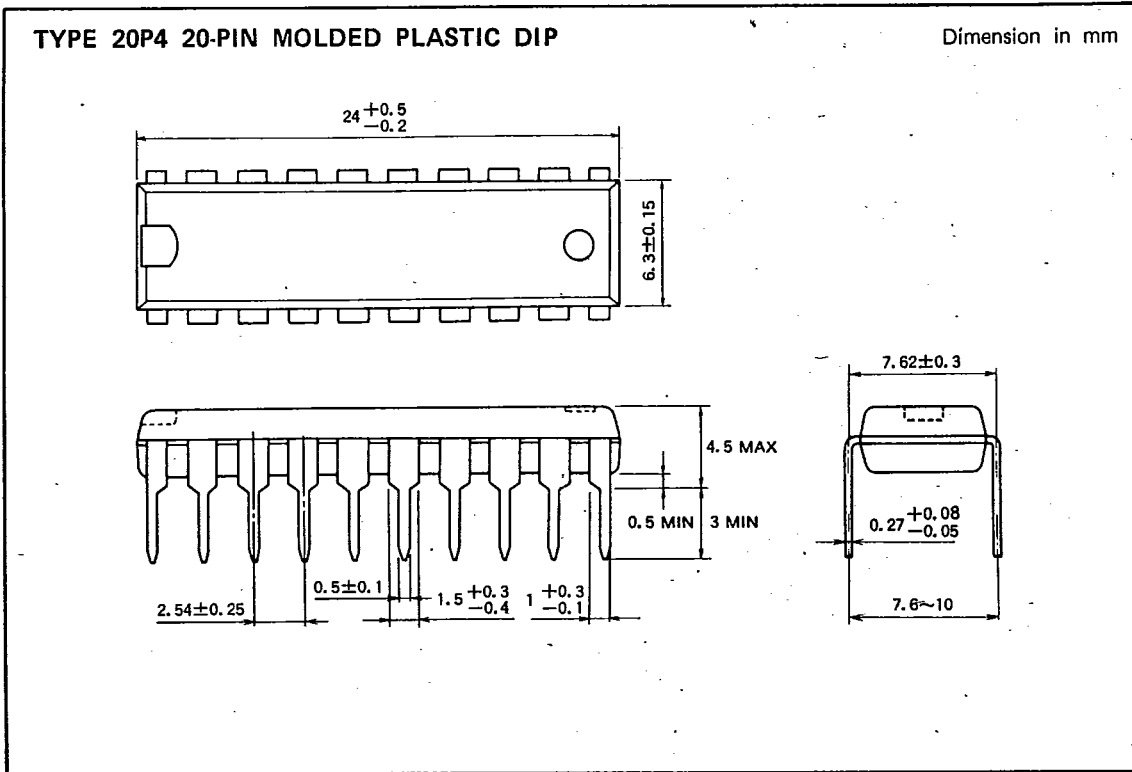




PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12324 D T-90-20



TYPE DESIGNATION TABLE

MITSUBISHI (DGTL LOGIC)

91D D ■ 6249827 0012784 7 ■ MIT3

T-90-20

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	*	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	*	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	*	Hex Inverter	14P2P
M74ALS05ADP	**	Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	*	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	**	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	*	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	*	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	**	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	**	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	**	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	*	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	**	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	**	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	*	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	**	Dual J-K Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	*	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	**	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	*	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	**	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	**	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	**	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	**	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	*	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	**	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	**	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	*	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	*	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	**	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	**	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	**	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	**	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	**	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	**	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	**	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	**	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	**	Hex Noninverting Buffer	14P2P

*: New product **: Under development

6249827 MITSUBISHI (DGTL LOGIC)

91D 12785 D

MITSUBISHI ALSTTLs

DESCRIPTION

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012785 9 ■ MIT3

T-90-20

DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

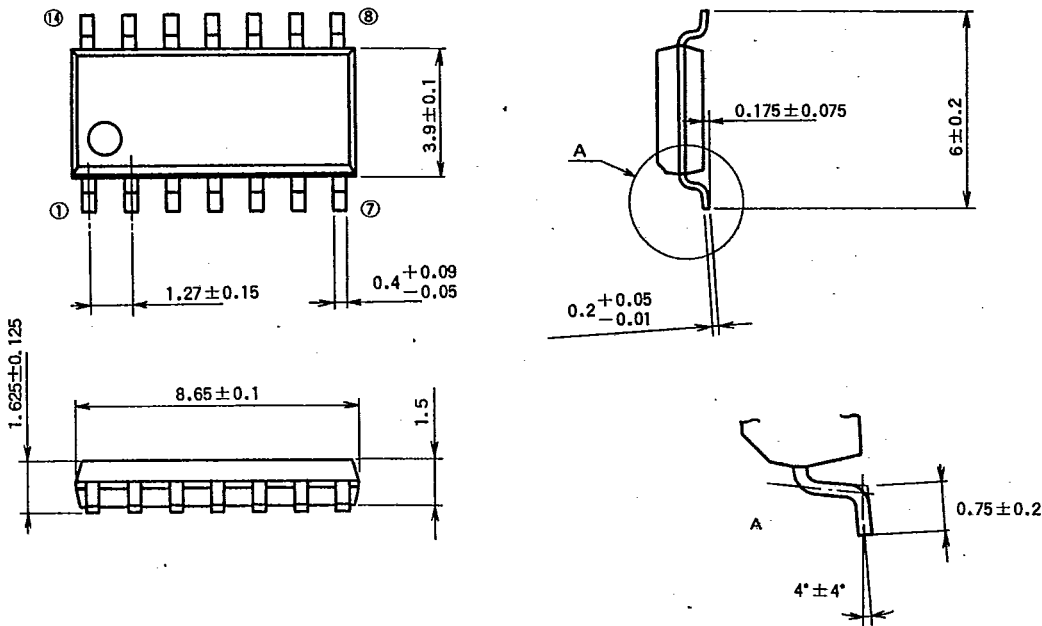
MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012786 0 ■ MIT3

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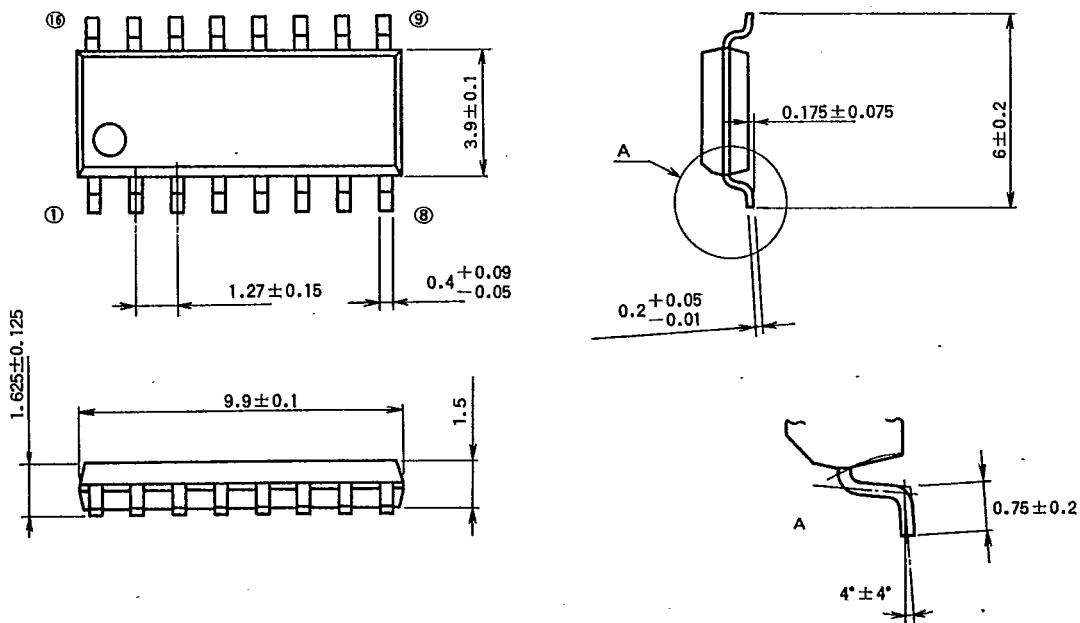
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC)

9LD D ■ 6249827 0012787 2 ■ MIT3

T-90-20

