TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT161P, TC74ACT161F, TC74ACT161FN
TC74ACT163P, TC74ACT163F, TC74ACT163FN

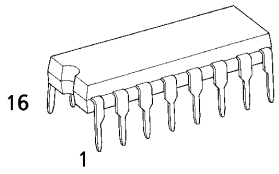
SYNCHRONOUS PRESETTABLE 4 – BIT BINARY COUNTER

TC74ACT161P/F/FN ASYNCHRONOUS CLEAR
TC74ACT163P/F/FN SYNCHRONOUS CLEAR

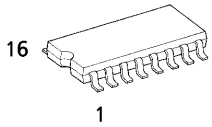
(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74ACT161 and T163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERs fabricated with silicon gate and double - layer metal wiring C2MOS technology.
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active on low logic level.
Presetting of these IC's is synchronous to the rising edge of CK.
The clear function of the TC74ACT163 is synchronous to CK, while the TC74ACT161 are cleared asynchronously.
Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n - bit counters without using external gates.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

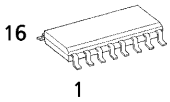
FEATURES :
- High Speed ····· f_{MAX} = 110MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.) V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.) Capability of driving 50Ω tansmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F161 / 163



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

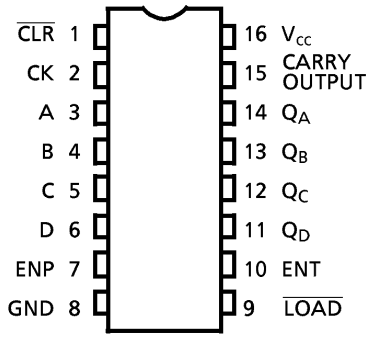


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

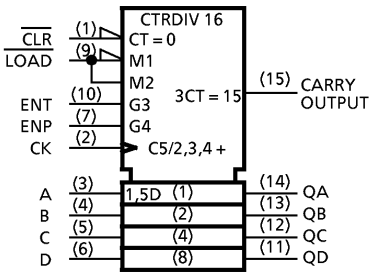
PIN ASSIGNMENT



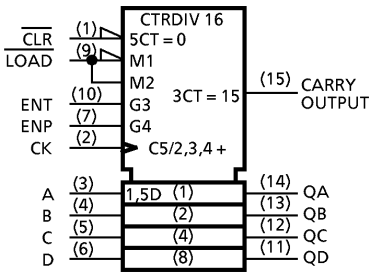
(TOP VIEW)

IEC LOGIC SYMBOL

TC74ACT161



TC74ACT163

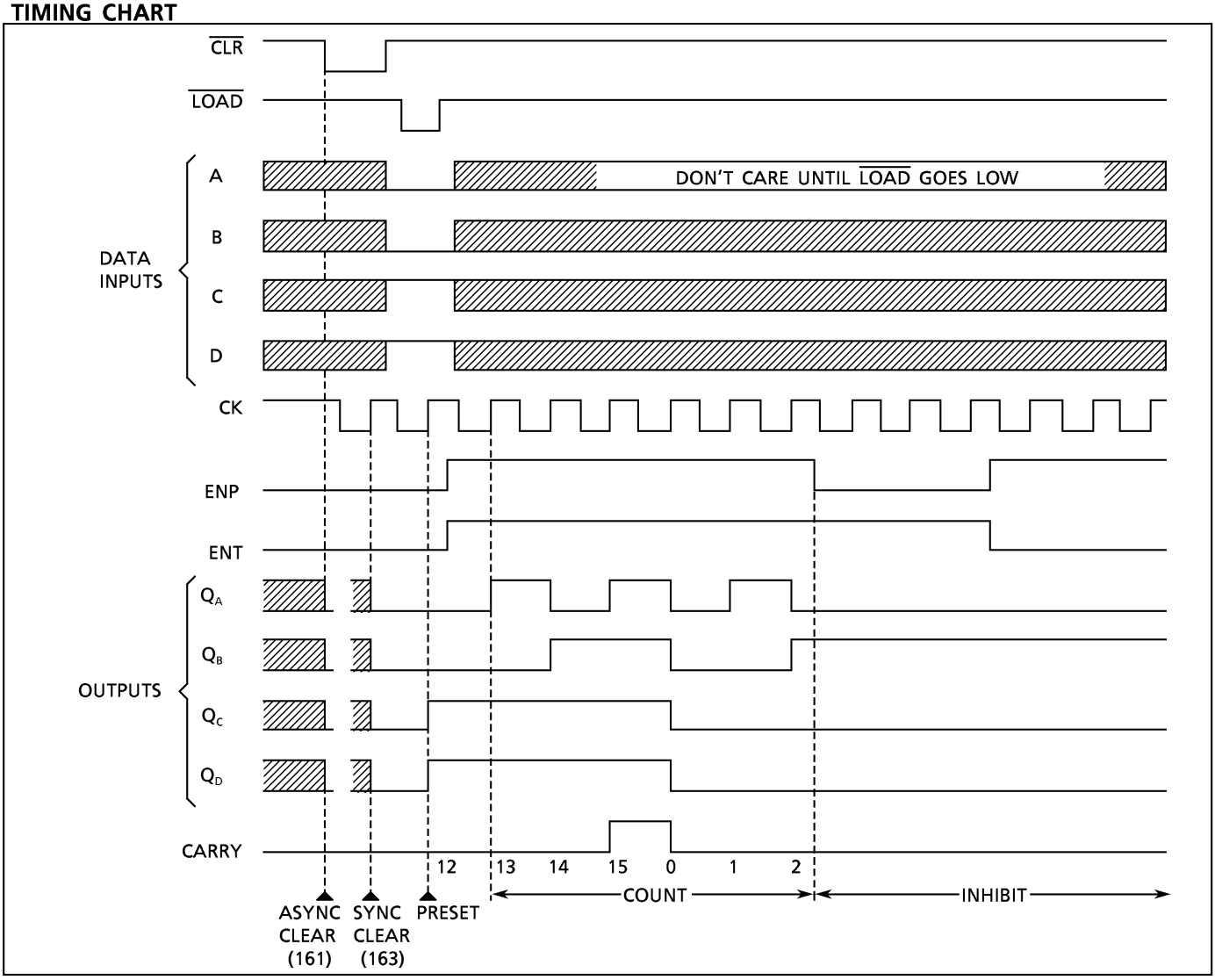


TRUTH TABLE

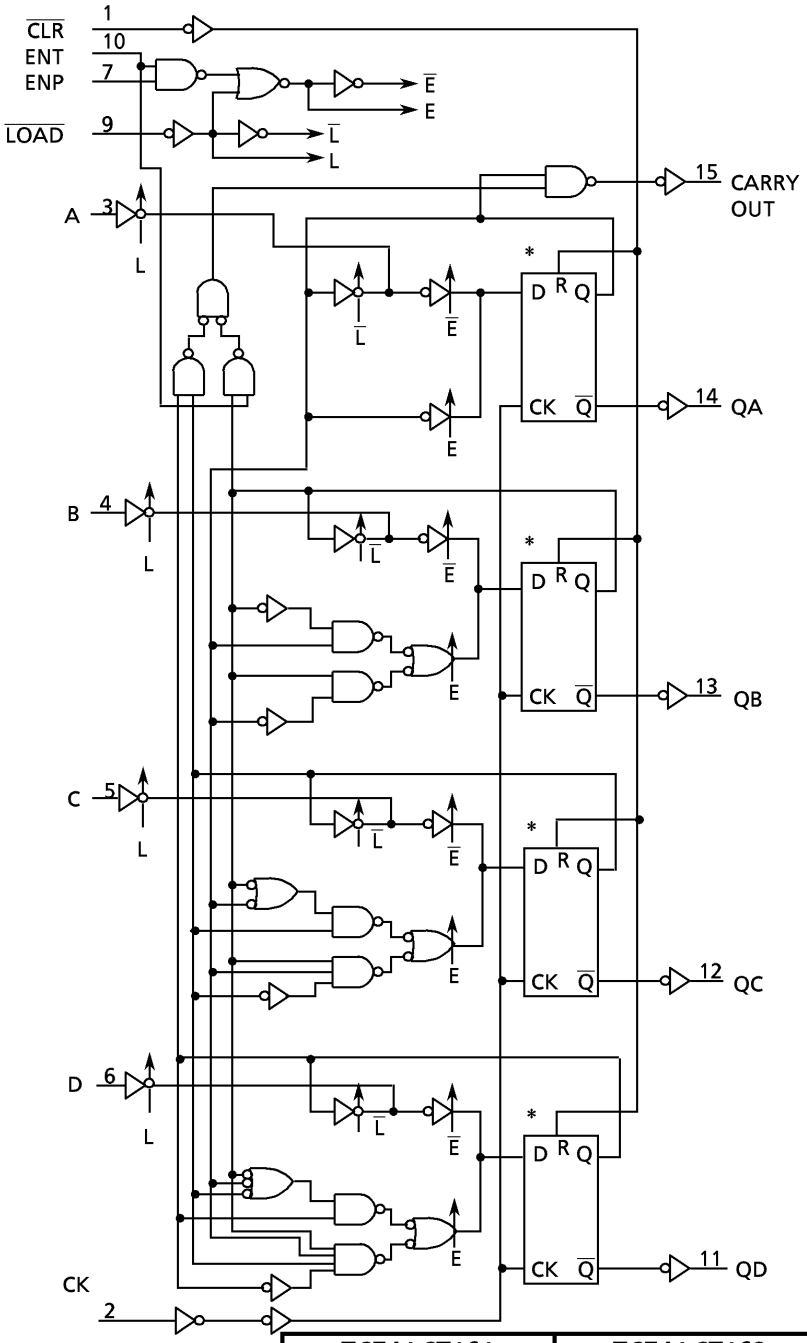
INPUTS							OUTPUTS				FUNCTION
$\overline{CLR}$ (161)	$\overline{CLR}$ (163)	$\overline{LOAD}$	ENP	ENT	CK (161)	CK (163)	QA	QB	QC	QD	
L	L	X	X	X	X	↑	L	L	L	L	RESET TO "0"
H	H	L	X	X	↑	↑	A	B	C	D	PRESET DATA
H	H	H	X	L	↑	↑	NO CHANGE				NO COUNT
H	H	H	L	X	↑	↑	NO CHANGE				NO COUNT
H	H	H	H	H	↑	↑	COUNT UP				COUNT
H	X	X	X	X	↓	↓	NO CHANGE				NO COUNT

Note X : Don't Care
A, B, C, D : Logic Level of Data Inputs
Carry : CARRY = ENT·QA · QB · QC · QD

TIMING CHART



SYSTEM DIAGRAM



* TRUTH TABLE OF INTERNAL F/F

TC74ACT161					TC74ACT163				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↑	H	L	H
L	↑	L	L	H	L	↑	L	L	H
H	↑	L	H	L	X	↑	L	H	L
X	↓	L	NO CHANGE		X	↓	L	NO CHANGE	

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±125	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	μA
	I_C	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = −40~85°C	UNIT
			V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	Fig .1	5.0 ± 0.5	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$)*	$t_{W(L)}$	Fig .4	5.0 ± 0.5	5.0	5.0	
Minimum Pulse Width ($\overline{LOAD}$, ENP, ENT)	t_s	Fig .2, 3	5.0 ± 0.5	6.0	6.0	
Minimum Set - up Time (A, B, C, D)	t_s	Fig .2	5.0 ± 0.5	4.0	4.0	
Minimum Set - up Time ($\overline{CLR}$)**	t_s	Fig .5	5.0 ± 0.5	3.0	3.0	
Minimum Hold Time ($\overline{LOAD}$, ENP, ENT)	t_h	Fig .2, 3	5.0 ± 0.5	1.0	1.0	
Minimum Hold Time (A, B, C, D)	t_h	Fig .2	5.0 ± 0.5	2.0	2.0	
Minimum Hold Time ($\overline{CLR}$)**	t_h	Fig .5	5.0 ± 0.5	2.0	2.0	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}	Fig .4	5.0 ± 0.5	1.0	1.0	

* for TC74ACT161 only
** for TC74ACT163 only

AC ELECTRICAL CHARACTERISTICS (CL = 50pF, RL = 500 Ω, Input tr = tf = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}	Fig.1	5.0 ± 0.5	−	7.2	10.5	1.0	12.0	ns
Propagation Delay Time (CK−CARRY, Count Mode)	t_{pLH} t_{pHL}	Fig.1	5.0 ± 0.5	−	8.5	13.0	1.0	15.0	
Propagation Delay Time (CK−CARRY, Preset Mode)	t_{pLH} t_{pHL}	Fig.2	5.0 ± 0.5	−	9.7	15.0	1.0	17.0	
Propagation Delay Time (ENT−CARRY)	t_{pLH} t_{pHL}	Fig.6	5.0 ± 0.5	−	6.6	10.0	1.0	11.5	
Propagation Delay Time ($\overline{CLR}$−Q)*	t_{pHL}	Fig.4	5.0 ± 0.5	−	6.3	10.0	1.0	11.5	
Propagation Delay Time ($\overline{CLR}$−CARRY)*	t_{pHL}	Fig.4	5.0 ± 0.5	−	7.7	12.3	1.0	14.0	
Maximum Clock Frequency	f_{MAX}		5.0 ± 0.5	70	100	−	60	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	46	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:

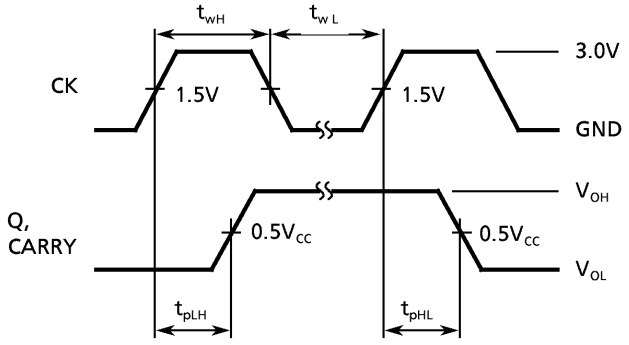
$$\triangle I_{cc} = f_{CK} \bullet V_{cc} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

C_{QA}~C_{QD} and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.
f_{CK} is the input frequency of the CK.

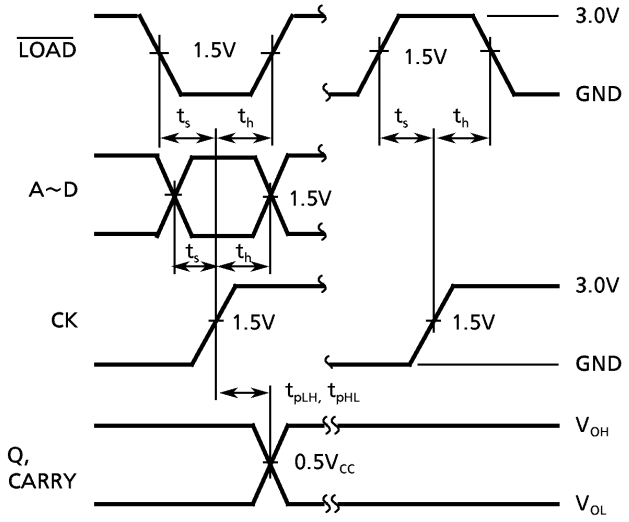
(2) * for TC74ACT161 only

SWITCHING CHARACTERISTICS TEST WAVEFORM

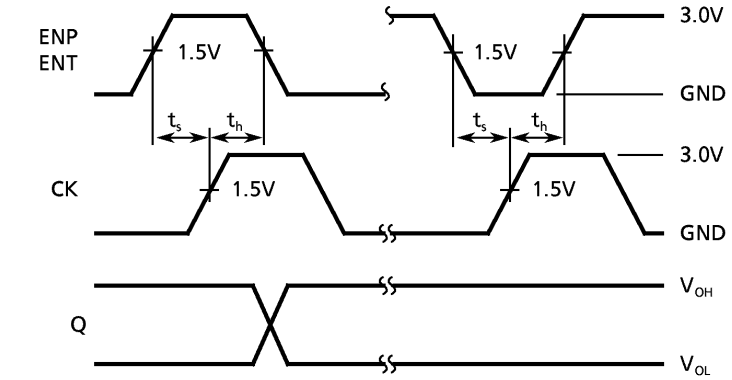
COUNT MODE (Fig. 1)



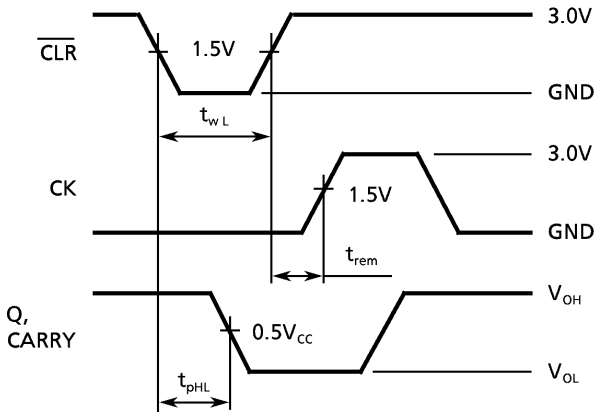
PRESET MODE (Fig. 2)



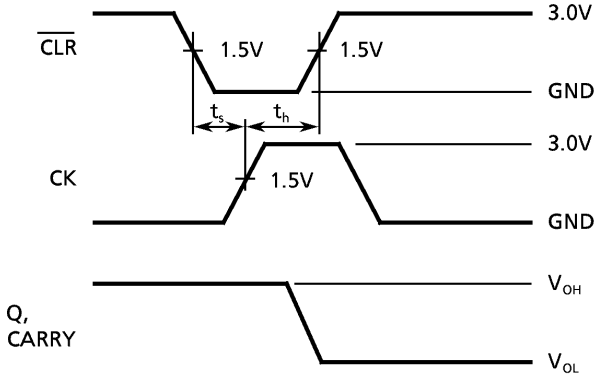
COUNT ENABLE MODE (Fig. 3)



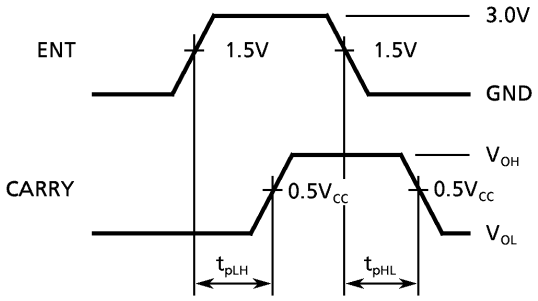
CLEAR MODE (TC74ACT161) (Fig. 4)



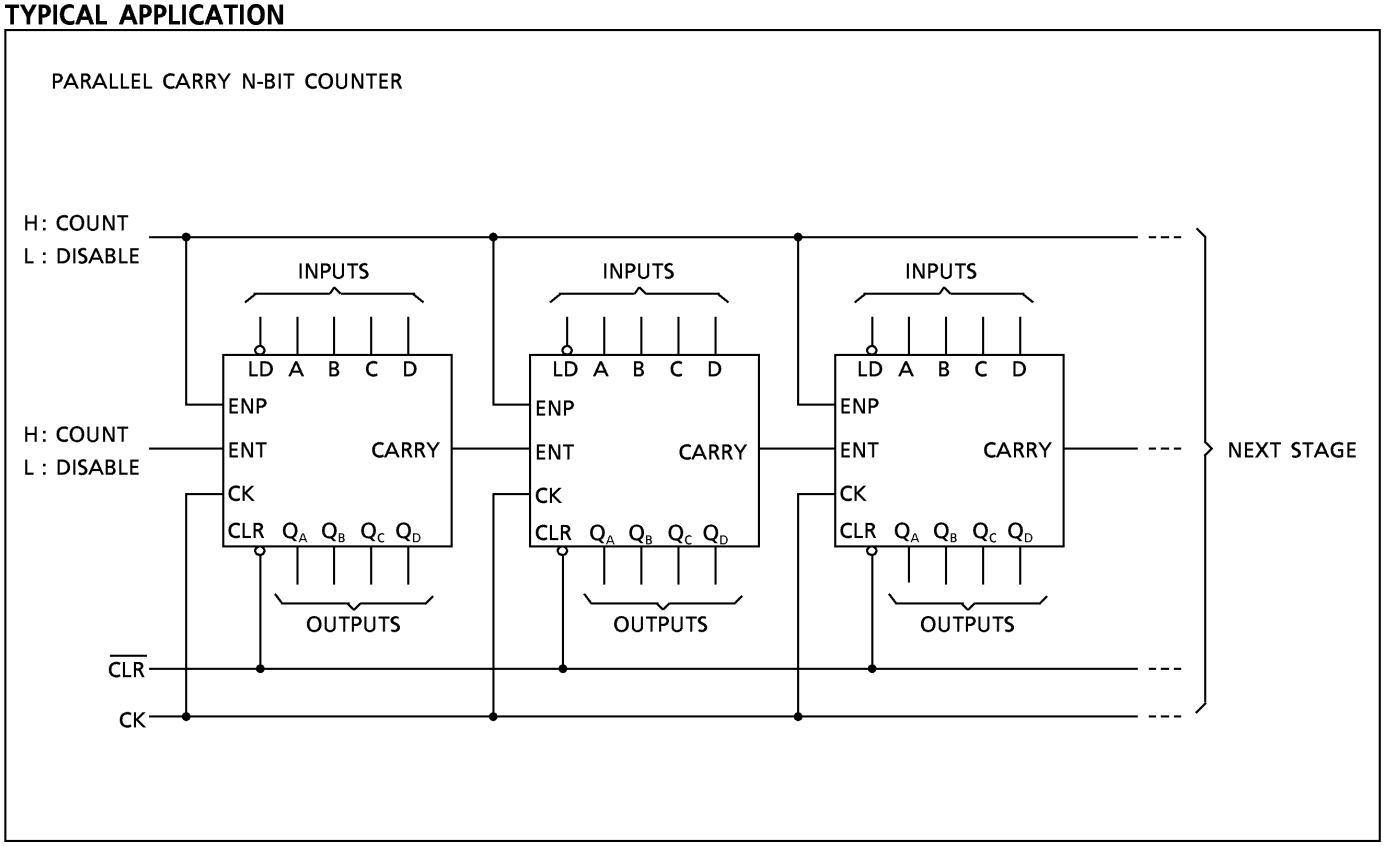
CLEAR MODE (TC74ACT163) (Fig. 5)



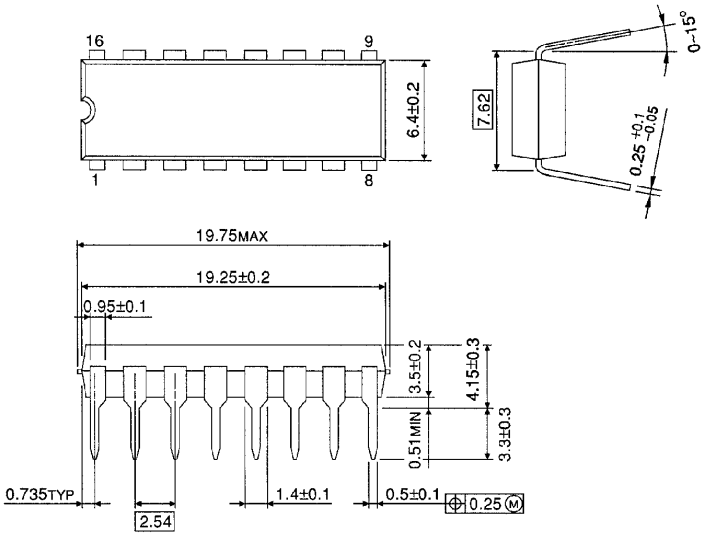
CASCADE MODE (Fix Maximum Count) (Fig. 6)



TYPICAL APPLICATION

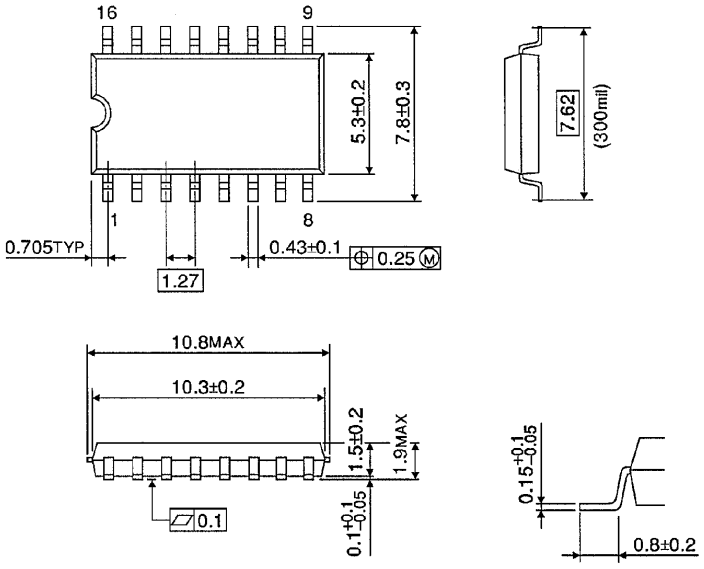


DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

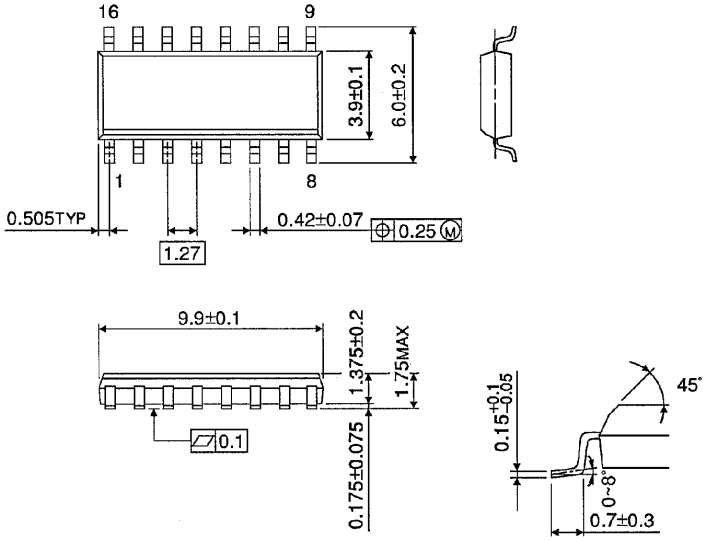
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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