Datasheet

DS000609

CMV8000

8MP CMOS Machine Vision Image Sensor

v1-00 • 2019-Jun-12

Content Guide

1 General Description

The CMV8000 is a high-speed CMOS image sensor developed for machine vision and traffic applications, with 3360 by 2496 active pixels. The image array consists of 5.5 µm by 5.5 µm pipelined global shutter pixels, which allow exposure during read-out, while performing CDS operation. The image data is read out serially through 16 LVDS channels, with 10-bit or 12-bit resolution. The sensor also integrates a programmable gain amplifier and offset regulation. Each LVDS output channel runs at 600 Mbps maximum, which results in a frame rate of 103 FPS at full image resolution with 10-bit color. Higher frame rates are possible when reading out a smaller region of interest or when subsampling is enabled. These modes are all programmable using the SPI interface. A programmable on-board sequencer generates all internal exposure and read-out timings. External triggering and exposure programming is possible. Optical dynamic range can be increased by several on-chip high dynamic range (HDR) modes.

1.1 Key Benefits & Features

The benefits and features of CMV8000, 8MP CMOS Machine Vision Image Sensor, are listed below:

Figure 1:
Added Value of Using CMV8000

Benefits	Features
Designed for high performance applications	Resolution of 3360 by 2496 at 103 frames per second
Capture fast moving objects	8T global shutter pixel with true correlated double sampling
Easy to operate	On-chip digital sequencer which handles all the sensor controls, over SPI
High inspection rate	High bit rate

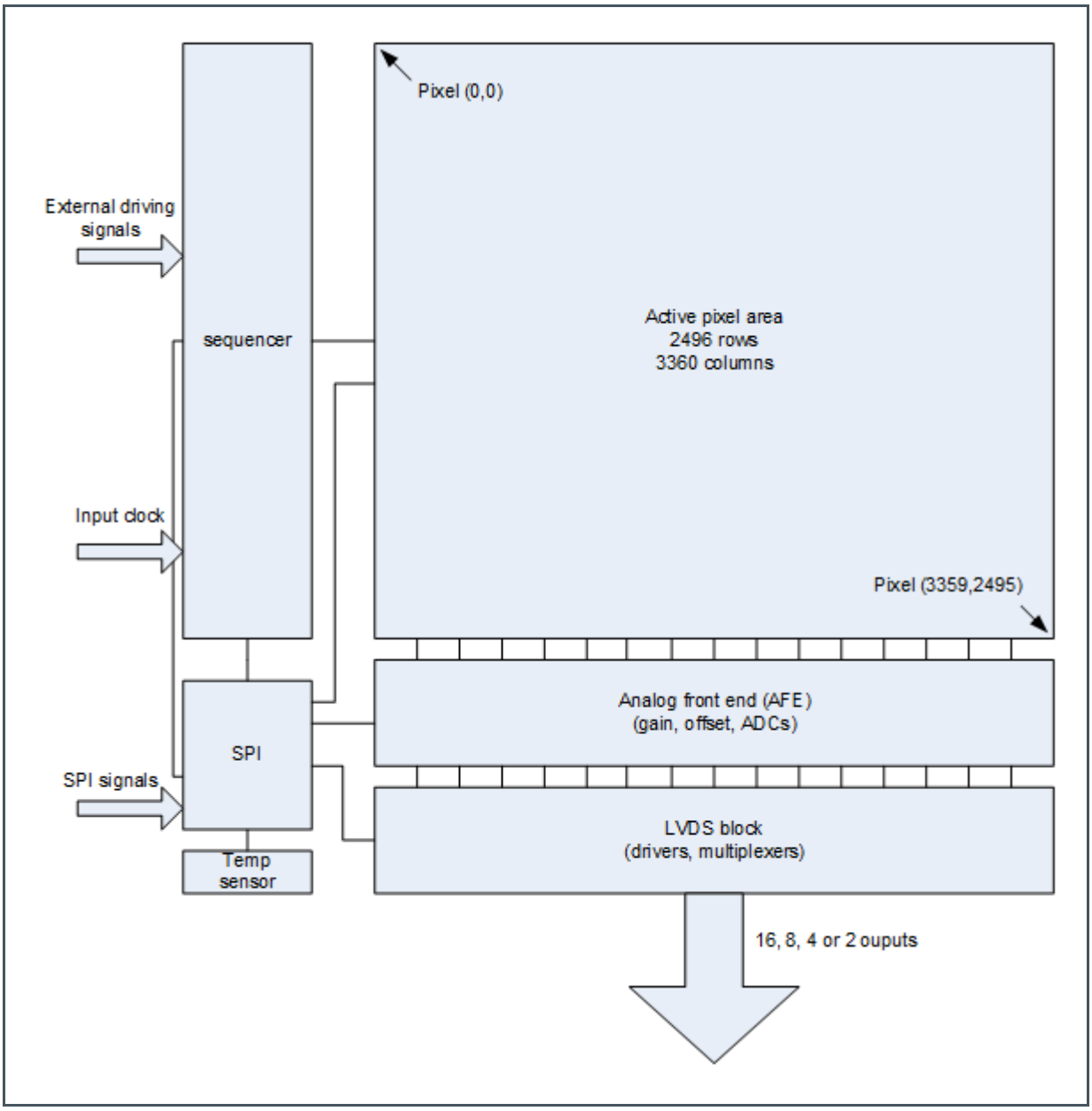
1.2 Applications

- Machine vision
- Motion capture
- Intelligent traffic systems
- Video and broadcast
- Medical
- Scientific

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of CMV8000



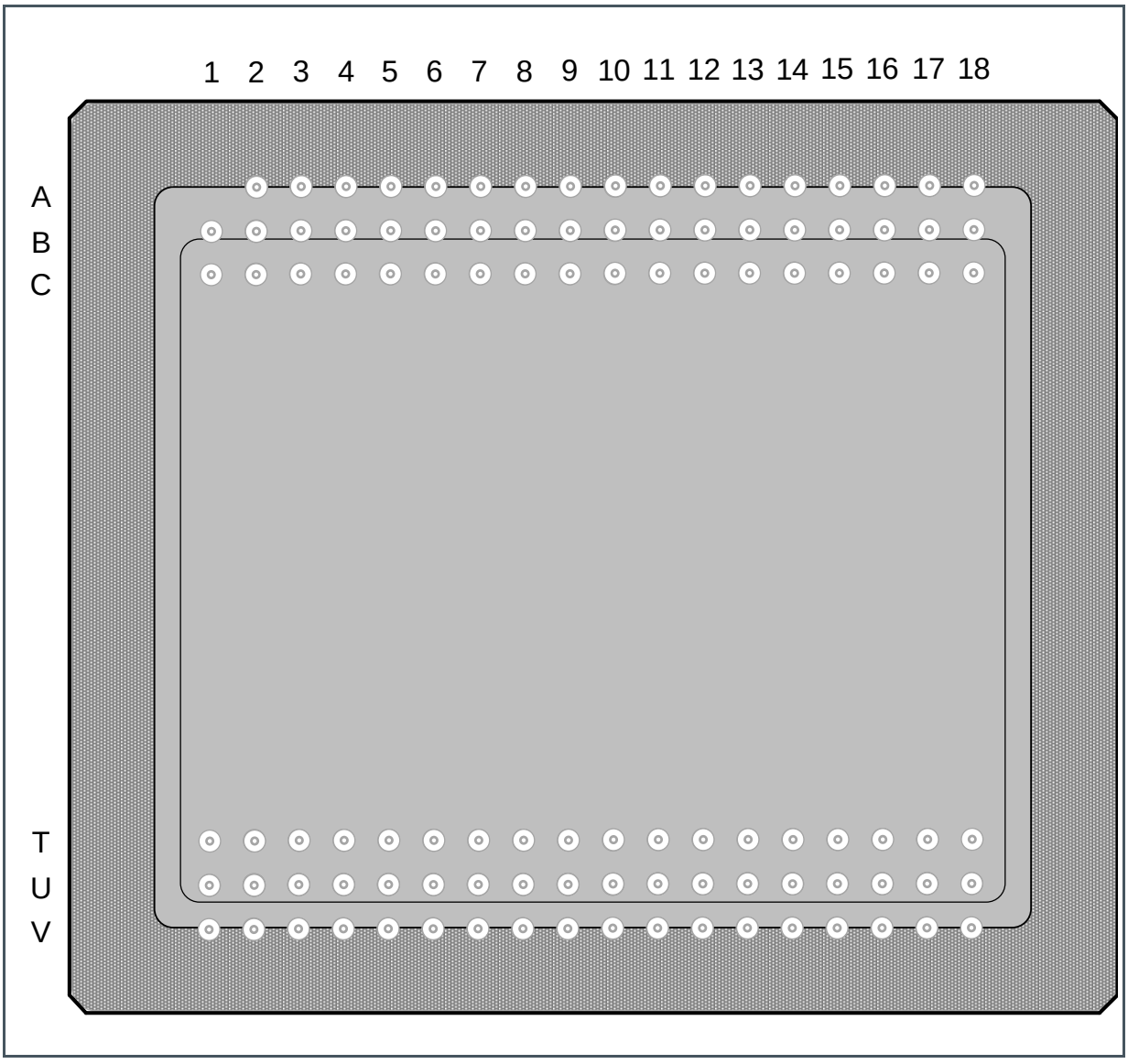
2 Ordering Information

Ordering Code	Package	Chroma	Options	Delivery Quantity
CMV8000ES-1E5M1PA	µPGA	Mono		24 pcs / tray
CMV8000ES-1E5C1PA	µPGA	Color		24 pcs / tray

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Assignment PGA (top view)



3.2 Pin Description

Figure 4:
Pin Description of CMV8000

Pin Number	Pin Name	Pin Type[1]	Description
A17	DNC	\	Do not connect!
B9	T_ANA	Analog output	Analog test mux output
A8	CMDN	Bias	Analog reference
A2	CMDN_COL_LOAD	Bias	Analog reference
B14	CMDN_COL_LOAD	Bias	Analog reference
A13	CMDN_COL_AMPL	Bias	Analog reference
A14	CMDN_COL_PC	Bias	Analog reference
B12	VTF_LOW1	Bias	Analog reference
A12	VTF_LOW2	Bias	Analog reference
B13	VTF_LOW3	Bias	Analog reference
A16	VBGAP	Bias	Analog reference
A9	VPC_L	Bias	Analog reference
B8	VPC_H	Bias	Analog reference
C16	VPC_COMP	Bias	Analog reference
B16	VREF	Bias	Analog reference
B17	VRAMP_SIG	Bias	Analog reference
C17	VRAMP_RES	Bias	Analog reference
B10	VRST_L	Bias	Analog reference
A7	CMDP	Bias	Analog reference
C15	CMDP_COMP	Bias	Analog reference
B7	CMDP_INV	Bias	Analog reference
B15	CMDP_RAMP	Bias	Analog reference
A15	CMDN_LVDS	Bias	Analog reference
C6	SYS_RESN	DI	Global sensor reset
V2	GND	Digital ground	Digital ground
A3	F_REQ	DI	Frame request
C4	INT2	DI	External integration control
B3	INT1	DI	External integration control
B5	SPI_ENABLE	DI	SPI enable signal
B4	SPI_CLK	DI	SPI clock signal
A4	SPI_IN	DI	SPI input data

Pin Number	Pin Name	Pin Type[1]	Description
A5	SPI_OUT	DO	SPI output data
B2	TDIG1	DI	Digital test pin 1
C3	TDIG2	DO	Digital test pin 2
T1	IN_LCLK_P	LVDS input	Clock input channel
U1	IN_LCLK_N	LVDS input	Clock input channel
T17	OUT_CLK_P	LVDS output	Clock output channel
U17	OUT_CLK_N	LVDS output	Clock output channel
U2	OUT_CTR_P	LVDS output	Control output channel
T2	OUT_CTR_N	LVDS output	Control output channel
U3	OUT1_P	LVDS output	Channel 1 output
T3	OUT1_N	LVDS output	Channel 1 output
T5	OUT3_P	LVDS output	Channel 3 output
T4	OUT3_N	LVDS output	Channel 3 output
V4	OUT5_P	LVDS output	Channel 5 output
U4	OUT5_N	LVDS output	Channel 5 output
V5	OUT7_P	LVDS output	Channel 7 output
U5	OUT7_N	LVDS output	Channel 7 output
T8	OUT9_P	LVDS output	Channel 9 output
T7	OUT9_N	LVDS output	Channel 9 output
V7	OUT11_P	LVDS output	Channel 11 output
U7	OUT11_N	LVDS output	Channel 11 output
V8	OUT13_P	LVDS output	Channel 13 output
U8	OUT13_N	LVDS output	Channel 13 output
V9	OUT15_P	LVDS output	Channel 15 output
U9	OUT15_N	LVDS output	Channel 15 output
V10	OUT17_P	LVDS output	Channel 17 output
U10	OUT17_N	LVDS output	Channel 17 output
T10	OUT19_P	LVDS output	Channel 19 output
T9	OUT19_N	LVDS output	Channel 19 output
T13	OUT21_P	LVDS output	Channel 21 output
T12	OUT21_N	LVDS output	Channel 21 output
V12	OUT23_P	LVDS output	Channel 23 output
U12	OUT23_N	LVDS output	Channel 23 output
V13	OUT25_P	LVDS output	Channel 25 output
U13	OUT25_N	LVDS output	Channel 25 output

Pin Number	Pin Name	Pin Type[1]	Description
V14	OUT27_P	LVDS output	Channel 27 output
U14	OUT27_N	LVDS output	Channel 27 output
V15	OUT29_P	LVDS output	Channel 29 output
U15	OUT29_N	LVDS output	Channel 29 output
T15	OUT31_P	LVDS output	Channel 31 output
T14	OUT31_N	LVDS output	Channel 31 output
T18	VDD18	Digital supply	Supply for ADC counters and logic
U6	VDD18	Digital supply	Supply for ADC counters and logic
U11	VDD18	Digital supply	Supply for ADC counters and logic
U16	VDD18	Digital supply	Supply for ADC counters and logic
V1	VDD18	Digital supply	Supply for ADC counters and logic
V17	VDD18	Digital supply	Supply for ADC counters and logic
B1	VDD18	Digital supply	Supply for ADC counters and logic
C1	VSS18	Digital ground	Digital ground
V18	VSS18	Digital ground	Digital ground
T6	VSS18	Digital ground	Digital ground
T11	VSS18	Digital ground	Digital ground
T16	VSS18	Digital ground	Digital ground
U18	VSS18	Digital ground	Digital ground
V3	VSS18	Digital ground	Digital ground
V16	VSS18	Digital ground	Digital ground
B11	VDDPIX	Analog supply	Pixel array supply
C7	VDDPIX	Analog supply	Pixel array supply
C10	VDDPIX	Analog supply	Pixel array supply
A6	VDDPIX	Analog supply	Pixel array supply
C14	VDDPIX	Analog supply	Pixel array supply
A10	VRST_H	Analog supply	Pixel reset driver supply
B6	VDD33	Analog supply	Analog circuit supply
C11	VDD33	Analog supply	Analog circuit supply
C18	VDD33	Analog supply	Analog circuit supply
V11	VDD33	Analog supply	Analog circuit supply
V6	VSS33	Analog ground	Analog ground
C12	VSS33	Analog ground	Analog ground
C13	VSS33	Analog ground	Analog ground
A11	VSS33	Analog ground	Analog ground

Pin Number	Pin Name	Pin Type(1)	Description
A18	VSS33	Analog ground	Analog ground
B18	VSS33	Analog ground	Analog ground
C2	VSS33	Analog ground	Analog ground
C5	VSS33	Analog ground	Analog ground
C8	VSS33	Analog ground	Analog ground
C9	VSS33	Analog ground	Analog ground

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of CMV8000

Symbol	Parameter	Min	Max	Unit	Comments
Continuous Power Dissipation (T_A = 70 °C)					
P_T	Continuous Power Dissipation		1200	mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	Class 1C JS-001-2012
Temperature Ranges and Storage Conditions					
T_J	Operating Junction Temperature	-30	70	°C	TBC
T_{STRG}	Storage Temperature Range	20	40	°C	TBC
RH_{NC}	Relative Humidity (non-condensing)	30	60	%	Storage conditions

5 Electrical Characteristics

If not stated otherwise, all values are typical.

Figure 6:
Electrical Characteristics of CMV8000

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
VDD18	Digital blocks		1.95	1.98	2.00	V
VDD33	Analog blocks		3.2	3.3	3.4	V
VDDPIX	Pixel array power supply		2.9	3.0	3.1	V
VRST_H	Pixel reset pulse		3.2	3.3	3.4	V
IDD18	Supply current	Nominal		410		mA
IDD33	Supply current	Nominal		125		mA
IDDPIX	Supply current	Nominal Peak(1)		20 150		mA
IDDRST_H	Supply current	Nominal Peak		0.5 20		mA
P_{tot}	Total power consumption			1.2		W
Digital I/O						
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD33=3.3 V I_{OH}=2 mA	2.1			V
V_{OL}	Low level output voltage	VDD33=3.3 V I_{OH}=2 mA			0.4	V
f_{IN_LCLK}	IN_LCLK frequency		125		300	MHz
DC_{IN_LCLK}	IN_LCLK duty cycle		45	50	55	%
f_{SPI_CLK}	SPI input clock frequency				60	MHz
LVDS Driver						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OD}	Differential output voltage	Steady state, R_L = 100 Ω	247	350	757	mV
ΔV_{OD}	Difference in VOD between complementary output states	Steady state, R_L = 100 Ω			50	mV
V_{OC}	Common mode voltage	Steady state, R_L = 100 Ω	1.26	1.37	1.50	V
ΔV_{OC}	Difference in VOC between complementary output states	Steady state, R_L = 100 Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA
f	Operating frequency				240	MHz
LVDS Receiver						
V_{ID}	Differential input voltage	Steady state	100		600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$ = 1.2 V ± 50 mV 0 ≤ $V_{INP\|INN}$ ≤ 2.4 V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

(1) This is a short current peak during FOT. This peak current should be supplied by enough decoupling capacitors.

6 Typical Operating Characteristics

6.1 Electro-Optical Characteristics

Below are the typical electro-optical specifications of the CMV8000. These are typical values for the whole operating range.

Figure 7:
Electro-Optical Characteristics

Parameter	Value	Remark
Effective pixels	3360 x 2496	
Pixel pitch	5.5 µm x 5.5 µm	
Optical format	1.43 optical inch	
Pixel type	Global shutter with true CDS	Allows fixed pattern noise correction and reset (kTC) noise cancelling by true correlated double sampling
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image
Full well charge	11700 e^-	Pinned photodiode pixel
Conversion gain	0.077DN/e^-	10-bit mode, unity gain
Temporal noise	8.6 e^-	Read noise. Measured with high gain setting
Dynamic range	61 dB	
Shutter efficiency	1/20000	
DC	41.2 e^-/s	At 25 ºC die temperature. The dark current doubles every 6.5 ºC increase.
DSNU	5.6DN/s	At 25 ºC die temperature, in 10-bit mode
PRNU	< 1% RMS of signal	
Color filters	Optional	RGB Bayer pattern
QE	59%	At 568 nm with microlenses
LVDS outputs	16 data 1 control 1 clock	Each data output running at 600 Mbps. 8, 4 and 2 outputs selectable at reduced frame rate.

Parameter	Value	Remark
Frame rate	103 fps	Using a 10-bit/pixel and 600 Mbps data rate. Higher frame rate is possible in row-windowing mode.
Timing generation	On-chip	Possibility to control exposure through an external pin.
PGA	Yes	5 analog gain settings
Programmable registers	Sensor parameters	Window coordinates, timing parameters, gain & offset, exposure time, mirrored read-out in X and Y direction...
HDR mode	Interleaved Piece-wise linear response	2 exposures for odd/even columns Response curve with 2 kneepoints
ADC	10-bit / 12-bit	Column ADC
Interface	LVDS	Serial output data + synchronization signals
I/O logic levels	LVDS = 1.8 V Digital I/O = 3.3 V	
Cover glass	D263Teco	Double side AR coating, no IR cut-off filter R <2.2% abs, 400 nm – 900 nm, per surface, AOI = 15º

6.2 Spectral Characteristics

Figure 8:
Quantum Efficiency

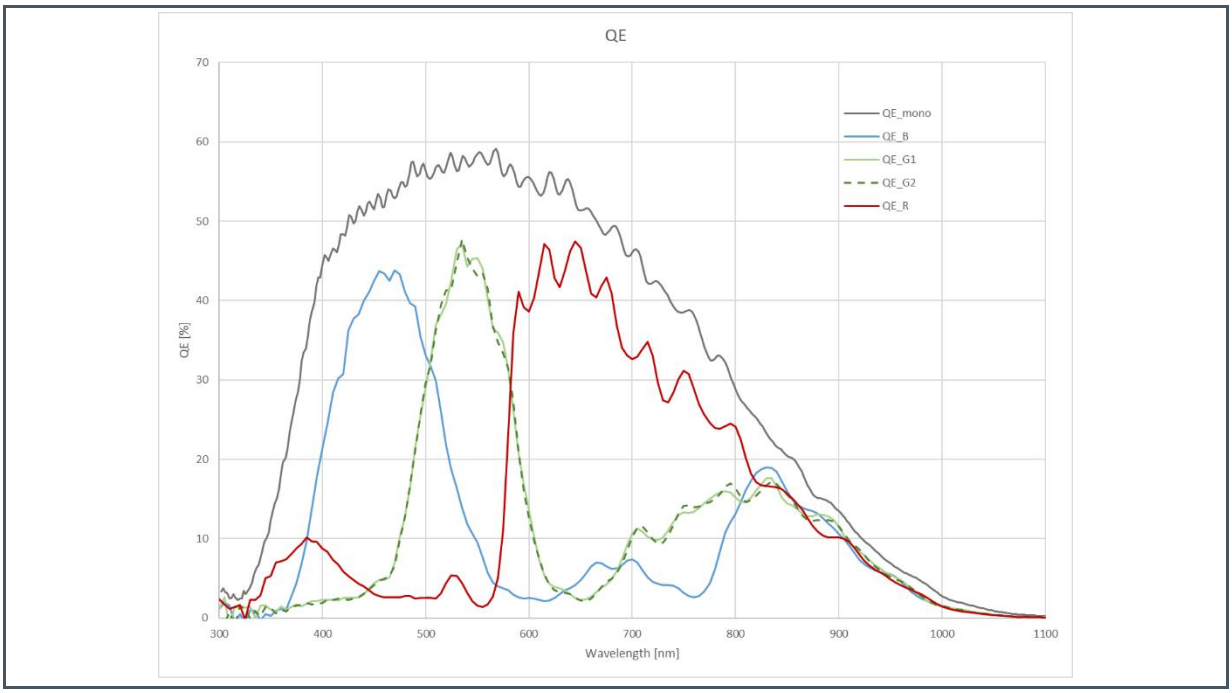


Figure 9:
Spectral Response

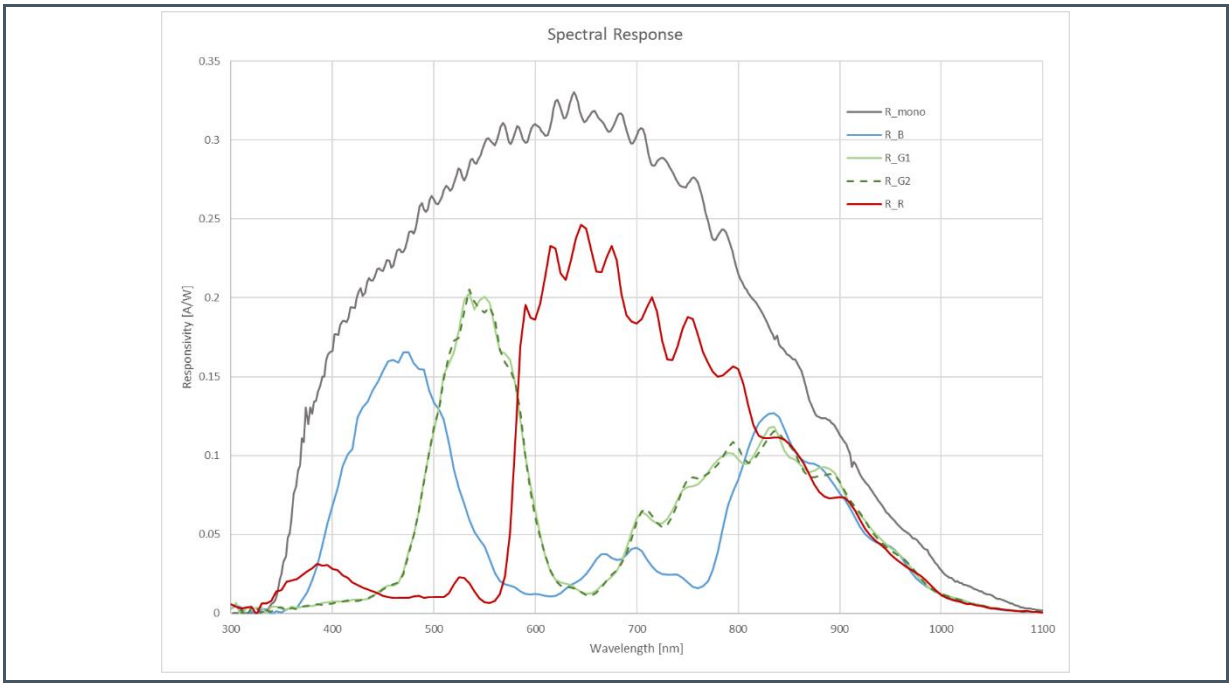
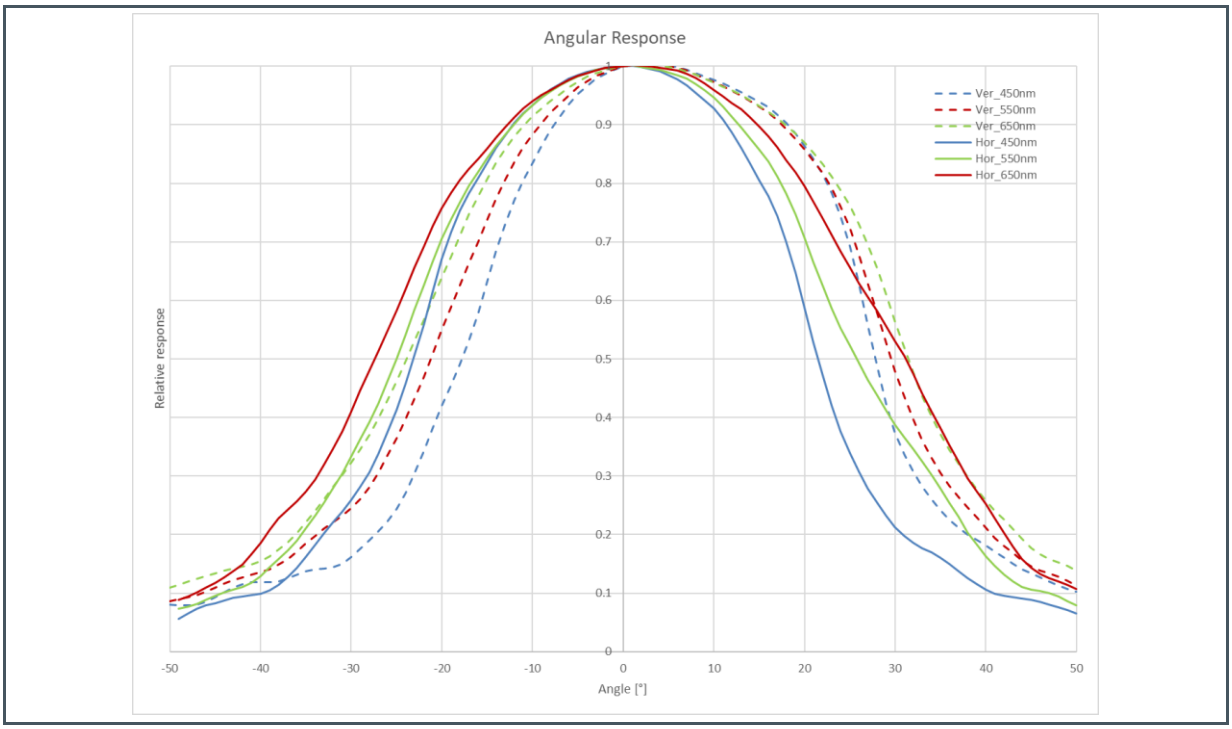


Figure 10:
Angular Response



7 Functional Description

7.1 Sensor Architecture

Figure 2 shows the architecture of the CMV8000 image sensor. The internal sequencer generates the necessary signals for image acquisition. Once the acquisition is complete, the image is stored in the pixel (global shutter) and is then read out row by row. The signal then passes through an analog front end, where gain can be applied, and an ADC block where the analog to digital conversion is done.

These digital signals then go to the LVDS output stage, to be serialized to 16 parallel output channels. In the default LVDS configuration, each output channel puts out 224 adjacent columns of the pixel array in two bursts of 112 pixels to form a row of 3584 pixels. Two additional output channels contain a double data rate clock signal to sample the pixel data, and a control channel containing the sync codes which identify when valid pixel data is available.

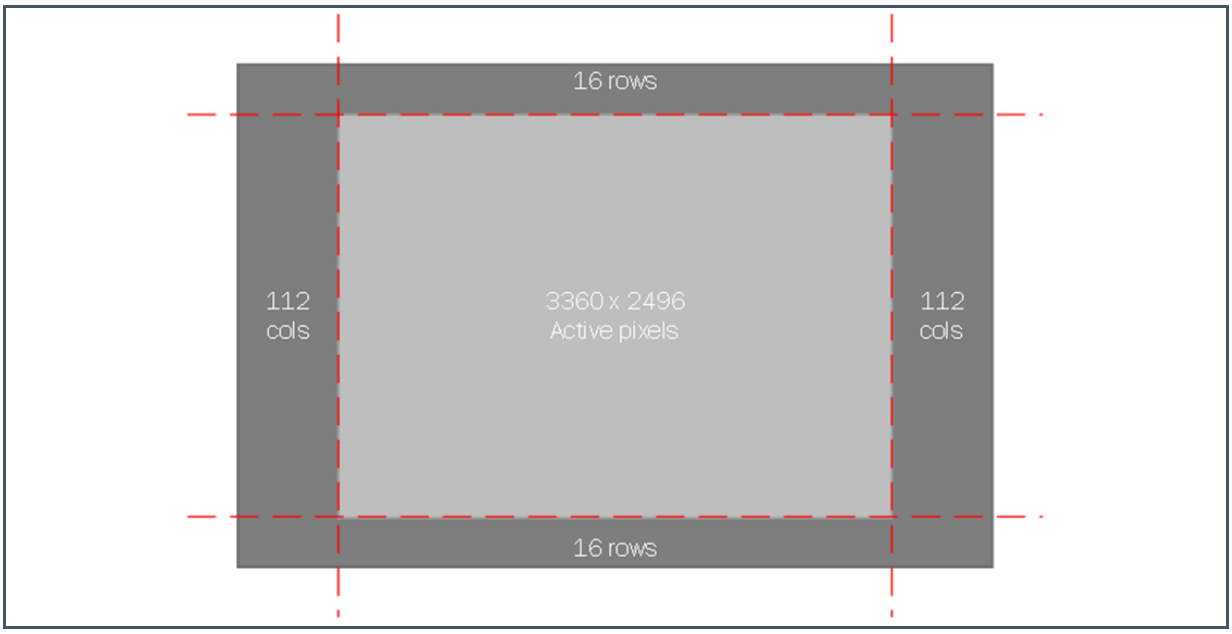
The on-chip sequencer can be controlled through a four-wire serial interface, which reads and writes to the sequencer's control registers. An on-chip temperature sensor can also be read out through this interface.

7.1.1 Pixel Array

The total pixel array consists of 3584 by 2528 pixels, each with a surface of 5.5 µm by 5.5 µm. Of this total array, 224 columns and 32 rows contain an electrical black signal, leaving an active image resolution of 3360 by 2496 pixels. Figure 11 shows the physical layout of the complete pixel array.

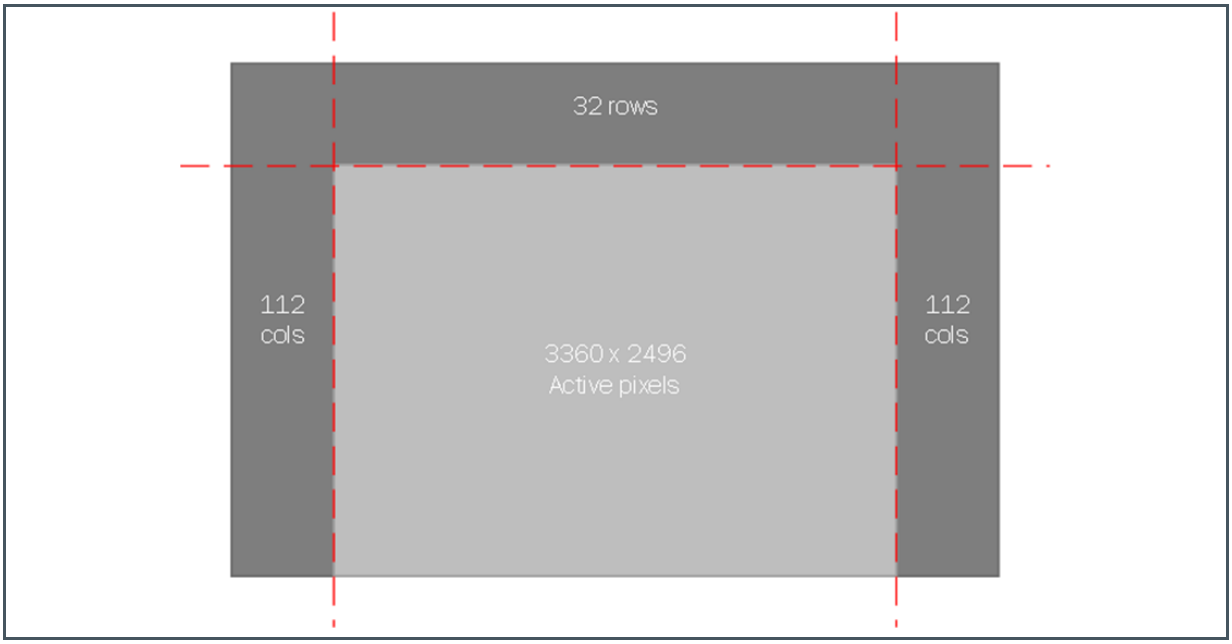
The pixels are designed to achieve maximum sensitivity with low noise and good PLS performance. Microlenses are placed on top of the pixels for improved quantum efficiency.

Figure 11:
Pixel Array Physical Layout



To ensure that the electrical black rows are always read out first by the sequencer, these rows are assigned the 32 lowest logical addresses. When the image is mirrored in the Y-direction, the black rows will still be read out first, from row31 to row0, followed by the active pixels on row32 to row2527. In the image below, the pixel array is plotted to the logical addresses, instead of the physical location.

Figure 12:
Pixel Array Logical Organization



7.1.2 Analog Front End

The analog front-end (AFE) consists of two major parts: a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies an analog gain, programmable through the serial interface.

The column ADC converts the analog pixel value to a 10-bit or 12-bit value. A digital offset can also be applied to the output of the column ADCs.

7.1.3 DPP

The digital data block performs some operations on the digitized pixel data such as digital gain and digital offset adjustment.

7.1.4 LVDS Block

The LVDS block and serializer convert digital pixel data into standard serial LVDS data running at a maximum of 600 Mbps. The sensor has 18 LVDS output pairs.

- 16 data channels
- 1 control channel
- 1 clock channel

The 16 data channels are used to transfer 10-bit or 12-bit words of pixel data from sensor to receiver. The output clock channel is a DDR clock, synchronous to the data on the other LVDS channels. This clock should be used at the receiving end to sample the data. The control channel contains the sync codes for the data channels (DVAL, LVAL, FVAL) and other useful information about the sensor status, such as the integration pulse.

As LVDS is a differential interface, it requires impedance matched traces and a parallel termination at the receiver side. On the sensor input clock IN_LCLK_P (pin T1) and IN_LCLK_N (pin U2), an external 100 Ω resistor should be added. In the same manner, all the LVDS outputs should be terminated at the FPGA side. See the TIA/EIA-644A standard for more details.

7.1.5 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface.

7.1.6 SPI Interface

The SPI interface is used to load the sequencer registers with data. Features like windowing, subsampling, gain and offset are all programmed using this interface. This interface also has read access to these registers to validate a write command, or to read out the temperature sensor.

7.1.7 Temperature Sensor

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI interface. The temperature sensor value can be obtained by reading out the registers with address 88 and 89.

7.2 Operating the Sensor

This section explains how to connect and power the sensor, and basic recipes of how to configure the sensor in a certain operation modes.

7.2.1 Power Supplies

The sensor requires four externally generated supplies as listed in Figure 6.

All variations on the VDD33 and VDDPIX supply can contribute to image noise as they are directly connected to the analog circuits and pixel signals. Therefore, the right precautions should be taken to minimize voltage ripple on these supplies.

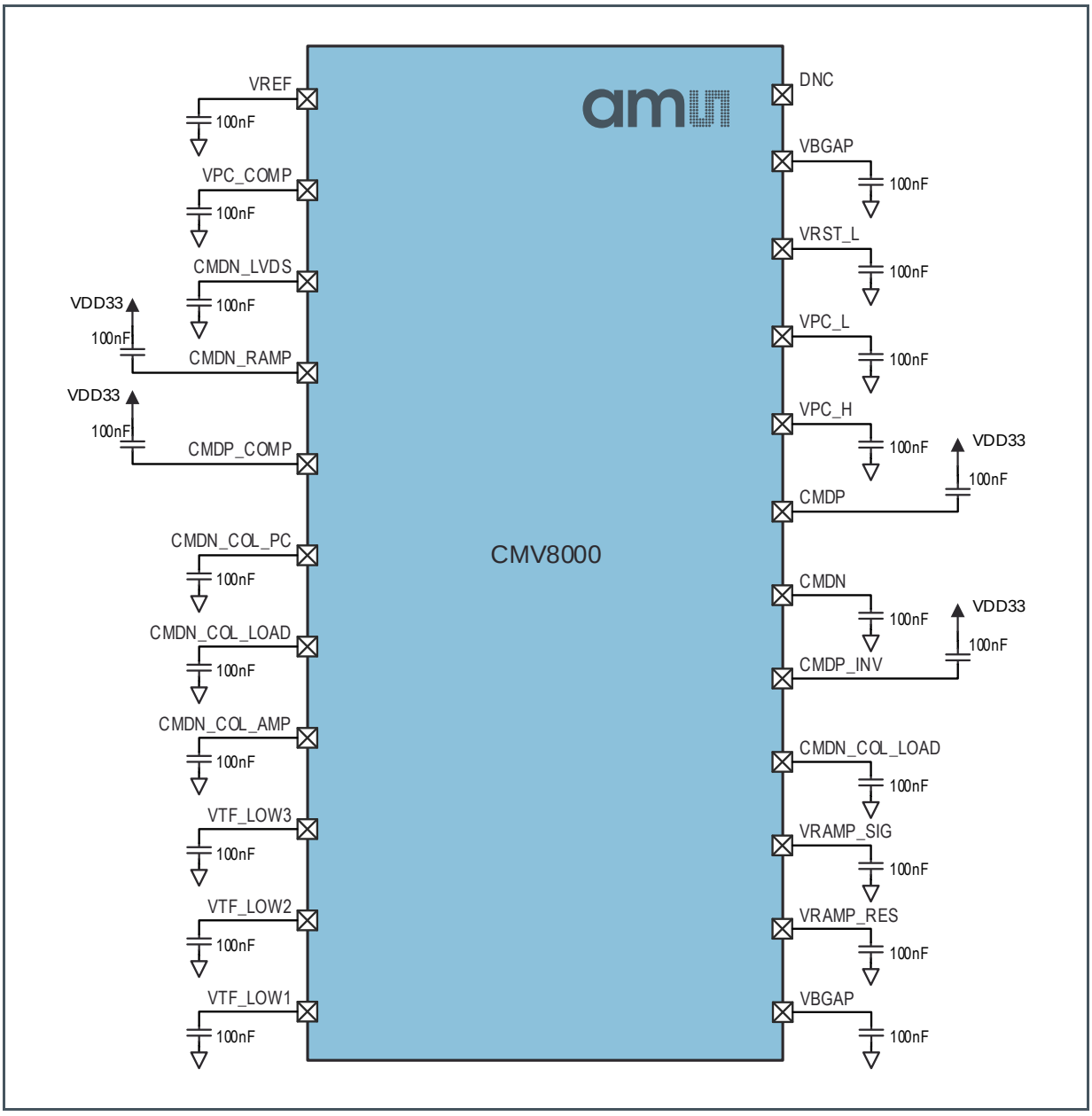
Sufficient decoupling is required, both at the regulator and at the sensor side to minimize the influence of supply variance on the image. We advise to have at least 100 µF bulk capacitance near the regulator of each supply plane (we advise a 330 µF electrolytic, a 33 µF tantalum and a 10 µF ceramic capacitor per supply and directly at the regulator output).

At the sensor side, we advise 4.7 µF and 100 nF ceramic capacitors per power supply pin and 100 µF ceramic capacitor per power supply plane (VDD18, VDDPIX, VDD33), placed closely to the sensor. For the VRST_H supply, a 100 µF capacitor is not required.

Biasing

Some of the sensor pins are regulator outputs that need to be decoupled for the sensor to operate. The capacitor value and connections are detailed in the following diagram. For decoupling, 100 nF ceramic capacitors can be used.

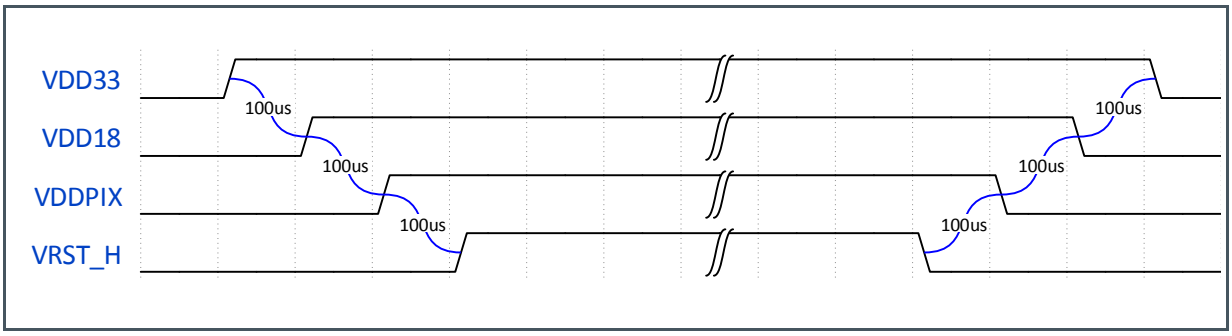
Figure 13:
Connection Diagram



7.2.2 Power-Up/Down Sequence

To avoid putting the sensor in an unknown state and to avoid unexpected current peaks, the following power-up and power-down sequence is advised.

Figure 14:
Supply Power-Up and Power-Down Sequence



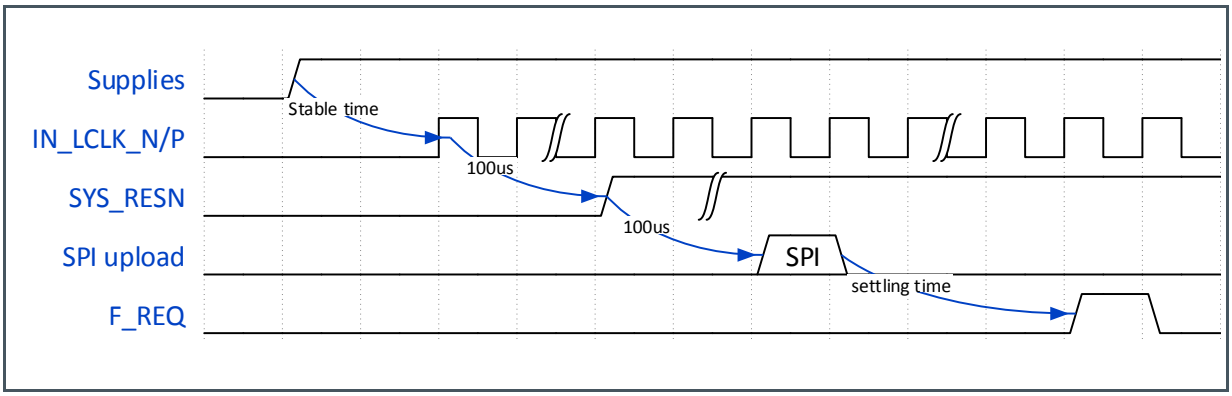
7.2.3 Startup & Reset Sequence

The following sequence should be followed when the sensor is started up.

The input clock should start after the rise time of the supplies. The SYS_RESN pin should be released about 100 µs after the input clock is stable. The recommended register settings can be uploaded 100 µs after the rising edge on SYS_RESN.

The first F_REQ pulse must not be sent until the SPI upload is completed, plus a settling time. This is to ensure that the changes programmed in the SPI upload have taken effect before an image is captured. The settling time is mainly determined by changing the ADC gain, because the voltage the ramp capacitor has to settle. For typical applications, the gain is changed from the default value of 32 to a value that saturates the ADC output (e.g. 39), the settling time is 8 ms. In extreme cases, when the ADC gain would be increased to its maximum value of 63, the settling time can increase to 20 ms. Not respecting the settling time can lead to the first images having an uneven response, or deviating black level.

Figure 15:
Start-Up Sequence



If a sensor reset is necessary during sensor operation, the same sequence should be followed, starting from the rising edge on the SYSRESN pin. A reset action (falling edge on SYSRESN) triggers all programmable registers to return to their default value. After a reset sequence, a minimum time of 1 µs needs to be respected before a frame is requested with the F_REQ pin.

7.2.4 Clocking

The sensor has two input clocks, SPI_CLK and IN_LCLK. The SPI_CLK signal is a standard 3.3 V CMOS signal that is used only for the SPI interface. The OUT_CLK signal is an LVDS clock signal used to drive the image sensor. All internal timing signals are generated from this differential input clock.

Attention

Any change in clock speed during sensor operation must be preceded by setting the clock gating register 123[0] to “1”. After the change is valid, the clock gating register can be set back to “0”.

7.2.5 SPI and Register Access

Programming the sensor is done by writing the appropriate values to the sensor register. These registers are accessed through a four-wire serial interface (SPI). The details of the timing and data format are described below. The registers also have a read function to check their current values.

A single SPI command must consist of the following parts:

- Single control bit, master to slave, signifying a read or write operation
- 7-bit address value of register that is accessed
- 8-bit data value from master to slave(write operation) or from slave to master (read operation)

The sensor operates as an SPI slave.

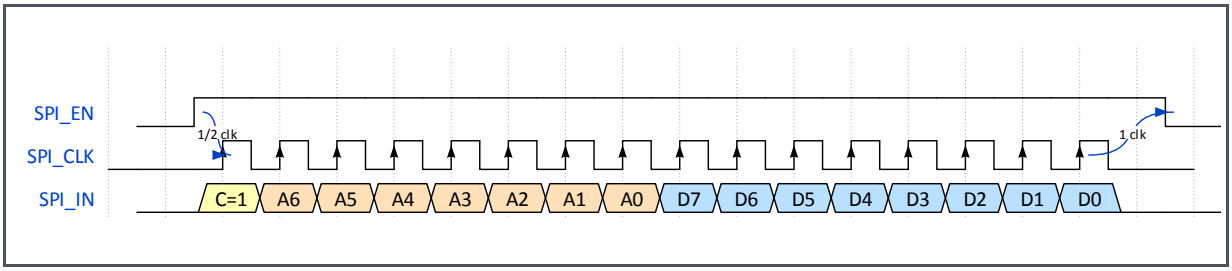
Figure 16:
SPI Signal Overview

Pin Name	Direction	Purpose
SPI_EN	Sensor input	Chip select for image sensor
SPI_CLK	Sensor input	Rising edge triggered clock
SPI_IN	Sensor input (MOSI)	Data from master to slave
SPI_OUT	Sensor output (MISO)	Data from slave to master

SPI Write

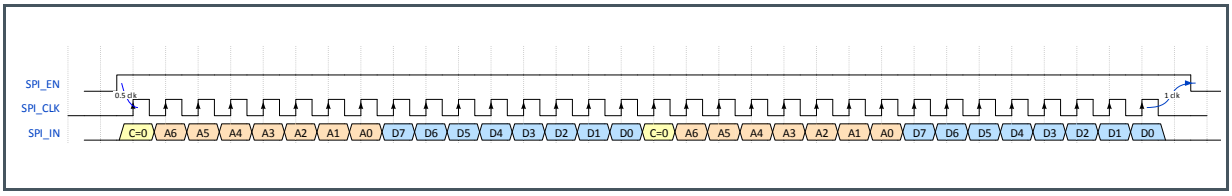
The sensor samples the data on the rising edge of the SPI_CLK. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled and it has to remain high for 1 clock period after the last data bit is sent. SPI_EN has to remain high for 1 clock cycle and SPI_CLK has to receive a final falling edge to complete the write operation.

Figure 17:
SPI Write Timing



If several sensor registers need to be written sequentially, a burst-mode can be used by keeping the SPI_EN signal high continuously. See Figure 18 below for an example of two registers written in burst mode.

Figure 18:
SPI Write Burst



Attention

When SPI_EN is not applied, the SPI_IN line is not put to a high impedance state. This means that, if there are other devices tied to the same SPI bus, a buffer needs to be included on the SPI_IN line to the sensor. This will avoid the SPI_IN input pulling the line low when addressing other devices.

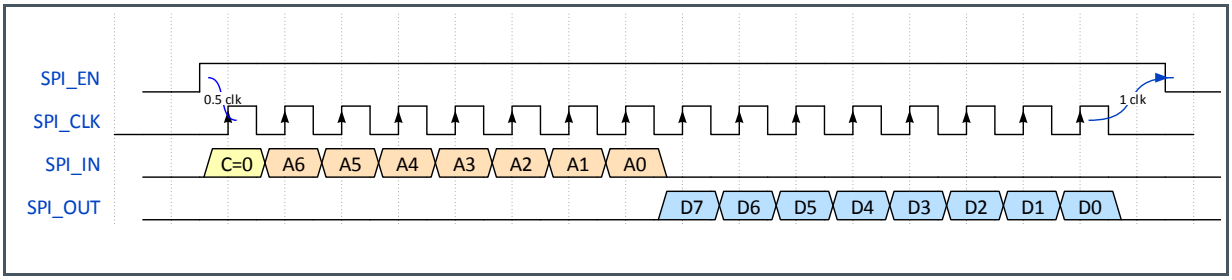
SPI Read

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is set to “0”. The address of the register being read out is sent immediately after this control bit in a MSB first fashion. After the LSB of the address value, the data is launched on the SPI_OUT pin.

Attention

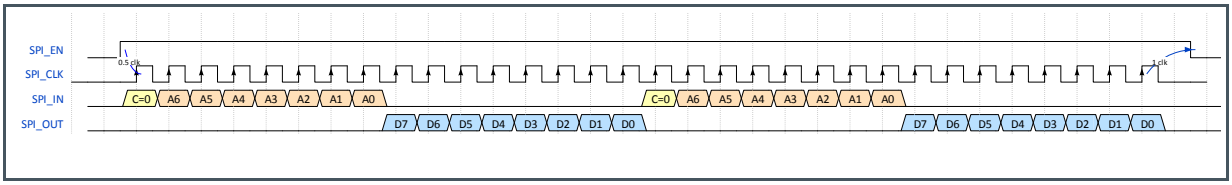
For SPI_CLK frequencies below 30 MHz, the SPI_OUT is best sampled on the rising edge of the clock. For higher frequencies, the SPI+OUT data has to be sampled on the next falling edge. The data is sent over SPI_OUT in MSB first order.

Figure 19:
SPI Read Timing



For reading several register sequentially, the SPI_EN signal stays at a high level in the same fashion as with the write command.

Figure 20:
SPI Read Burst Mode



Register Categories

The registers are grouped into various categories, based on when they can be updated. The category for each register is included in Section 8. The table below explains the different categories.

Figure 21:
Register Categories

Category	Description	Registers
-	Registers without a category can be changed at any time, but might directly influence the sensor execution.	56 – 57

Category	Description	Registers
DC	Can only be changed when the sensor is IDLE or in FOT.	1 – 34, 35-38, 54, 80, 82[4:0], 118
RO	Read-only register. All write operations are ignored.	88-89, 90

7.2.6 Sensor Control Modes

Figure 22:
Control Mode Register

Bit Name	Address	Description
ext[0]	40	0: Internal mode 1: External mode
frames[15:0]	54-55	Set the amount of frames in internal mode

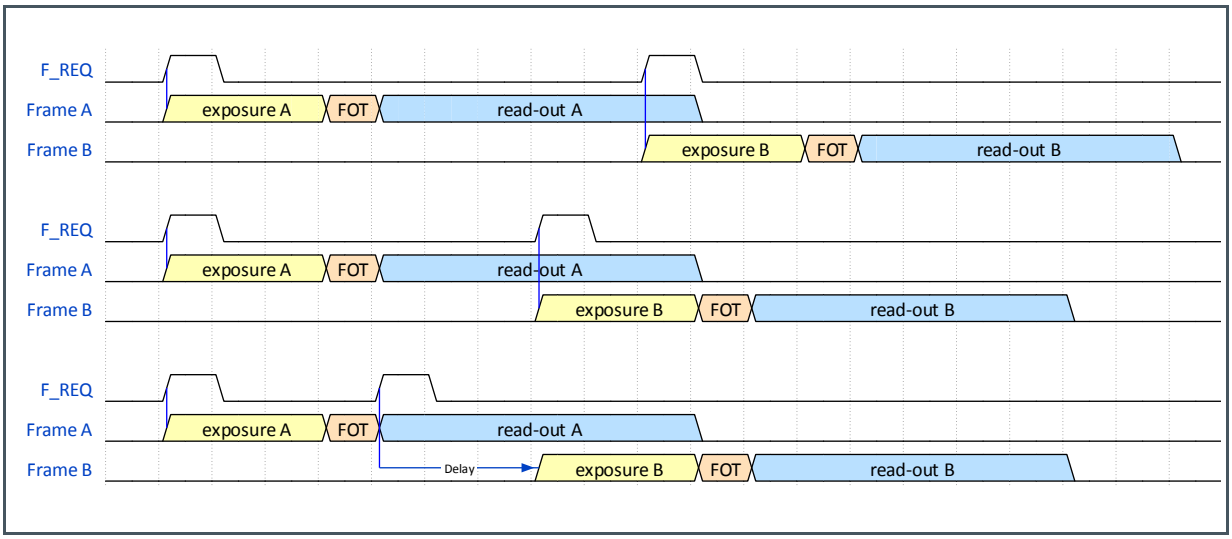
Figure 23:
Control Modes

EXT	Name	External Control (F_REQ pin)	Internal Control
0	Internal mode	Start of exposure	Length of exposure Start of read-out Read-out timing
1	External mode	Start of exposure Start of read-out	Read-out timing

Control Mode 0: Internal Mode

In this mode, a single trigger is needed to request a frame (F_REQ), and the exposure time is set by sensor registers 41 to 43. After a high state on the F_REQ pulse is detected, the sensor will start exposure immediately. Using the register value, the sensor counts down to the end of the exposure time, after which the pixels are sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is sent out. If more than one frame is requested with the **FRAMES** register, the sensor times the start of the next exposure so that the maximum frame rate is guaranteed.

Figure 24:
Request for 2 Frames in Internal Exposure Mode



In some cases the F_REQ timing is such that the exposure start of FRAME B would trigger the read-out period of FRAME B to start when the read-out period of FRAME A has not yet finished, causing a timing conflict.

When using internal exposure mode, the sensor will buffer the start of exposure for FRAME B so that it starts at a time when the read-out of FRAME B would not cause a timing conflict.

This means that this mode is safer when it comes to F_REQ timing because no read-out cut-offs will happen, but also that the delay between F_REQ signal and start of exposure is not always predictable and depends on the circumstances, as shown in Figure 24.

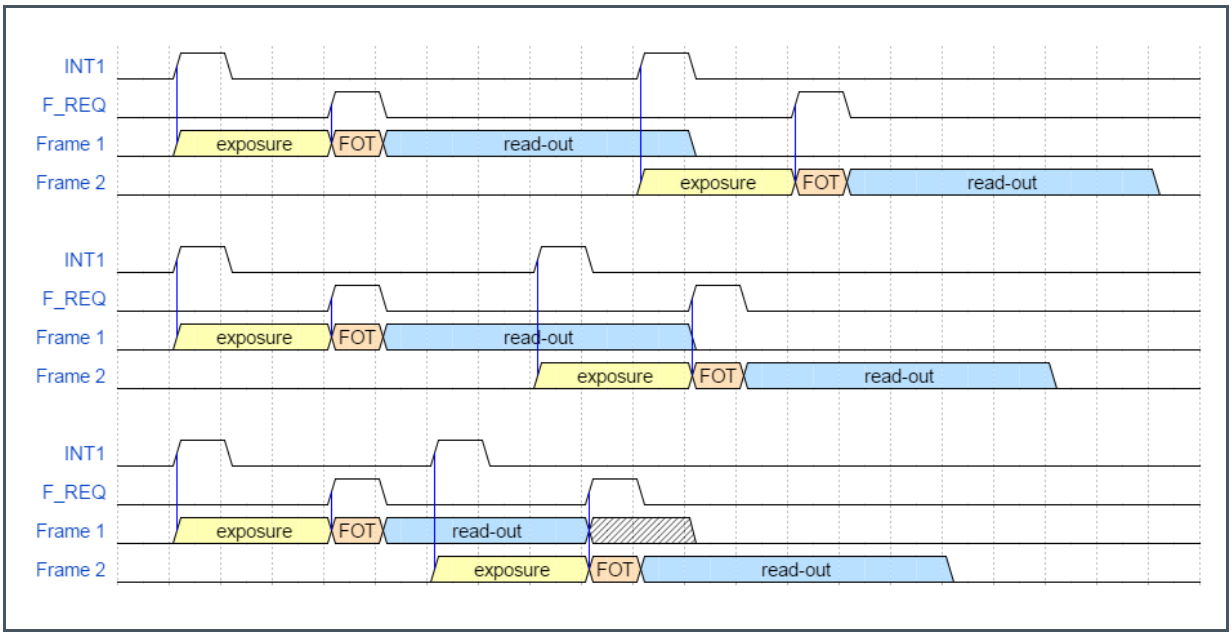
Control Mode 1: External Mode

In external mode, two pulses are needed to request exposure (INT1) and request frame (F_REQ). The time between these pulses determines the exposure time.

In this mode, the F_REQ pulse will start frame-overhead time and read-out period no matter what state the sensor is in. This means that a new exposure can only be requested once the read-out of the current frame has completed, to not cause a cut-off of the current read-out.

When using two exposure groups for HDR imaging, the INT2 pulse controls the exposure of the second exposure group. Both INT1 and INT2 are level sensitive.

Figure 25:
Request for 2 Frames in External Exposure Mode



7.3 Sensor Read-Out Format

7.3.1 LVDS Outputs

The CMV8000 has Low Voltage Differential Signaling (LVDS) outputs to transport the image data to the surrounding system. Next to 16 data channels carrying image data, the sensor has two additional LVDS channels dedicated to sync codes and a Double Data Rate (DDR) clock for sampling. In total, the sensor has 18 LVDS output pairs.

The sensor uses a total of 36 pins for the LVDS outputs. Please refer to the pin list for the pin numbers that assigned to LVDS signaling.

The 16 data channels transfer 10-bit or 12-bit pixel data from the sensor to the receiver, with each pixel value serialized over a single LVDS pair.

The output clock channel OUT_CLK conveys a clock signal, synchronous to the data on the other LVDS channels. It is strongly advised that this clock is used to sample the data instead of an external clock signal. This clock has a double data rate, which means that the pixel data is launched on both rising and falling edges of this signal. When the OUT_CLK is a 300 MHz signal, the output data rate per channel is 600 Mbps.

The control channel puts out sync codes that contain status information of the data channels. This information is grouped in 10-bit or 12-bit words that are sent out synchronous to the 16 data channels.

7.3.2 Readout Format

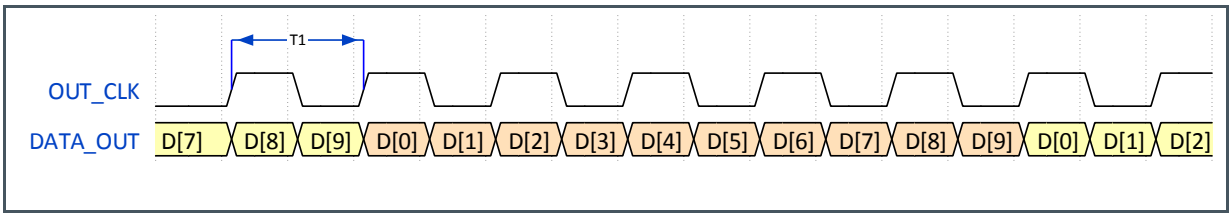
Similar to other CMV products, the data readout is organized in pixels that are aligned using a side-band control channel.

Low-Level Pixel Timing

- Data is transferred in words of 10-bit or 12-bit over each channel, with each word containing the value of a single pixel.
- Data is transferred LSB first

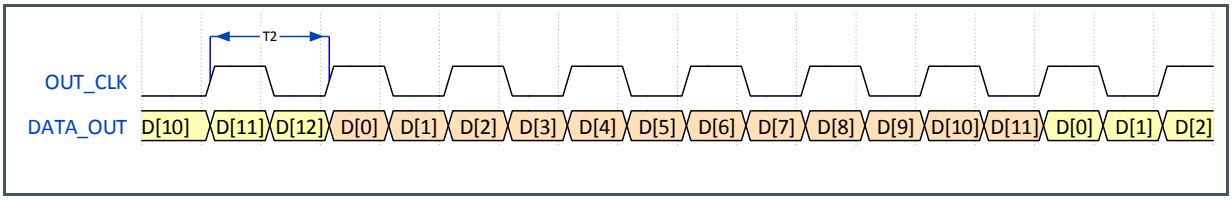
The figure below shows the timing for the read-out of 10-bit and 12-bit pixel data over one LVDS output, together with the DDR output clock (OUT_CLK). The D[0] bit is always transferred during the high phase of the output clock.

Figure 26:
10-Bit Pixel Data



For 10-bit mode, the time ‘T1’ in Figure 26 will be equal to 1 clock cycle of the IN_LCLK input clock. When a frequency of 300 MHz (max for 10-bit mode) is applied to IN_LCLK, this results in a 300 MHz OUT_CLK.

Figure 27:
12-Bit Pixel Data



For 12-bit mode, the time ‘T2’ in the above figure will be equal to 1 clock cycle of the IN_LCLK input clock. When a frequency of 300 MHz is used for IN_LCLK (maximum in 12-bit mode), this results in a 300 MHz OUT_CLK.

Control Channel

The OUT_CTR LVDS output channel is dedicated to the valid data synchronization signals of the data channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers its data in 10-bit or 12-bit words, depending on the selected bit mode. Every bit has a specific function, as described in Figure 28 below.

Figure 28:
Control Word

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data is on the data channels
[1]	LVAL	Indicates validity of a row read-out
[2]	FVAL	Indicates validity of a frame read-out
[3]	SLOT	Indicates the overhead period before 112-pixel bursts
[4]	ROW	Indicates the overhead period before the read-out of a row
[5]	FOT	Indicates when the sensor is in FOT
[6]	INTE1	Indicates exposure of pixels in exposure group 1
[7]	INTE2	Indicates exposure of pixels in exposure group 2
[8]	0	Constant zero
[9]	1	Constant one
[10]	0	Constant zero
[11]	0	Constant zero

Information

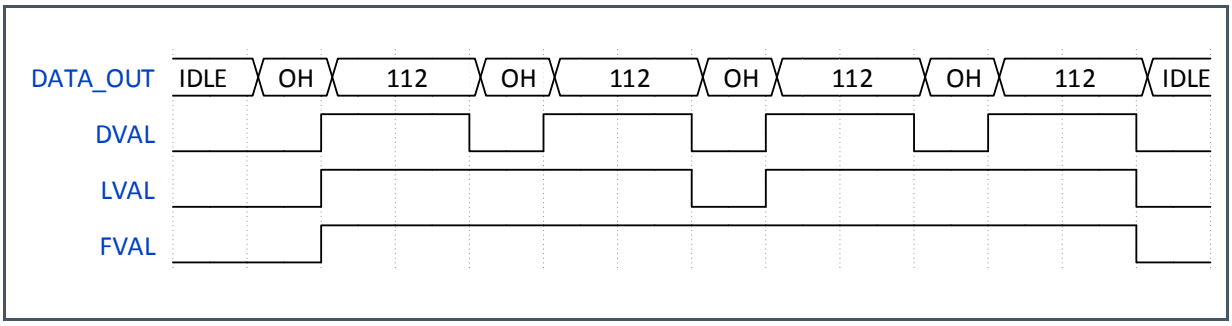
Status bits [3] through [7] are purely informational and are not strictly required for sampling image data. DVAL, LVAL and FVAL signals are sufficient to synchronize the pixel data.

Information

The INTE status bits will be zero at the start of the FOT signal, although the actual exposure time continues during part of the FOT.

Figure 29 shows the timing of the DVAL, LVAL and FVAL codes for the read-out of a frame of 2 rows. This example uses the default mode of 16 LVDS outputs in 10-bit mode.

Figure 29:
Sync Code Timing in 16-Channel Mode

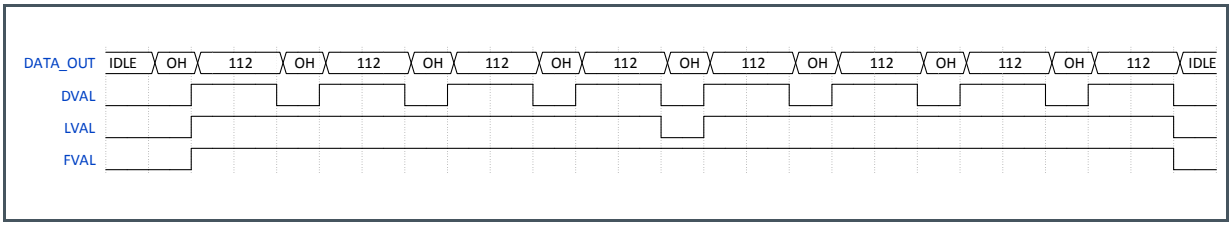


When only 8-channels are used, the line read-out time is 2 times longer. The control channel considers this and adjusts the sync codes (LVAL) to suit the slower read-out. The timing extrapolates identically for 4 and 2 channel read-out.

Attention

At the end of the frame, the DVAL signals last falling edge will occur 5 OUT_CLK cycles before the FVAL and LVAL signals. As the pixel data is sent out at double data rate, this time is equivalent to one 10-bit word of pixel data. The actual end of valid image data only occurs at the falling edge of LVAL and FVAL.

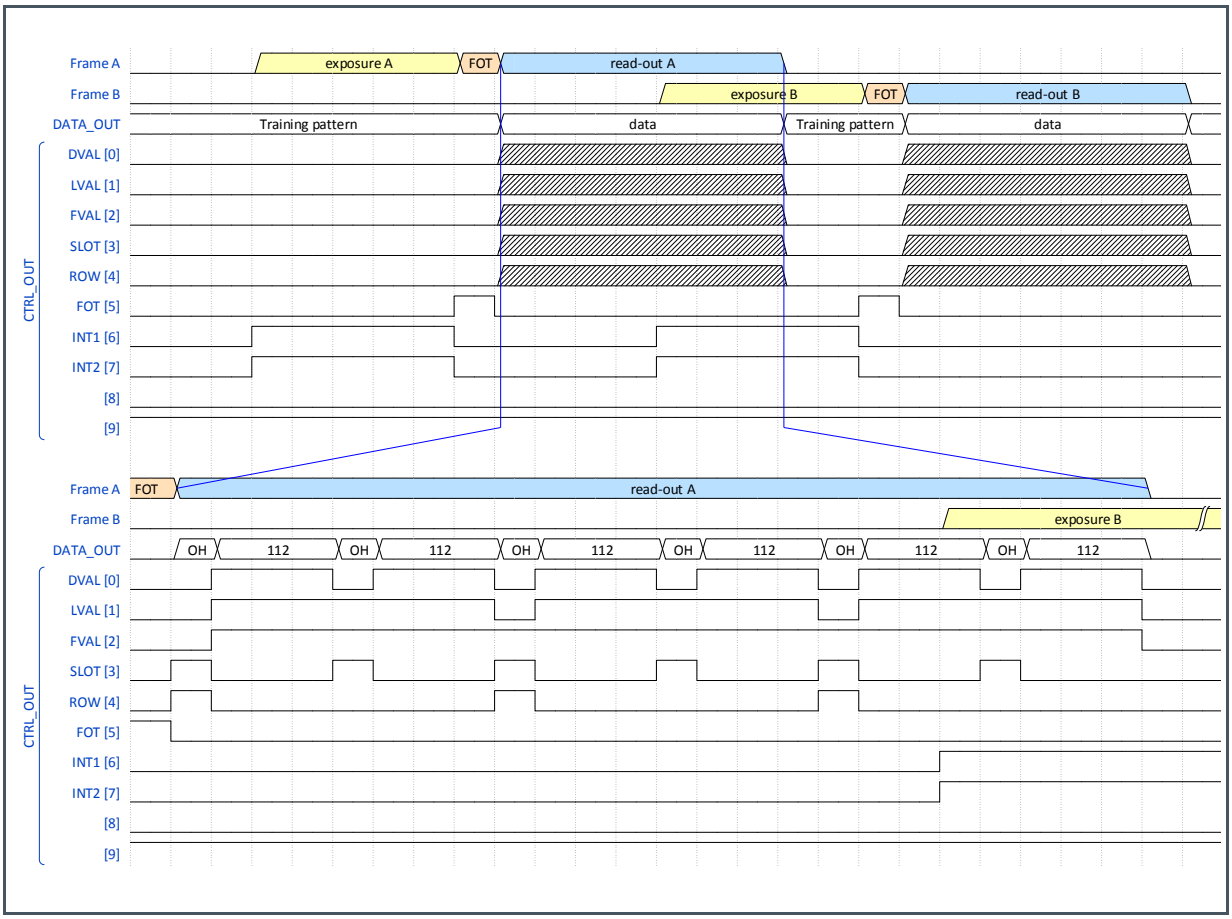
Figure 30:
Sync Code Timing in 8-Channel Mode



The following diagram shows in more detail what happens on the control channel when reading out an image. Two frames are exposed and read out through 16 data channels in 10-bit mode. The DVAL, LVAL and FVAL pulses show when the data is valid for one 112-pixel burst, one row and one frame respectively, while the SLOT and ROW pulses signify the overhead periods between bursts and rows. On the last line, the status of all signals on the control channel is presented in binary format as it is transmitted on the LVDS channel.

Note how bits [8] and [9] have constant values. In 12-bit mode, the control word is expanded to include [10] and [11] of the control word, but remains the same otherwise.

Figure 31:
Detailed Timing of the Control Channel



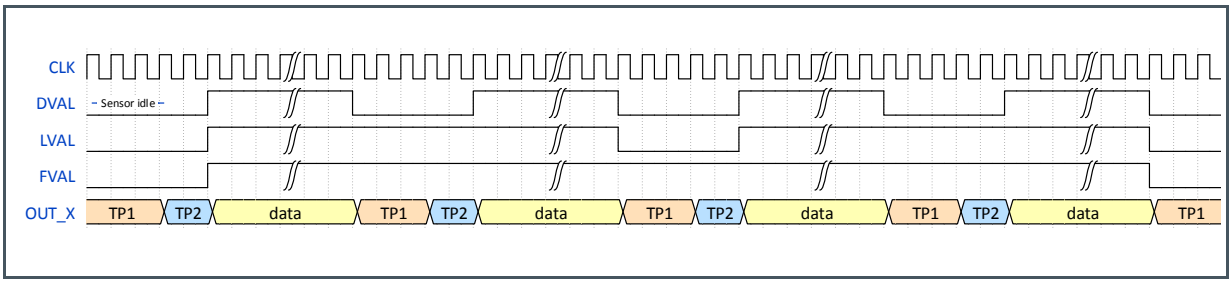
Training Pattern

To synchronize each LVDS output coming from the sensor, a known training pattern is presented on the data channels. This known 10-bit or 12-bit word can be used for bit and word alignment in the receiving system. The training pattern is put out on all active data channels whenever the sensor is idle or in between LVAL and DVAL pulses. The sensor has a 12-bit sequencer register where the user can configure the desired training pattern TP1.

Before each LVAL pulse, the pattern changes to training pattern TP2 for one pixel period. TP2 is derived from TP1, and has the 8 LSBs inverted, and the 4 (or 2) MSBs set to zero.

The figure below shows the location of when each training pattern can be expected. OUT_X represents every active data channel.

Figure 32:
Training Pattern Location



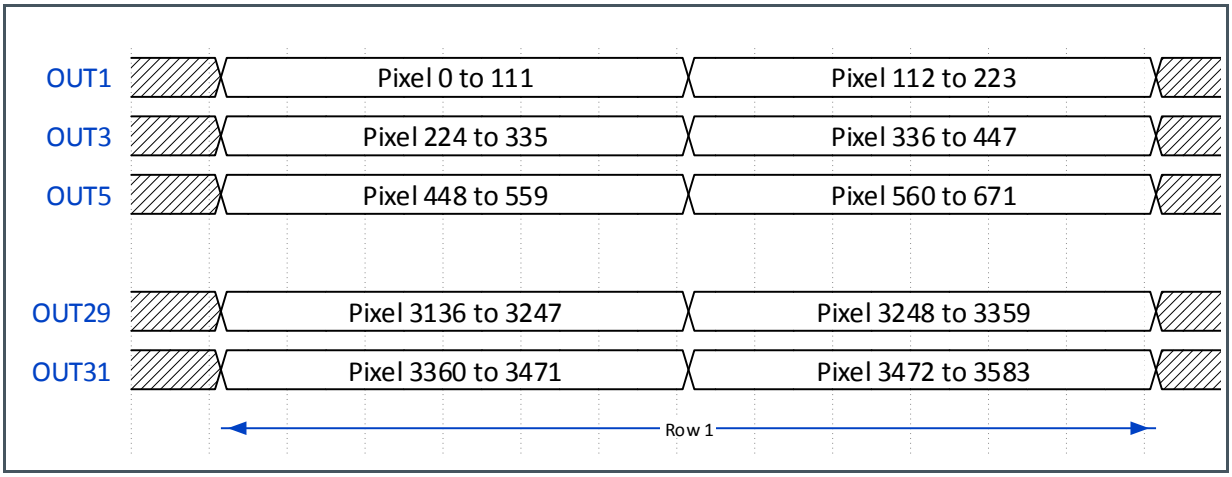
Pixel Remapping

Depending on the number output channels, the pixels are read out by different channels. The following figures detail how pixel data from different columns is presented to different output channels, depending on the multiplex mode.

In each of the following figures, the timing for reading out one row of pixels is illustrated. When the image data is multiplexed to fewer output channels, the unused channels are automatically switched off.

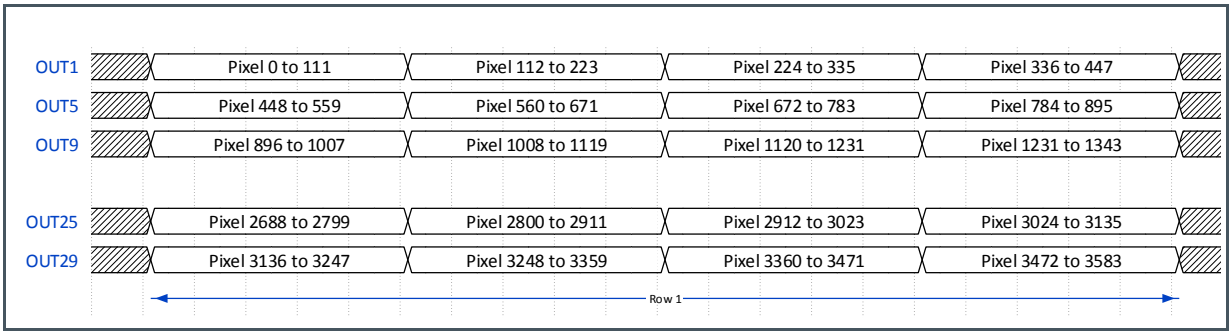
In 16-channel mode, one row is read out over 16 data channels in two bursts of 112 pixels.

Figure 33:
Pixel Remapping for 16 Output Channels



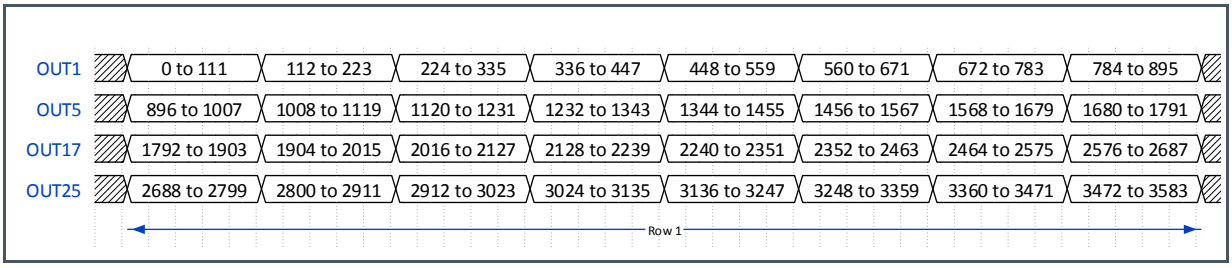
In 8-channel mode, one row is read out over 8 data channels in four bursts of 112 pixels.

Figure 34:
Pixel Remapping for 8 Output Channels



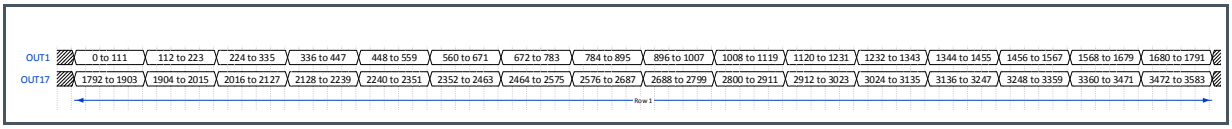
In 4-channel mode, one row is read out over 4 data channels in eight bursts of 112 pixels.

Figure 35:
Pixel Remapping for 4 Output Channels



In 2-channel mode, one row is read out over 2 data channels in sixteen bursts of 112 pixels.

Figure 36:
Pixel Remapping for 2 Output Channels



Output Clock Phase

The sensor output clock is not aligned with the data channels. Therefore, interface training in the receiving system is needed.

7.4 Configuring Readout and Exposure

7.4.1 Frame Time and Exposure Time

The sensor has two modes for initiating an exposure. Control Mode 0 generates the integration time internally by way of a register settings where a single trigger is required to start integration (F_REQ). The second mode, Control Mode 1, requires two external triggers to start integration (INT1) and stop integration (F_REQ). These modes are controlled through sensor registers.

Figure 37:
Exposure Time Registers

Bit Name	Register Address	Description
ext[0]	40	Sets the integration mode
exp_length[23:0]	41-43	Sets the integration time in internal mode

When internal exposure mode is used, the exposure time is controlled by the sensor and can be calculated with the following formula. After the programmed exposure, the pixel starts sampling its signal during FOT, but this does not immediately stop the exposure time. Therefore, the actual exposure time consists of the programmed value in the register and a fraction of the FOT duration.

Equation 1:

$$T_{exp} = T_{reg} + T_{FOT}$$

Equation 2:

$$t = \frac{\#bits}{2} \times T \times \left(\frac{148}{224} \times (224 \times FOT\_LENGTH + 1) + (SLOT\_LENGTH + 1) \times EXP\_LENGTH\right)$$

With

T = Clock period
#bits = ADC bit mode
FOT_LENGTH = Value of address 77
SLOT_LENGTH = Value of address 61
EXP_LENGTH = Value of address 41-43

This same equation in a different form can also be used to calculate the required register value for a certain exposure time.

Equation 3:

$$EXP\_LENGTH = \frac{\frac{exposure\ time}{\frac{\#bits}{5} \times T} - \frac{148}{224} \times (224 \times FOT\_LENGTH + 1)}{SLOT\_LENGTH + 1}$$

When external exposure mode is used, the exposure is controlled by the time between the INT1 and F_REQ, but the additional exposure during FOT is still part of the equation as it is an essential part of the read-out sequence.

Equation 4:

$$t = \frac{\#bits}{2} \times T \times \frac{148}{224} \times (224 \times FOT\_LENGTH + 1) + external\ exposure\ time$$

The minimum value of the **EXP_LENGTH** register is 1. Considering the maximum input clock speed of 300 MHz, the minimum exposure time in internal mode is 125 µs.

In external mode, the minimum time between INT1 and F_REQ is one clock cycle. In this case, the minimum exposure time is 123 µs.

Dual Exposure HDR

In dual exposure mode, the sensor has a different exposure time for the odd and even columns. This mode is available in both external and internal exposure mode.

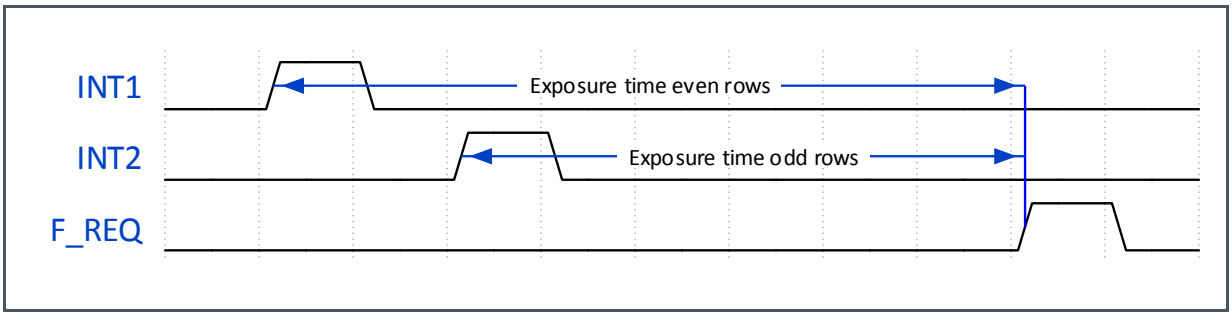
Figure 38:
Dual Exposure Registers

Bit Name	Address	Description
dual[1]	40	0: Dual exposure mode off 1: Dual exposure mode on
exp_length[23:0]	41-43	Set the exposure time for the even columns, when dual exposure mode is on
exp_length2[23:0]	44-46	Sets the exposure time for the odd columns, when dual exposure mode is on

The sensor does not recombine the odd and even columns in this mode, this should be done by the receiving system.

For external exposure mode, the **EXP_LENGTH** registers are not used. Therefore, enable the dual[1] bit on the **INTE** register and apply pulses to the INT1 and INT2 pins to start exposure on odd and even columns. A pulse on F_REQ will stop exposure on all columns.

Figure 39:
Dual Exposure in External Mode



When a color sensor is used, the dual exposure mode has to be adjusted to preserve the Bayer pattern. By enabling the following register, the two exposure groups are valid for two adjacent columns.

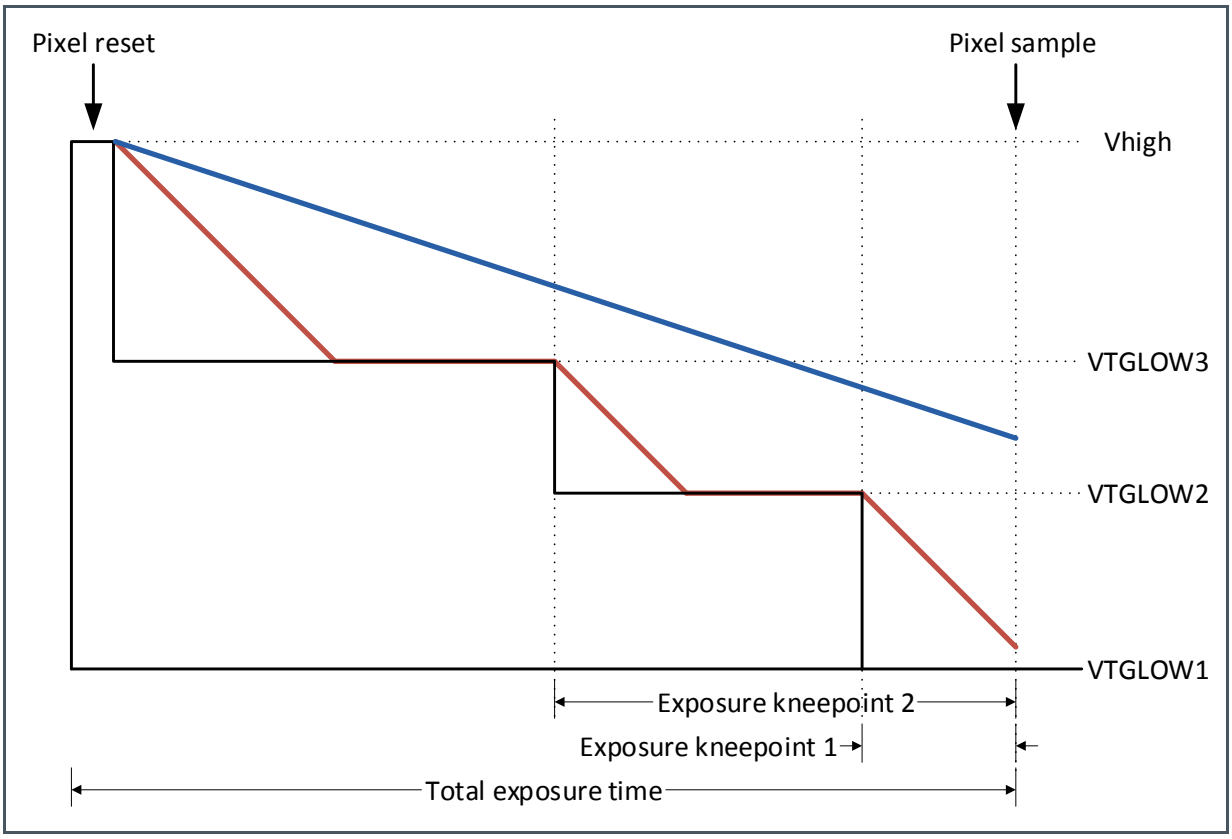
Figure 40:
Color Registers

Bit Name	Address	Description
mono[0]	121	0: Color sensor is used 1: Monochrome sensor is used

Piecewise Linear Response HDR

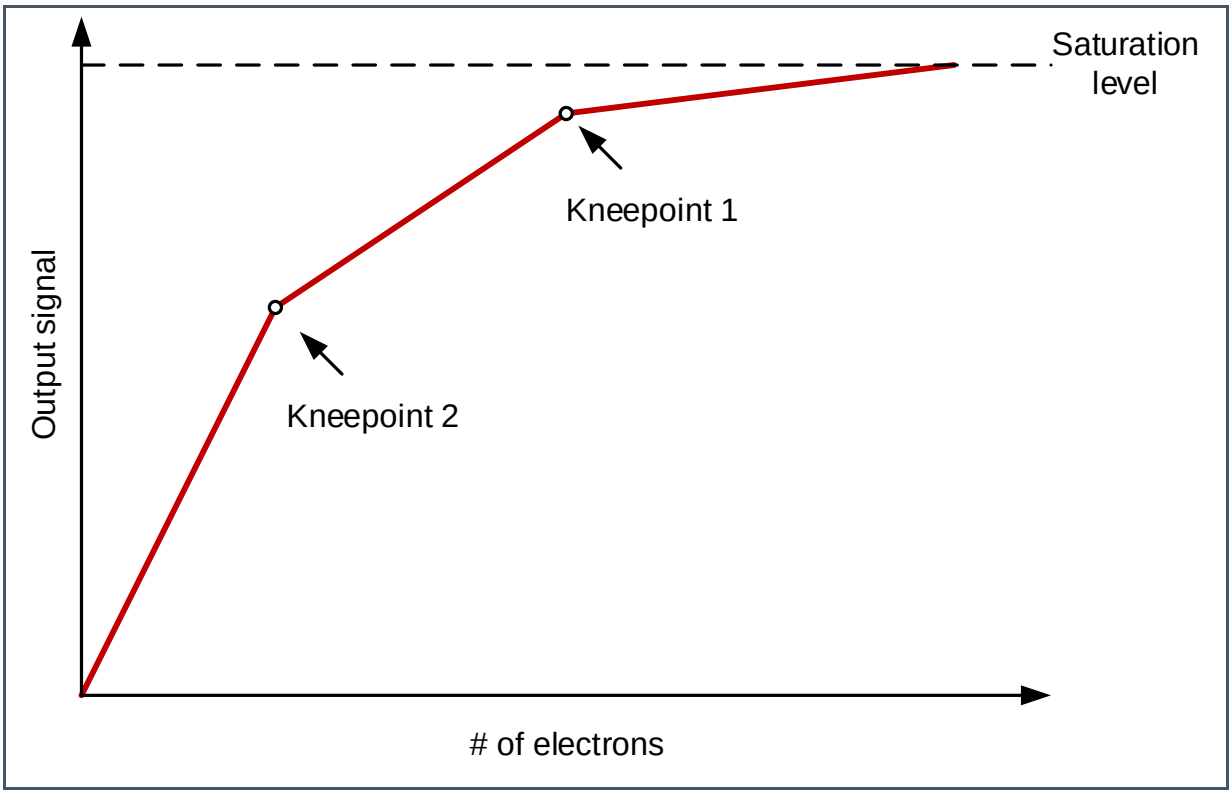
The sensor has the option to achieve a higher optical dynamic range by configuring the pixel to have a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted two times within one exposure to achieve a maximum of three linear slopes in the response curve.

Figure 41:
Programmable Multiple Slope Response



In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to not saturate the pixel at the end of the exposure time. This does not influence the darker pixels, so they will have a normal response. The VTGLOW voltages and different exposure times are programmable using the sequencer registers. The VTGLOW programming controls the placement of the knee points on the X-axis, while the programmed exposure times control the slope of the segments. With both these features, you can achieve a response as seen in the figure below.

Figure 42:
Piecewise Linear Response



This mode can be both used in internal and external exposure mode. In the latter case, only the VTGLOW registers need to be set and the kneepoints are controlled by pulsing the INT1 signal, as shown in Figure 43.

Figure 43:
Piecewise Linear With External Exposure Mode

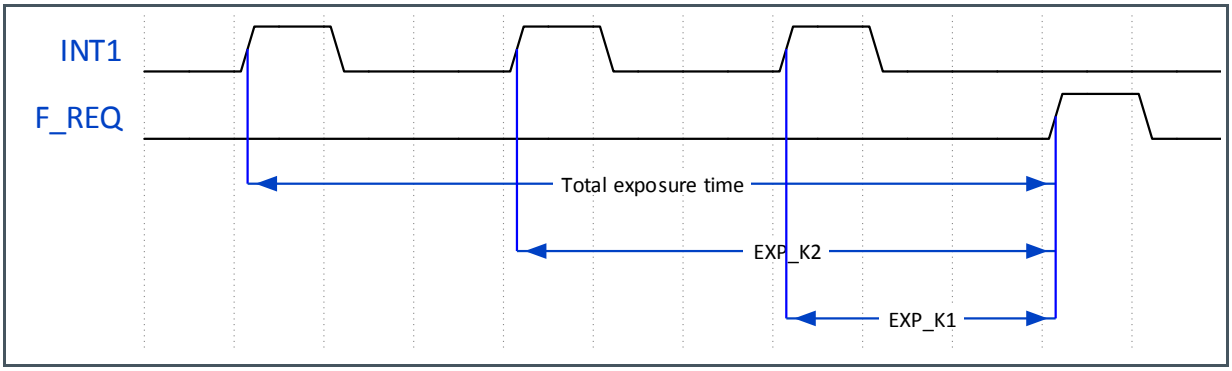


Figure 44:
Piecewise Linear Registers

Bit Name	Address	Description
exp_length[7:0]	41-43	Set the total exposure time
slopes[1:0]	47	Set the number of slopes
exp_k1[7:0]	48-50	Set the exposure time of kneepoint 1
exp_k2[7:0]	51-53	Set the exposure time of kneepoint 2
vtglow1[6:0]	94	Set the VTGLOW1 voltage Bit[6] = Enable Bit[5:0] = Set voltage between 0 V and 1.8 V (linear)
vtglow2[6:0]	95	Set the VTGLOW2 voltage Bit[6] = Enable Bit[5:0] = Set voltage between 0 V and 1.8 V (linear)
vtglow3[6:0]	96	Set the VTGLOW3 voltage Bit[6] = Enable Bit[5:0] = Set voltage between 0 V and 1.8 V (linear)

Maximum Frame Rate Calculation

The frame rate is determined by two factors.

- Exposure time
- Frame time

In case the exposure time is longer than the frame time, the frame rate is entirely determined by the exposure time and is thus dependent on the user. For the following calculation, we assume that the exposure time is shorter than the frame time, which means the frame rate is defined by the sensor. The frame time depends on the following factors:

- Clock speed
- ADC mode
- Number of lines in the frame
- Multiplexing mode

If any of these parameters change, it will have an impact on the maximum frame rate of the sensor. For this calculation the following assumptions are made:

- Clock speed: 300 MHz
- ADC mode: 10-bit
- Full resolution frame
- Multiplexing mode: All 16-LVDS outputs used

First, the frame overhead time is calculated. In this sequence, the sensor samples the signal in the pixel and presents it to the read-out.

Equation 5:

$$FOT = \frac{\#bits}{2} \times T \times \left(224 \times FOT\_LENGTH + 1 + 112 + 2 \times 113 \times \frac{32}{\#outputs}\right)$$

With the above assumptions in mind and with the FOT_LENGTH register set to 50, the frame overhead time is 196.08 µs.

The rest of the frame time is defined by the read-out sequence:

Equation 6:

$$readout = \left((SLOT\_LENGTH + 1) \times \frac{\#bits}{2} \times T \times \frac{32}{\#outputs}\right) \times YSIZE\_TOT$$

When reading out a full resolution image with the recommended settings in 10-bit mode this results in a read-out time of 9522.13 µs.

The total frame time is now the sum of both the frame overhead time and the read-out time, or 9718 µs. The maximum frame rate is thus 102.9 FPS.

The table below gives a few examples of how the frame rate increases when the frame size is reduced.

Figure 45:
Typical Frame Rates

Frame Size	Number of Columns	Number of Lines	Max Frame Rate
Full resolution	3584	2528	103
Active rows only	3584	2496	104
Largest 16/9 window	3584	1890	139
Half resolution	3584	1264	202
Largest 21/9 window	3584	1440	177
100 lines	3584	100	1746

Using 12-bit mode changes the ADC conversion time and the frame time, so the above formulas have to be adjusted. In this case, the FOT is defined by:

Equation 7:

$$FOT = \frac{\#bits}{2} \times T \times \left(224 \times FOT\_LENGTH + 1 + 112 + 4 \times 125 \times \frac{32}{\#outputs}\right)$$

In the same fashion, the read-out time is defined by:

Equation 8:

$$readout = \left(2 \times (SLOT\_LENGTH + 1) \times \frac{\#bits}{2} \times T \times \frac{32}{\#outputs}\right) \times YSIZE\_TOT$$

This leads to a reduced max. frame rate of 40 FPS for 12-bit mode and a full resolution image.

Sequence Length

In internal exposure mode, each high level on the F_REQ pin will trigger exposure and read-out of one or more frames. With the FRAMES register, the user can control how many frames will follow after the F_REQ pulse. The sensor adjusts the timing of these frames so that the maximum frame rate for that use case is achieved.

Figure 46:
FRAMES Register

Bit Name	Address	Description
frames[15:0]	54-55	Sets the number of frames in internal exposure mode

7.4.2 Windowing

The sensor supports several windowing modes in the vertical direction to create different regions of interest.

Vertical ROI Settings

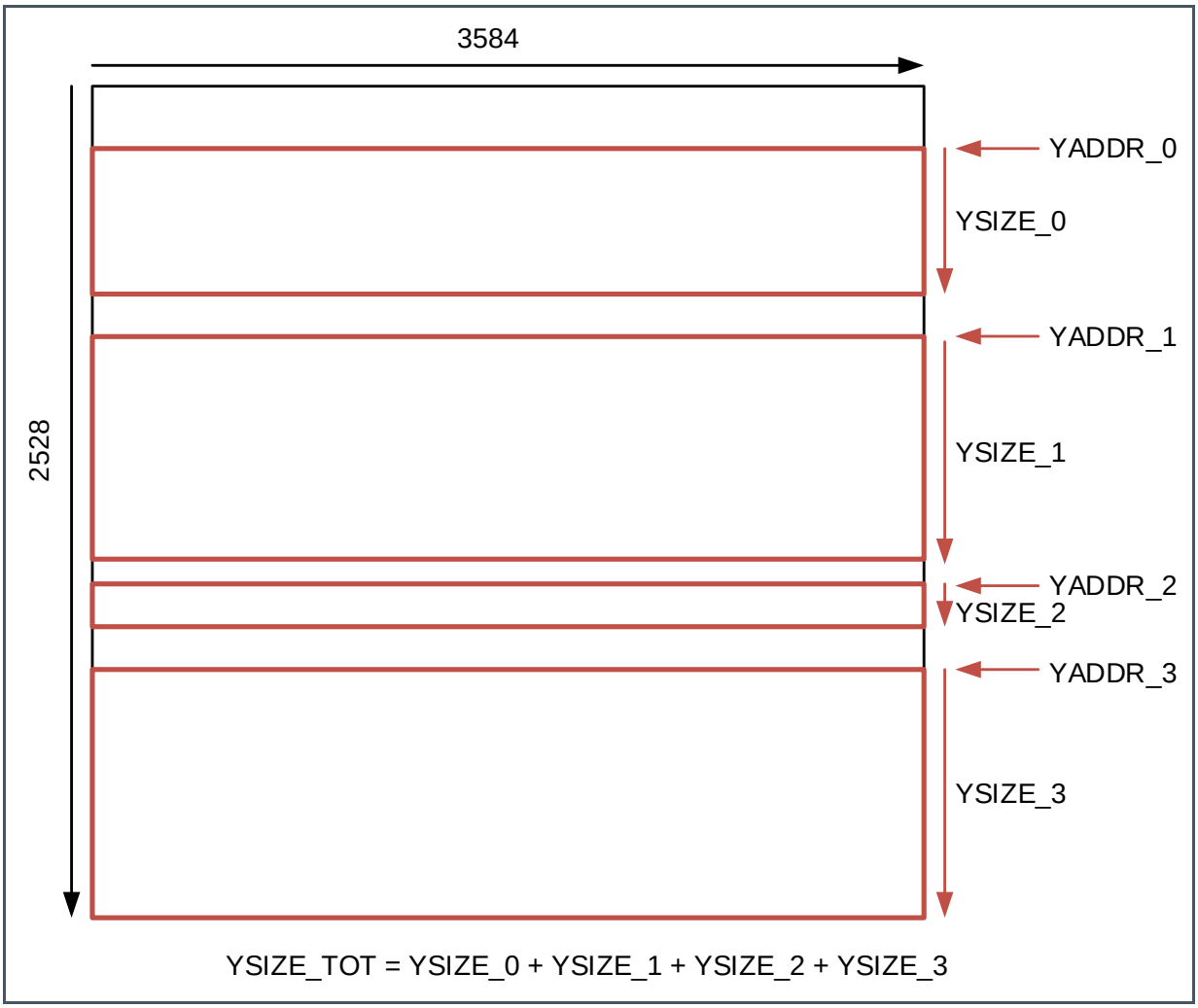
To limit the amount of data or to increase the frame rate of the sensor, windowing in Y-direction is supported. The amount of windows can vary from 1 to 8. The number of lines for each window and the start addresses can be set by programming the registers in the table below. The YSIZE_TOT register needs to be programmed at all times as the sum of all window sizes. The sensor reads out the pixel array from window 0 to window 7, regardless of the rows that these windows address. The default mode is to read out a single window with the full frame size of 2528 rows.

Figure 47:
Windowing Registers

Bit Name	Address	Description
ysize_tot[15:0]	1-2	Set the total number of lines to read out

Bit Name	Address	Description
yaddr_0[15:0]	3-4	Set the start address for window 0
yaddr_1[15:0]	5-6	Set the start address for window 1
yaddr_2[15:0]	7-8	Set the start address for window 2
yaddr_3[15:0]	9-10	Set the start address for window 3
yaddr_4[15:0]	11-12	Set the start address for window 4
yaddr_5[15:0]	13-14	Set the start address for window 5
yaddr_6[15:0]	15-16	Set the start address for window 6
yaddr_7[15:0]	17-18	Set the start address for window 7
ysize_0[15:0]	19-20	Set the number of rows in window 0
ysize_1[15:0]	21-22	Set the number of rows in window 1
ysize_2[15:0]	23-24	Set the number of rows in window 2
ysize_3[15:0]	25-26	Set the number of rows in window 3
ysize_4[15:0]	27-28	Set the number of rows in window 4
ysize_5[15:0]	29-30	Set the number of rows in window 5
ysize_6[15:0]	31-32	Set the number of rows in window 6
ysize_7[15:0]	33-34	Set the number of rows in window 7

Figure 48:
Example of Multiple Window Configuration



Window Overlap

In case the windows overlap, rows can be read out twice for the same exposure. However, due to destructive read-out nature of the sensor, valid image data will only appear on these rows for the first read-out.

7.4.3 Vertical Subsampling

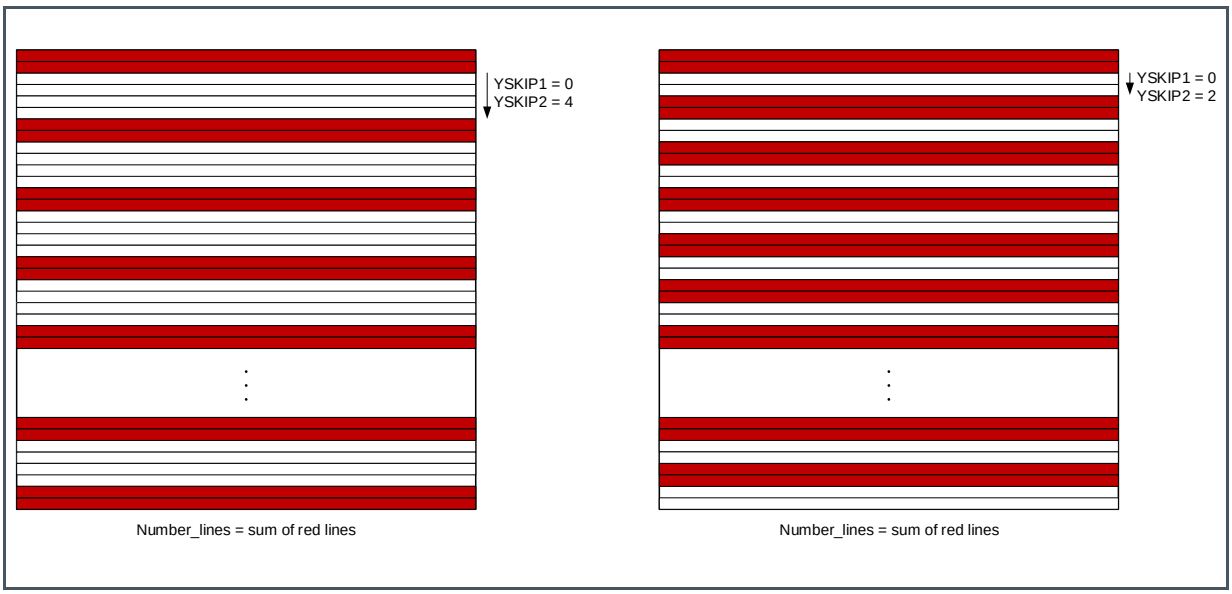
Figure 49:
Vertical Subsampling Registers

Bit Name	Address	Description
ysize_tot[7:0]	1-2	Set the total number of lines to be read out by the sensor
yskip1[7:0]	35-36	Set the number of rows to skip in group 1
yskip2[7:0]	37-38	Set the number of rows to skip in group 2

To maintain the same field of view, but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers, which can be found in the table above.

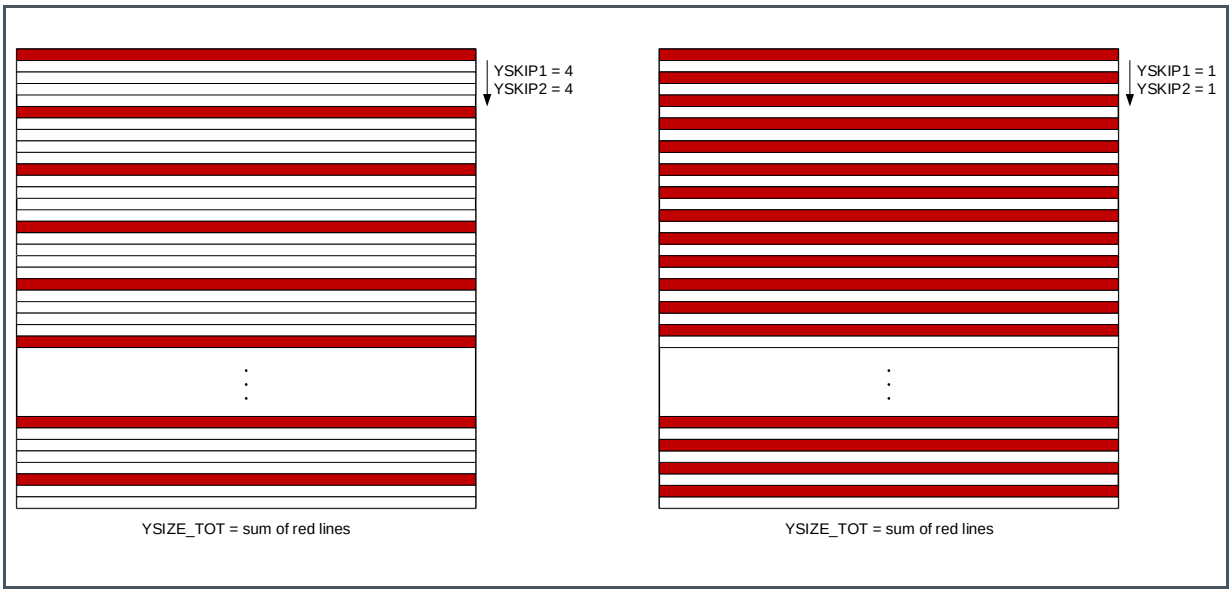
For a color sensor, the value of YSKIP1 should be set to 0 and YSKIP2 to an even number. This ensures that the Bayer pattern is preserved in the subsampled image by reading out two adjacent lines.

Figure 50:
Subsampled Image for Color Sensor



For a monochrome sensor, the values of YSKIP1 and YSKIP2 should be equal to skip single or multiple lines.

Figure 51:
Subsampled Image for Monochrome Sensor



7.4.4 Mirroring

The image can be mirrored, both in the X and Y direction. In the example below, 2 channel output mode is used to simplify the figure. When mirroring is disabled, output channel OUT1 reads out first the pixel in the top left of the array (pixel (0,0). When mirroring in Y is enabled, OUT1 starts from the last row at pixel (0,2495) in the bottom left of the array and counts downwards to pixel (0,0). When mirroring in X is enabled, only the pixels within an output channel are mirrored. In this mode, OUT1 will start reading out pixel (1679,0) first and then count to pixel (0,0) in the top left of the array.

Figure 52:
Image Mirroring

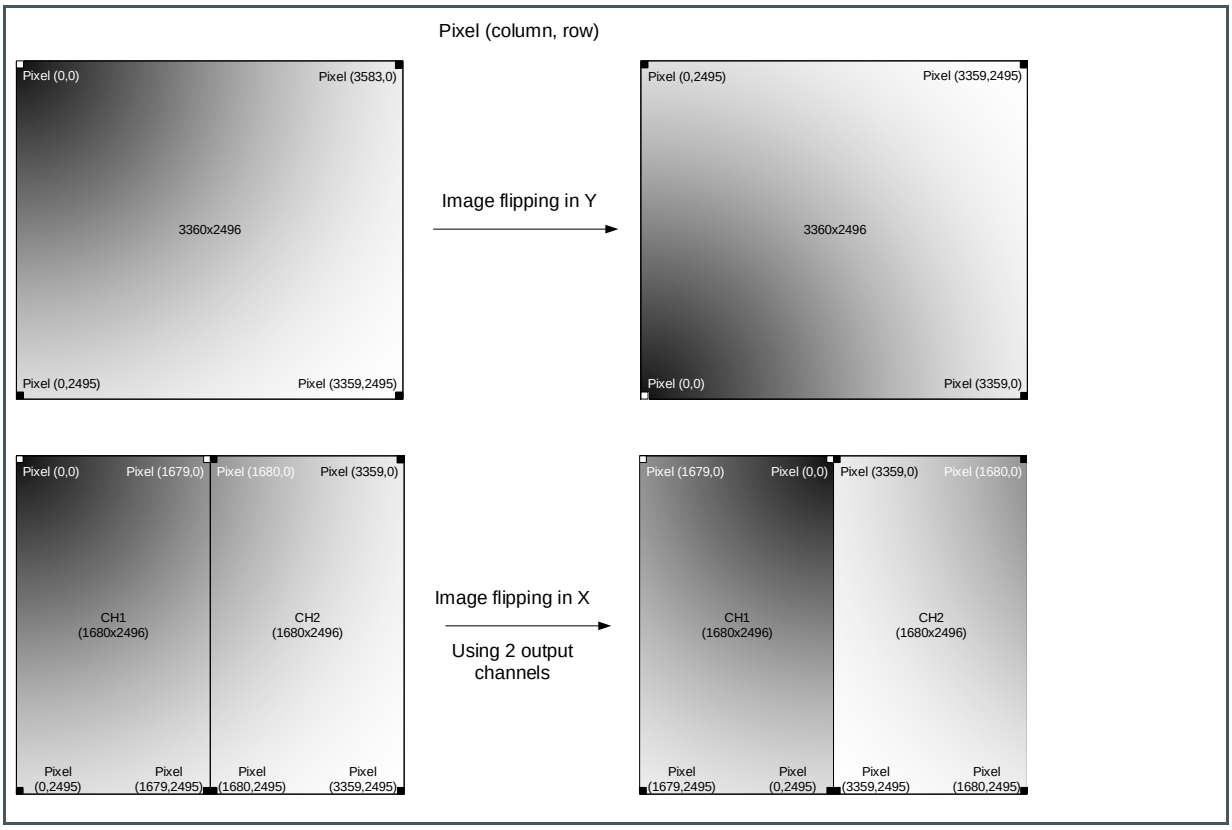


Figure 53:
Mirroring Register

Bit Name	Address	Description
mirror[1:0]	39	0: No mirroring 1: Mirroring in X 2: Mirroring in Y 3: Mirroring in X and Y

7.5 Configuring the Output Data Format

7.5.1 Word Alignment

To do word alignment in the receiving system, a training pattern TP1 is sent out over the data channels whenever the sensor is idle, and in between LVAL and DVAL pulses. TP1 is a 10-bit or 12-bit word that can be configured with a register.

Figure 54:
Training Pattern

Bit Name	Address	Description
lvds_train[12:0]	56 - 57	The 12 LSBs of this 16-bit word are sent in 12-bit mode. In 10-bit mode, the 10 LSBs are sent.

7.5.2 Bit Depth

The on-chip ADC can be configured to do a 10-bit or 12-bit conversion. Because the 12-bit conversion takes more time to complete, the on-chip read-out timing needs to be adjusted and the frame rate will be lower. The user can select the desired ADC resolution by programming the following sequencer registers.

Figure 55:
Bit Depth Registers

Bit Name	Address	Description
slot_length[7:0]	61	112: 10-bit mode 122: 12-bit mode
row_length[5:0]	62	2: 10-bit mode 4: 12-bit mode
smp_length[8:0]	65 - 66	96: 10-bit mode 231: 12-bit mode
adc_ramp_r_size[8:0]	71 - 72	29: 10-bit mode 54: 12-bit mode
adc_interval[7:0]	73	19:10-bit mode 1: 12-bit mode
adc_ramp_s_size[9:0]	74 - 75	120: 10-bit mode 397: 12-bit mode
db_offset_data[11:0]	80 - 81	444: 10-bit mode 1966: 12-bit mode

Bit Name	Address	Description
db_dig_gain[4:0]	82	4: 10-bit mode 1: 12-bit mode
lvds[1]	83	1:10-bit mode 0: 12-bit mode
div[4:0]	84	4: 10-bit mode 5: 12-bit mode
v_ramp_res[6:0]	115	70: 10-bit mode 76: 12-bit mode
v_ramp_sig[6:0]	116	70: 10-bit mode 76: 12-bit mode
tune[2:0]	117	0: 10-bit mode 3: 12-bit mode
gate_parallel_clock[0]	123	Set to 1 before adjusting settings

Attention

Whenever changing bit mode when the sensor is in operation, set register 123[0] to 1 before adjusting any of the registers above.

7.5.3 Outputs

The sensor has in total 16 LVDS channels that transport pixel data. It is also possible to multiplex the pixel data to fewer outputs for receiving systems that do not support as many I/Os or for power sensitive applications.

The number of LVDS data channels can be programmed with the MUX register. Because each row takes longer to read out in a multiplexed configuration, the ROW_LENGTH register also has to be adjusted.

Figure 56:
Multiplexing Registers

Bit Name	Address	Description
mux[4:0]	59	1: 16 outputs 3: 8 outputs 7: 4 outputs 13: 2 outputs

Bit Name	Address	Description	
		10-bit mode	**12-bit mode**
row_length[6:0]	62	2: 16 outputs 4: 8 outputs 8: 4 outputs 16: 2 outputs	4: 16 outputs 8: 8 outputs 16: 4 outputs 32: 2 outputs

When multiplexing data to less than 16 output channels, the remaining LVDS channels are switched off automatically. The following table details which channels remain active in the different multiplexing modes.

Figure 57:
Active LVDS Channels

MUX	Active LVDS Channels	Pixels Per Channel
3	OUT1, OUT5, OUT0, OUT13, OUT17, OUT21, OUT25, OUT29	224
7	OUT1, OUT9, OUT17, OUT25	448
15	OUT1, OUT17	896

7.6 Configuring the On-Chip Data Processing

7.6.1 Setting the Black Level

Figure 58:
Offset Register

Bit Name	Address	Description
db_offset_data[11:0]	80-81	Set the black level of the sensor in 1DN increments

A digital offset can be applied to the output signal. This dark level offset can be programmed by setting the desired value in the DB_OFFSET_DATA register. This 12-bit register value is a 2-complement number, allowing addition and subtraction from the current black level, from +2047 to -2048. The ADC itself has a fixed offset of -440DN.

To calculate the sensor black level, use the ADC offset and add or subtract the DB_OFFSET_DATA value. For example, with the default value of this register at 444, the typical black level of the sensor should be -440 + 444 = 4DN in 10-bit mode. For a register value greater than 2048, the value is converted to a negative number like in Figure 59 below:

Figure 59:
Offset Calculation

DB_OFFSET_DATA Value		Effect on Offset
Decimal	**Binary**	
0	0000 0000 0000	+0
1	0000 0000 0001	+1
...	...	...
2047	0111 1111 1111	+2047
2048	1000 0000 0000	+2048
2049	1000 0000 0001	-2047
...	...	...
4095	1111 1111 1111	-4095

7.6.2 Analog and Digital Gain

Figure 60:
Analog Gain Register

Bit Name	Address	Description
pga_gain[3:0]	118	Set the gain of the column amplifier

Register PGA_GAIN is used to apply an analog gain to the signal on the column bus. In low light conditions, increasing the analog gain should be the primary action to increase signal to noise ratio. This lowers the sensor read noise. Figure 61 details the gain settings that can be applied.

Figure 61:
Analog Gain Setting

PGA_GAIN Value	Applied Gain Level
7	1
15	1.33
14	2
5	3
13	4

The ADC also has a gain level that stems from the adjustable slope on the ADC ramps.

Figure 62:
ADC Gain Setting

Bit Name	Address	Description
adc_gain[5:0]	117	Set the slope of the ADC ramp

Careful consideration should be taken when adjusting the ADC_GAIN setting, as this also changes the reference values for the ADC ramps. The default value of this register is 32, which corresponds to a gain of x1. Setting this register to 48 will give a gain of around x2, but column noise can occur due to the difference in reference levels.

7.7 Additional Features

7.7.1 Digital Test Outputs

Figure 63:
Digital Test Output Register

Bit Name	Address	Description
tmuxd1[3:0]	87	Program test signal on pin B3 (TDIG1)
tmuxd2[7:4]	87	Program test signal on pin C3 (TDIG2)

A number of digital signals relating to the control channel can be mapped to two sensor pins, by programming the following values to register address 87.

Figure 64:
Digital Test Signals

tmuxd1[3:0] and tmuxd2[7:4] Value	TDIG1 and TDIG2 Signal
0	INTE1
1	INTE2
2	DVAL
3	LVAL
4	FVAL

7.7.2 Temperature Sensor

Figure 65:
Temperature Sensor Registers

Bit Name	Address	Description
temp[7:0]	88-89	Value of temperature sensor

The total value of the temperature sensor is written to two consecutive register addresses 88 and 89. To ensure a correct reading, these addresses must be read out in burst mode. In a typical application, the sensor's operating temperature is 10 °C to 15 °C higher than ambient temperature.

Calibration

A calibration of the temperature sensor is needed to read out correct temperature data. The temperature sensor requires a running input clock, the other functions of the image sensor can be operational or powered off. The output value of the temperature sensor also scales with the input clock frequency, so this parameter must be taken into account when calculating the temperature.

The calibration procedure consists of first reading out the temperature sensor at a known temperature (eg. ambient) and storing the value at this point. The device temperature can then be calculated with any new value, and an assumption of the temperature sensor sensitivity or slope.

7.7.3 Sensor ID

Figure 66:
Sensor ID Register

Bit Name	Address	Description
product_id[7:4]	90	8: CMV8000 SENSOR
rev_id[3:0]	90	1: First revision

This register can be used to identify the sensor type in the camera. Future versions of CMV8000 will have an incremented rev_id value.

7.7.4 Test Images

A built-in digital test image is available to. As this is digitally generated, consecutive frames should be identical. The test image is a repeating pattern of gradients that are 112 columns wide. The first gradient starts at value DB_OFFSET_MODE and increments 1 digital number for each column. The second gradient has the same evolution, but starts at DB_OFFSET_MODE+1, the third at DB_OFFSET_MODE+2 and so on.

As the value of the test pattern is entirely predictable, its mean value and standard deviation can be pre-calculated to check if it correctly received by the camera. Note that this is only valid for values of DB_OFFSET_DATA that do not clip pixel values to black or white, as this skews the standard deviation.

Equation 9:

$$\sigma_{ti} = 33.6229$$

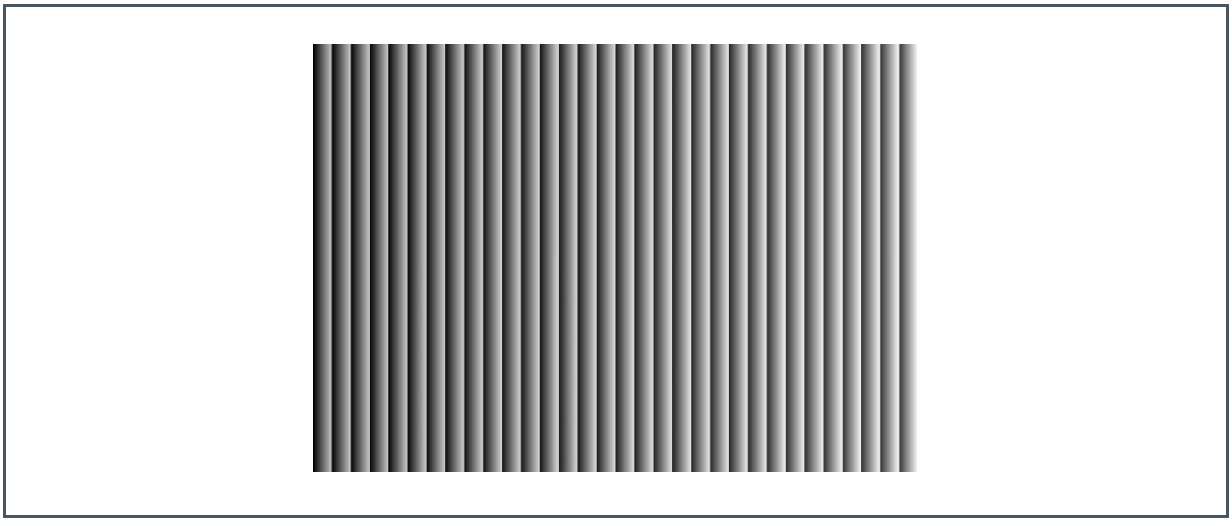
Equation 10:

$$\mu_{ti} = 71 + [DB\_OFFSET\_MODE]$$

Figure 67:
Test Image Registers

Bit Name	Address	Description
db_test_mode[1:0]	79	3: Enable test image
db_offset_data[12:0]	80 - 81	Set offset of test image

Figure 68:
CMV8000 Test Image



8 Register Description

8.1 Register Overview

Figure 69:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0	**<RESERVED>**	-	-	-	-	-	-	-	-
1	**YSIZE_TOT**	ysize_tot[7:0]							
2	**YSIZE_TOT**	ysize_tot[15:8]							
3	**YADDR_0**	yaddr_0[7:0]							
4	**YADDR_0**	yaddr_0[15:8]							
5	**YADDR_1**	yaddr_1[7:0]							
6	**YADDR_1**	yaddr_1[15:8]							
7	**YADDR_2**	yaddr_2[7:0]							
8	**YADDR_2**	yaddr_2[15:8]							
9	**YADDR_3**	yaddr_3[7:0]							
10	**YADDR_3**	yaddr_3[15:8]							
11	**YADDR_4**	yaddr_4[7:0]							
12	**YADDR_4**	yaddr_4[15:8]							
13	**YADDR_5**	yaddr_5[7:0]							
14	**YADDR_5**	yaddr_5[15:8]							
15	**YADDR_6**	yaddr_6[7:0]							
16	**YADDR_6**	yaddr_6[15:8]							
17	**YADDR_7**	yaddr_7[7:0]							
18	**YADDR_7**	yaddr_7[15:8]							
19	**YSIZE_0**	ysize_0[7:0]							
20	**YSIZE_0**	ysize_0[15:8]							
21	**YSIZE_1**	ysize_1[7:0]							
22	**YSIZE_1**	ysize_1[15:8]							
23	**YSIZE_2**	ysize_2[7:0]							
24	**YSIZE_2**	ysize_2[15:8]							
25	**YSIZE_3**	ysize_3[7:0]							
26	**YSIZE_3**	ysize_3[15:8]							
27	**YSIZE_4**	ysize_4[7:0]							
28	**YSIZE_4**	ysize_4[15:8]							
29	**YSIZE_5**	ysize_5[7:0]							
30	**YSIZE_5**	ysize_5[15:8]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
31	**YSIZE_6**	ysize_6[7:0]							
32	**YSIZE_6**	ysize_6[15:8]							
33	**YSIZE_7**	ysize_7[7:0]							
34	**YSIZE_7**	ysize_7[15:8]							
35	**YSKIP1**	yskip1[7:0]							
36	**YSKIP1**	yskip1[15:8]							
37	**YSKIP2**	yskip2[7:0]							
38	**YSKIP2**	yskip2[15:8]							
39	**MIRROR**							y[1]	x[0]
40	**INTE**						sync[2]	dual[1]	ext[0]
41	**EXP_LENGTH**	exp_length[7:0]							
42	**EXP_LENGTH**	exp_length[15:8]							
43	**EXP_LENGTH**	exp_length[23:16]							
44	**EXP_LENGTH2**	exp_length2[7:0]							
45	**EXP_LENGTH2**	exp_length2[15:8]							
46	**EXP_LENGTH2**	exp_length2[23:16]							
47	**SLOPES**							slopes[1:0]	
48	**EXP_K1**	exp_k1[7:0]							
49	**EXP_K1**	exp_k1[15:8]							
50	**EXP_K1**	exp_k1[23:16]							
51	**EXP_K2**	exp_k2[7:0]							
52	**EXP_K2**	exp_k2[15:8]							
53	**EXP_K2**	exp_k2[23:16]							
54	**FRAMES**	frames[7:0]							
55	**FRAMES**	frames[15:8]							
56	**LVDS_TRAIN**	lvds_train[7:0]							
57	**LVDS_TRAIN**					lvds_train[11:8]			
58	**DUMMY**	dummy[7:0]							
59	**MUX**				mux[4:0]				
60	**CHANNEL_EN**					channel_en[3:0]			
61	**SLOT_LENGTH**	slot_length[7:0]							
62	**ROW_LENGTH**		row_length[6:0]						
63	**<RESERVED>**								
64	**<RESERVED>**								
65	**SMP_LENGTH**	smp_length[7:0]							
66	**<RESERVED>**								
67	**<RESERVED>**								
68	**SMP_OPTIONS**				clamp_sig		pc_disable		
69	**<RESERVED>**								
70	**<RESERVED>**								

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
71	**ADC_RAMP_R_SIZE**	adc_ramp_r_size[7:0]							
72	**ADC_RAMP_R_SIZE**								adc_ramp_r_size[8]
73	**ADC_INTERVAL**	adc_interval[7:0]							
74	**ADC_RAMP_S_SIZE**	adc_ramp_size[7:0]							
75	**ADC_RAMP_S_SIZE**							adc_ramp_s_size[9:8]	
76	**ADC_OPTIONS**					no_ramp_ctrl			
77	**FOT_LENGTH**	fot_length[7:0]							
78	**FOT_OPTIONS**							adc_cal	amp_cal
79	**DB**							test_mode[1:0]	
80	**DB_OFFSET_DATA**	db_offset_data[7:0]							
81	**DB_OFFSET_DATA**					db_offset_data[11:8]			
82	**DB_DIG_GAIN**				db_dig_gain[4:0]				
83	**RESOLUTION**							lvds	adc
84	**CLK_OPTIONS**				div[4:0]				
85	**<RESERVED>**								
86	**<RESERVED>**								
87	**MONITOR**	tmuxd2[3:0]				tmuxd1[3:0]			
88	**TEMP_LO**	temp_lo[7:0]							
89	**TEMP_HI**	temp_hi[7:0]							
90	**REV_ID**	product_id				revision_id			
91	**V_PC**	v_pc[7:0]							
92	**V_PCHIGH**	v_pchigh[7:0]							
93	**<RESERVED>**								
94	**V_TGLOW1**		v_tglow1[6:0]						
95	**V_TGLOW2**		v_tglow2[6:0]						
96	**V_TGLOW3**		v_tglow3[6:0]						
97	**SLEW**	tg[3:0]				rst[3:0]			
98	**SLEW**	s2[3:0]				s1[3:0]			
99	**I_COL**					i_col[3:0]			
100	**<RESERVED>**								
101	**TMUXANA**					tmuxana[3:0]			
102	**I_LVDS**	rec[3:0]				driv[3:0]			
103	**V_CLAMP_RST**		v_clamp_rst[6:0]						
104	**<RESERVED>**								
105	**<RESERVED>**								
106	**I_ADC**					i_adc[3:0]			

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
107	**<RESERVED>**								
108	**<RESERVED>**								
109	**<RESERVED>**								
110	**<RESERVED>**								
111	**<RESERVED>**								
112	**<RESERVED>**								
113	**<RESERVED>**								
114	**<RESERVED>**								
115	**V_VRAMP_RES**		v_vramp_res[6:0]						
116	**V_VRAMP_SIG**		v_vramp_sig[6:0]						
117	**ADCRAMP**	tune[1:0]		adc_gain[5:0]					
118	**PGA_GAIN**					pga_gain[3:0]			
119	**<RESERVED>**								
120	**<RESERVED>**								
121	**ANA_ENABLE**				lvds_rec				mono
122	**<RESERVED>**								
123	**SPARE_1**								gate_clk
124	**<RESERVED>**								
125	**<RESERVED>**								
126	**<RESERVED>**								
127	**<RESERVED>**								

8.2 Detailed Register Description

8.2.1 YSIZE_TOT Register (Address 1-2)

Figure 70:
YSIZE_TOT Register

Address: 1-2		YSIZE_TOT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_tot	2528	DC	Set the total amount of rows in the frame

8.2.2 YADDR_0 Register (Address 3-4)

Figure 71:
YADDR_0 Register

Address: 3-4		YADDR_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_0	0	DC	Set the start address of window 0

8.2.3 YADDR_1 Register (Address 5-6)

Figure 72:
YADDR_1 Register

Addr: 5-6		YADDR_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_1	0	DC	Set the start address of window 1

8.2.4 YADDR_2 Register (Address 7-8)

Figure 73:
YADDR_2 Register

Addr: 7-8		YADDR_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_2	0	DC	Set the start address of window 2

8.2.5 YADDR_3 Register (Address 9-10)

Figure 74:
YADDR_3 Register

Addr: 9-10		YADDR_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_3	0	DC	Set the start address of window 3

8.2.6 YADDR_4 Register (Address 11-12)

Figure 75:
YADDR_4 Register

Addr: 11-12		YADDR_4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_4	0	DC	Set the start address of window 4

8.2.7 YADDR_5 Register (Address 13-14)

Figure 76:
YADDR_5 Register

Addr: 13-14		YADDR_5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_5	0	DC	Set the start address of window 5

8.2.8 YADDR_6 Register (Address 15-16)

Figure 77:
YADDR_6 Register

Addr: 15-16		YADDR_6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_6	0	DC	Set the start address of window 6

8.2.9 YADDR_7 Register (Address 17-18)

Figure 78:
YADDR_7 Register

Addr: 17-18		YADDR_7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yaddr_7	0	DC	Set the start address of window 7

8.2.10 YSIZE_0 Register (Address 19-20)

Figure 79:
YSIZE_0 Register

Addr: 19-20		YSIZE_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_0	0	DC	Set the amount of rows in window 0

8.2.11 YSIZE_1 Register (Address 21-22)

Figure 80:
YSIZE_1 Register

Addr: 21-22		YSIZE_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_1	0	DC	Set the amount of rows in window 1

8.2.12 YSIZE_2 Register (Address 23-24)

Figure 81:
YSIZE_2 Register

Addr: 23-24		YSIZE_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_2	0	DC	Set the amount of rows in window 2

8.2.13 YSIZE_3 Register (Address 25-26)

Figure 82:
YSIZE_3 Register

Addr: 25-26		YSIZE_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_3	0	DC	Set the amount of rows in window 3

8.2.14 YSIZE_4 Register (Address 27-28)

Figure 83:
YSIZE_4 Register

Addr: 27-28		YSIZE_4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_4	0	DC	Set the amount of rows in window 4

8.2.15 YSIZE_5 Register (Address 29-30)

Figure 84:
YSIZE_5 Register

Addr: 29-30		YSIZE_5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_5	0	DC	Set the amount of rows in window 5

8.2.16 YSIZE_6 Register (Address 31-32)

Figure 85:
YSIZE_6 Register

Addr: 31-32		YSIZE_6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_6	0	DC	Set the amount of rows in window 6

8.2.17 YSIZE_7 Register (Address 33-34)

Figure 86:
YSIZE_7 Register

Addr: 33-34		YSIZE_7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	ysize_7	0	DC	Set the amount of rows in window 7

8.2.18 YSKIP1 Register (Address 35-36)

Figure 87:
YSKIP1 Register

Addr: 35-36		YSKIP1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yskip1	0	DC	Set the amount of rows to skip in group 1

8.2.19 YSKIP2 Register (Address 37-38)

Figure 88:
YSKIP2 Register

Addr: 37-38		YSKIP2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	yskip2	0	DC	Set the amount of rows to skip in group 2

8.2.20 MIRROR Register (Address 39)

Figure 89:
MIRROR Register

Addr: 39		MIRROR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	x	0		Mirror in X-direction
[1]	y	0		Mirror in Y-direction

8.2.21 INTE Register (Address 40)

Figure 90:
INTE Register

Addr: 40		INTE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	ext	0		Set exposure mode to external
[1]	dual	0		0: Complete array has the same exposure time 1: Set exposure mode to HDR mode, odd and even rows integrate with group 1 and group 2 exposure times
[2]	sync	1		Synchronize start of integration and DVAL pulses

8.2.22 EXP_LENGTH Register (Address 41-43)

Figure 91:
EXP_LENGTH Register

Addr: 41-43		EXP_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[23:0]	exp_length	5056		Set the exposure length for group 1

8.2.23 EXP_LENGTH2 Register (Address 44-46)

Figure 92:
EXP_LENGTH2 Register

Addr: 44-46		EXP_LENGTH2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[23:0]	exp_length2	0		Set the exposure length for group 2

8.2.24 SLOPES Register (Address 47)

Figure 93:
SLOPES Register

Addr: 47		SLOPES		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	slopes	1		Sets the amount of slopes in the PWL HDR mode

8.2.25 EXP_K1 Register (Address 48-50)

Figure 94:
EXP_K1 Register

Addr: 48-50		EXP_K1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[23:0]	exp_k1	0		Sets the exposure time for kneepoint 1 in the PWL HDR mode

8.2.26 EXP_K2 Register (Address 51-53)

Figure 95:
EXP_K2 Register

Addr: 51-53		EXP_K2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[23:0]	exp_k2	0		Sets the exposure time for kneepoint 2 in the PWL HDR mode

8.2.27 FRAMES Register (Address 54-55)

Figure 96:
FRAMES Register

Addr: 54-55		FRAMES		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[15:0]	frames	1	DC	Sets the amount of frames to be sequenced following a single F_REQ pulse (internal exposure mode only)

8.2.28 LVDS_TRAIN Register (Address 56-57)

Figure 97:
LVDS_TRAIN Register

Addr: 56-57		LVDS_TRAIN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[11:0]	lvds_train	85		Sets the value of the training word

8.2.29 DUMMY Register (Address 58)

Figure 98:
DUMMY Register

Addr: 58		DUMMY		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	dummy	1		Sets the amount of dummy rows

8.2.30 MUX Register (Address 59)

Figure 99:
MUX Register

Addr: 59		MUX		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[4:0]	mux	1		Sets the multiplexing options on the LVDS channels

8.2.31 CHANNEL_EN Register (Address 60)

Figure 100:
CHANNEL_EN Register

Addr: 60		CHANNEL_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	channel_en	7		Sets the shutdown options on the LVDS channels

8.2.32 SLOT_LENGTH Register (Address 61)

Figure 101:
SLOT_LENGTH Register

Addr: 61		SLOT_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	slot_length	112		Sets the amount of clock cycles per slot (DVAL)

8.2.33 ROW_LENGTH Register (Address 62)

Figure 102:
ROW_LENGTH Register

Addr: 62		ROW_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	row_length	2		Sets the number of slots per row

8.2.34 SMP_LENGTH Register (Address 65)

Figure 103:
SMP_LENGTH Register

Addr: 65		SMP_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	smp_length	96		Sets the length of pixel sampling pulses

8.2.35 SMP_OPTIONS Register (Address 68)

Figure 104:
SMP_OPTIONS Register

Addr: 68		SMP_OPTIONS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[2]	pc_disable	0		Disables the column precharge pulse
[4]	clamp_sig	1		Sets the clamping level for the signal level

8.2.36 ADC_RAMP_R_SIZE Register (Address 71-72)

Figure 105:
ADC_RAMP_R_SIZE Register

Addr: 71-72		ADC_RAMP_R_SIZE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[8:0]	adc_ramp_r_size	41		Sets the size of the ADC reset ramp

8.2.37 ADC_INTERVAL Register (Address 73)

Figure 106:
ADC_INTERVAL Register

Addr: 73		ADC_INTERVAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	adc_interval	1		Sets the interval between signal and reset ADC ramps

8.2.38 ADC_RAMP_S_SIZE Register (Address 74-75)

Figure 107:
ADC_RAMP_S_SIZE Register

Addr: 74-75		ADC_RAMP_S_SIZE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[9:0]	adc_ramp_s_size	144		Sets the size of the ADC signal ramp

8.2.39 ADC_OPTIONS Register (Address 76)

Figure 108:
ADC_OPTIONS Register

Addr: 76		ADC_OPTIONS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3]	no_ramp_ctl	0		ADC test bit

8.2.40 FOT_LENGTH Register (Address 77)

Figure 109:
FOT_LENGTH Register

Addr: 77		FOT_LENGTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	fot_length	40		Sets the scaling factor for frame overhead time

8.2.41 FOT_OPTIONS Register (Address 78)

Figure 110:
FOT_OPTIONS Register

Addr: 78		FOT_OPTIONS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	amp_cal	0		Sets the amplifier calibration sequence
[1]	adc_cal	0		Sets the ADC calibration sequence

8.2.42 DB Register (Address 79)

Figure 111:
DB Register

Addr: 79		DB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[1:0]	test_mode	0		Sets the gradient test image

8.2.43 DB_OFFSET_DATA Register (Address 80-81)

Figure 112:
DB_OFFSET_DATA Register

Addr: 80-81		DB_OFFSET_DATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[11:0]	db_offset_data	444	DC	Sets the offset in the datablock, or image black level

8.2.44 DB_DIG_GAIN Register (Address 82)

Figure 113:
DB_DIG_GAIN Register

Addr: 82		DB_DIG_GAIN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[4:0]	db_dig_gain	4	DC	Sets the digital gain in datablock

8.2.45 RESOLUTION Register (Address 83)

Figure 114:
RESOLUTION Register

Addr: 83		RESOLUTION		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	adc	0		Not used
[1]	lvds	1		Sets the resolution of the LVDS data

8.2.46 CLK_OPTIONS Register (Address 84)

Figure 115:
CLK_OPTIONS Register

Addr: 84		CLK_OPTIONS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[4:0]	div	4		Sets the division factor between serial clock and pixel clock

8.2.47 MONITOR Register (Address 87)

Figure 116:
MONITOR Register

Addr: 87		MONITOR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	tmuxd1	0		Sets the test signal value on TDIG1 pin
[7:4]	tmuxd2	0		Sets the test signal value on TDIG2 pin

8.2.48 TEMP Register (Address 88-89)

Figure 117:
TEMP Register

Addr: 88-89		TEMP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	temp_lo	0	RO	Temperature sensor output, LSBs
[15:8]	temp_hi	0	RO	Temperature sensor output, MSBs

8.2.49 REV_ID Register (Address 90)

Figure 118:
REV_ID Register

Addr: 90		REV_ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:4]	product_id	8	RO	Shows the sensor product ID
[3:0]	rev_id	1	RO	Shows the sensor revision ID

8.2.50 V_PC Register (Address 91)

Figure 119:
V_PC Register

Addr: 91		V_PC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	v_pc	224		Sets the pixel pre-charge voltage

8.2.51 V_PCHIGH Register (Address 92)

Figure 120:
V_PCHIGH Register

Addr: 92		V_PCHIGH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[7:0]	v_pchigh	224		Sets the pixel pre-charge voltage during extra VPCHIGH pulse

8.2.52 V_TGLOW1 Register (Address 94)

Figure 121:
V_TGLOW1 Register

Addr: 94		V_TGLOW1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	v_tglow1	64		Sets the pixel transfer gate low voltage

8.2.53 V_TGLOW2 Register (Address 95)

Figure 122:
V_TGLOW2 Register

Addr: 95		V_TGLOW2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	v_tglow2	64		Sets the pixel transfer gate low voltage for slope 1 in PWL HDR mode

8.2.54 V_TGLOW3 Register (Address 96)

Figure 123:
V_TGLOW3 Register

Addr: 96		V_TGLOW3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	v_tglow3	64		Sets the pixel transfer gate low voltage for slope 2 in PWL HDR mode

8.2.55 SLEW Register (Address 97-98)

Figure 124:
SLEW Register

Addr: 97-98		SLEW		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	rst	8		Sets the slew current for pixel reset signal
[7:4]	tg	8		Sets the slew current for pixel transfer gate signal
[11:8]	s1	8		Sets the slew current for the pixel S1 signal
[15:12]	s2	8		Sets the slew current for the pixel S2 signal

8.2.56 I_COL Register (Address 99)

Figure 125:
I_COL Register

Addr: 99		I_COL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	i_col	11		Sets the column load current

8.2.57 TMUXANA Register (Address 101)

Figure 126:
TMUXANA Register

Addr: 101		TMUXANA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	tmuxana	0		Sets the analog test signal on the test output pin TMUX_ANA

8.2.58 I_LVDS Register (Address 102)

Figure 127:
I_LVDS Register

Addr: 102		I_LVDS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	driv	8		Sets the LVDS driver biasing current
[7:4]	rec	8		Sets the LVDS receiver biasing current

8.2.59 V_CLAMP_RST Register (Address 103)

Figure 128:
V_CLAMP_RST Register

Addr: 103		V_CLAMP_RST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	v_clamp_rst	84		Sets the clamp voltage for the reset signal

8.2.60 I_ADC Register (Address 106)

Figure 129:
I_ADC Register

Addr: 106		I_ADC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	i_adc	14		Sets the ADC biasing current

8.2.61 V_VRAMP_RES Register (Address 115)

Figure 130:
V_VRAMP_RES Register

Addr: 115		V_VRAMP_RES		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	v_vramp_res	94		Sets the start voltage for the reset ramp

8.2.62 V_VRAMP_SIG Register (Address 116)

Figure 131:
V_VRAMP_SIG Register

Addr: 116		V_VRAMP_SIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[6:0]	v_vramp_sig	94		Sets the start voltage for the signal ramp

8.2.63 ADCRAMP Register (Address 117)

Figure 132:
ADCRAMP Register

Addr: 117		ADCRAMP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[5:0]	adc_gain	32		Sets the ADC gain
[7:6]	tune	0		Tunes the ramp voltage to a different bit mode

8.2.64 PGA_GAIN Register (Address 118)

Figure 133:
PGA_GAIN Register

Addr: 118		PGA_GAIN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[3:0]	pga_gain	7	DC	Sets the column amplifier gain

8.2.65 ANA_ENABLE Register (Address 121)

Figure 134:
ANA_ENABLE Register

Addr: 121		ANA_ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	mono	1		Sets subsampling and HDR mode to monochrome mode – no Bayer pattern preservation
[4]	lvds_rec	1		Enables the LVDS receiver for IN_LCLK

8.2.66 SPARE_1 Register (Address 123)

Figure 135:
SPARE_1 Register

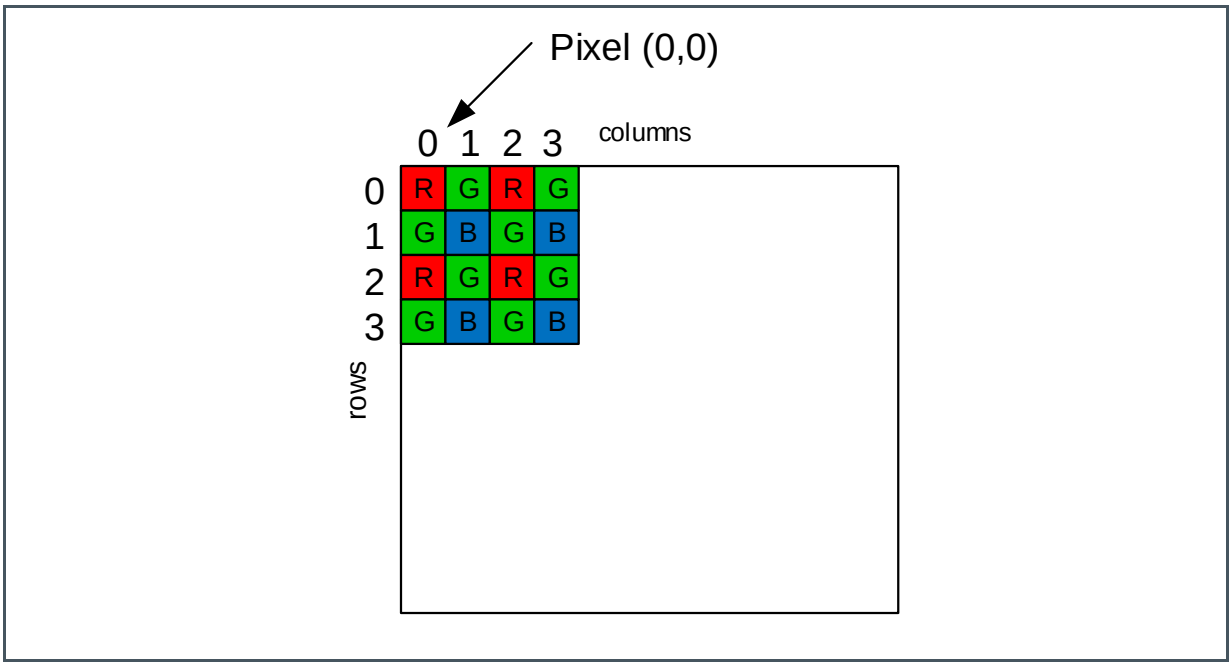
Addr: 123		SPARE_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
[0]	gate_clk	0		Sets the gating of the sensor parallel clock

9 Application Information

9.1 Color Filters

A color version of the CMV8000 is available that has a Bayer pattern applied to the pixels. The pixel on channel 1 which is available for read-out first, has the red filter applied.

Figure 136:
Bayer Pattern Layout



9.2 Socket

To avoid putting the sensor through the soldering heat (stressing the color filters and micro-lenses), it is advised to use a socket and place the sensor after the solder stage. Sockets for this device are available from Andon Electronics (www.andonelectronics.com). The following part numbers are available:

- Thru-hole: IS232-848107T-400T4-R27-L14
- SMD: IS232-848107T-414T4-R27-L14
- Rollerball®: IS232-848107T-RB501T4-R27-L14

For more information, contact Andon Electronics directly.

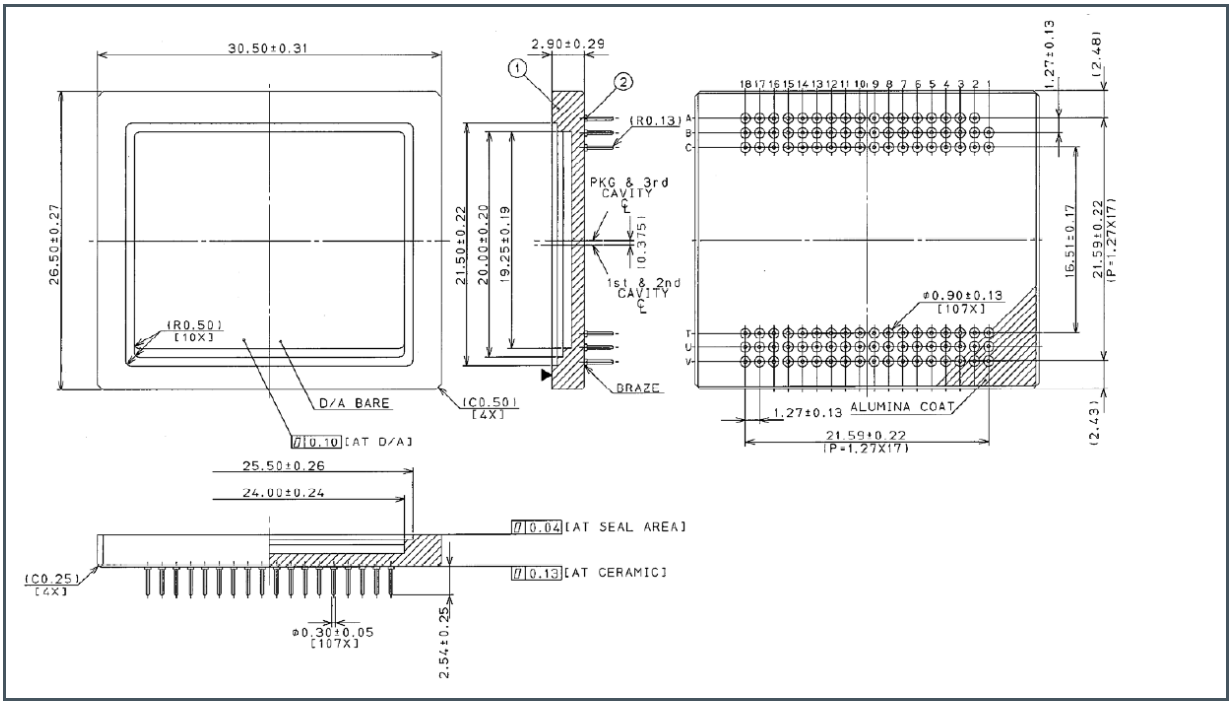
9.3 Pin Layout

Figure 137:
Pin Layout from Top View

top view	A	B	C		T	U	V
1		VDDPLL	VSS_PLL		IN_LCLK_P	IN_LCLK_N	VDD18
2	CMDN_ COL_LOAD	TDIG1	VSS33		OUT_CTR_N	OUT_CTR_P	MCLK
3	F_REQ	INT1	TDIG2		OUT1_N	OUT1_P	VSS18
4	SPI_IN	SPI_CLK	INT2		OUT3_N	OUT5_N	OUT5_P
5	SPI_OUT	SPI_ ENABLE	VSS33		OUT3_P	OUT7_N	OUT7_P
6	VDDPIX	VDD33	SYS_RESN		VSS18	VDD18	VSS33
7	CMDP	CMDP_INV	VDDPIX		OUT9_N	OUT11_N	OUT11_P
8	CMDN	VPC_H	VSS33		OUT9_P	OUT13_N	OUT13_P
9	VPC_L	T_ANA	VSS33		OUT19_N	OUT15_N	OUT15_P
10	VRST_H	VRST_L	VDDPIX		OUT19_P	OUT17_N	OUT17_P
11	VSS33	VDDPIX	VDD33		VSS18	VDD18	VDD33
12	VTF_LOW2	VTF_LOW1	VSS33		OUT21_N	OUT23_N	OUT23_P
13	CMDN_ COL_AMPL	VTF_LOW3	VSS33		OUT21_P	OUT25_N	OUT25_P
14	CMDN_ COL_PC	CMDN_ COL_LOAD	VDDPIX		OUT31_N	OUT27_N	OUT27_P
15	CMDN_ LVDS	CMDP_ RAMP	CMDP_ADC		OUT31_P	OUT29_N	OUT29_P
16	VBGAP	VREF	VPC_COMP		VSS18	VDD18	VSS18
17	DNC	VRAMP_ SIG	VRAMP_ RES		OUT_CLK_P	OUT_CLK_N	VDD18
18	VSS33	VSS33	VDD33		VDD18	VSS18	VSS18

10 Package Drawings & Markings

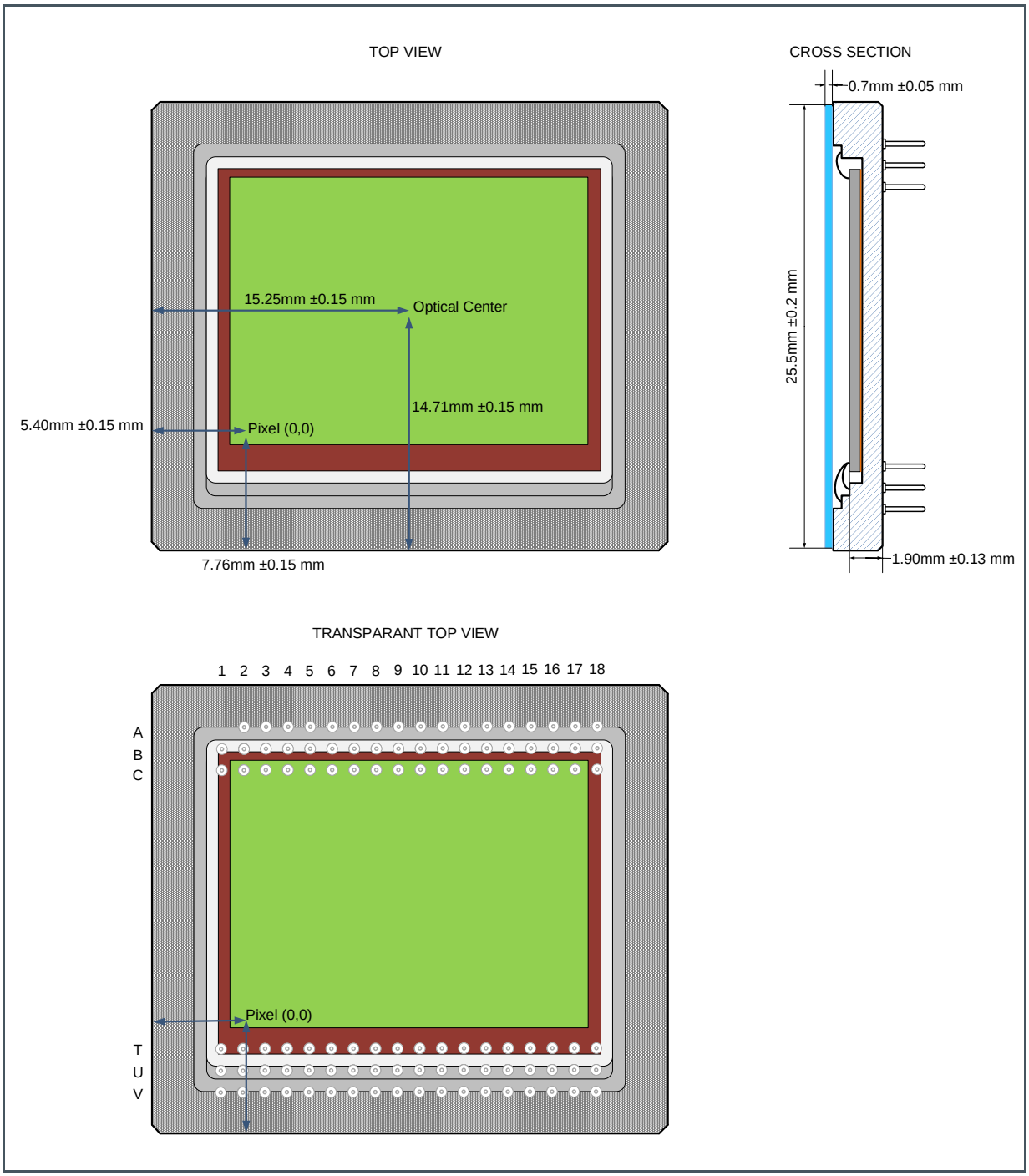
Figure 138:
CMV8000 Ceramic Package Drawing



Information

- All dimensions are in millimeter.
- Gold plate 0.76 min. over 2.0 µm min. nickel.
- Metallize by pin through plating, no tie bars.
- Unplated area on pin tip shall be less than 0.30 within 0.50 max from pin tip.
- NTK SPEC YA 1010 shall apply.
- No blisters on Au after 3 minutes (in air) at 350 °C as seen under 10x magnification.
- Excess Au plating on alumina coat is acceptable.

Figure 139:
CMV8000 Assembly Drawing



11 Soldering & Storage Information

Attention

Image sensors with color filter arrays and micro lenses are particularly sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the optical performance of the sensor.

A socket is the safest way to avoid any thermal stress. When not using a socket, we recommend to use manual hand soldering. Wave soldering can be used with precautions. Reflow soldering is not recommended.

Manual Soldering: Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350 °C with a 270 °C maximum pin temperature. Touch for a 2 seconds maximum duration per pin. Avoid touching and global heating of the ceramic package during soldering. Failure to do so may later device performance and reliability.

Wave Soldering: Wave solder dipping can cause damage to the glass and harm the imaging capability of the device. Avoid the solder to come in contact with the glass or ceramic body.

Figure 140:
Solder Reflow Profile Graph

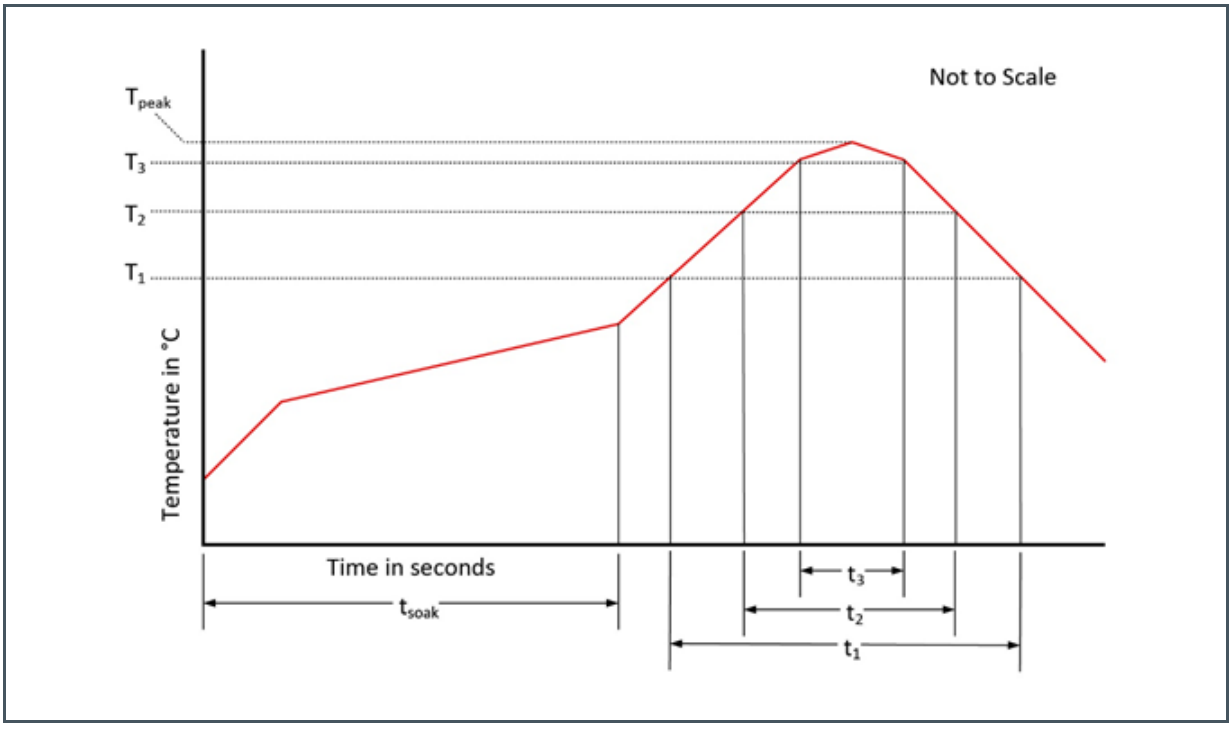


Figure 141:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	245 °C
Temperature gradient in cooling		Max -5 °C/s

12 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v1-00	Page
Corrected headings in the last few chapters	82
Added part numbers for the socket	82
Corrected max temperature during reflow soldering to 245°C	87

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

13 Legal Information

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For sales offices, distributors and representatives go to www.ams.com/Contact
For further information and requests, e-mail us at ams_sales@ams.com