DETAIL SPECIFICATION

ELMOS Part Nr :

910.01B

Contents

1 Project Summary

1.1 Purpose of Specification

The purpose of this specification is to define the mechanical, environmental and electrical characteristics for Application Specific integrated circuits supplied by ELMOS. All parts which comply with this specification shall be considered to meet the customers requirements. Any parameters which are left undefined will be processed in accordance with ELMOS´ standard Quality Control procedures.

This document is intended to take precedence of any applicable customer documents. When agreed by the customer and ELMOS, no changes or additions may be made without the written agreement of both the customer and ELMOS.

1.2 Life Support Policy/Product Liability

ELMOS products are not designed for use in Life Support Appliances, Devices or Systems where malfunction of an ELMOS product can be reasonably expected to result in personal injury. ELMOS customers using or selling ELMOS products for use in such applications do so at their own risk, and agree to full indemnify ELMOS for any damage resulting from such improper use or sale.

1.3 General Information

Elmos Project Name	:	910.01
Revision Status	:	B
Package Type	:	20PDIP / 20SOICW

1.4 Brief Functional Description

The IC E91001 is a 8-Way Power Driver (low side) with serial interface and interrogateable Output status.

The device incorporates the following features :

- Low standby current
- Serial structure for direct MPU interfacing
- Cascadable
- Interrogateable
- TTL- compatible input levels with hysteresis
- 8 high current outputs (R_{ON} typ. 1.5 Ω)
- Wide output operating voltage range
- Output open- and short-circuit protection
- Individual output short-circuit protection
- Thermal overstress protection

1.5 Related ELMOS Documents

QM-Nr:: 07PL0009.XX	Standard Qualification Plan
QM-Nr : 07SP0001.XX	Reliability Test Methods
QM-Nr : 07VA0013E.XX	Reliability Testing
QM-Nr : 07VA0005.XX	Finalpart Release for Shipment (Warenausgangsprüfung)
QM-Nr : 02SP0028.XX	Taping of Devices

1.6 Other Related Documents

None

1.7 Marking

Topside :

ELMOS
91001B
XXX# YWW *

Where :

91001B	Part Number
XXX	Lot Number
#	Assembler Code
YWW	Year and work week of assembly
*	Mask Revision status
Backside	None.

2 General Device Specification

2.1 Absolute Maximum Ratings (Non - operating)

Continuous operation of the device at or above these ratings is not permitted.

Absolute Maximum Ratings :				
Parameter	**Symbol**	**min**	**max**	**Unit**
Logic supply voltage	VDD	-0.3	7.0	V
Transient Output Voltage (Maximum 500 ms) (Maximum 500 µs)	VOUT VOUT	- -	40.0 50.0	V V
Output current	IOUT	-	350.0	mA
Output Current (Schaffner Pulses Type 2)	|IOUT P|		600.0	mA
Input Voltage	VIN	-0.3	VDD + 0.3	V
Power dissipation DIP 20 TA = 85 °C	P0	-	1000.0	mW
Power dissipation SO 20 TA = 85 °C	P0	-	800.0	mW
Thermal resistance DIL 20 (Junction to Ambient)	R_{ThJ-A}	-	65.0	K/W
Thermal resistance SO 20 (Junction to Ambient)	R_{ThJ-A}	-	80.0	K/W
Junction temperature	T_J	-	+ 150.0	°C
Operating temperature range	T_{OPT}	-40.0	+ 125.0	°C
Storage temperature	T_{STG}	-55.0	+ 150.0	°C

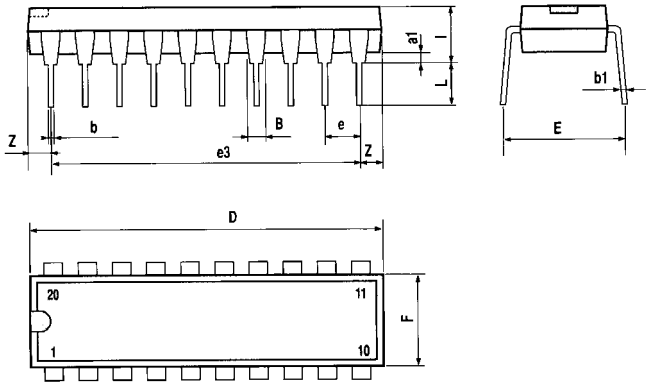
2.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated.

All of the following parameters are valid for an operating temperature range of -40°C up to 105°C (production test max limit is at 85°C), a supply voltage range of 4.5V < VDD < 5.5V, an output current IOUT ≤ 300mA and an output voltage range of 5.5V to 25V, unless otherwise specified.
Voltage reference is GND, if not otherwise specified.
The current values are positive, if flowing into the circuit.

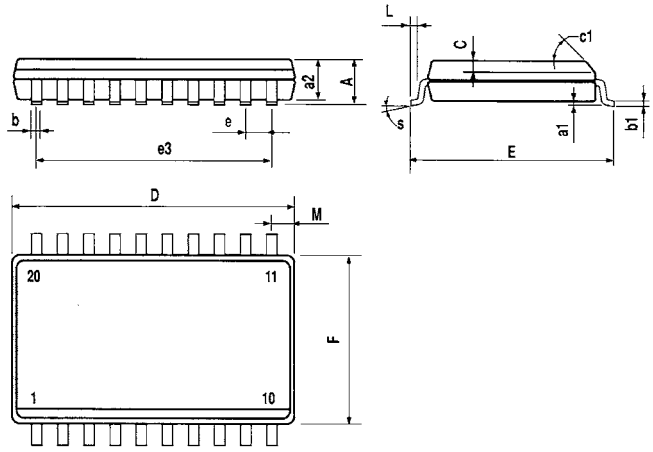
2.3 Package Outline

DIM	mm			inch		
	min	typ	max	min	typ	max
a1	.254			.010		
B	1.39		1.65	.055		.065
b		0.46			.018	
b1		0.25			.010	
D			25.40			1.00
E		8.5			.335	
e		2.54			.100	
e3		22.86			.900	
F			7.1			.280
I			3.93			.155
L		3.3			.130	
Z			1.34			.053



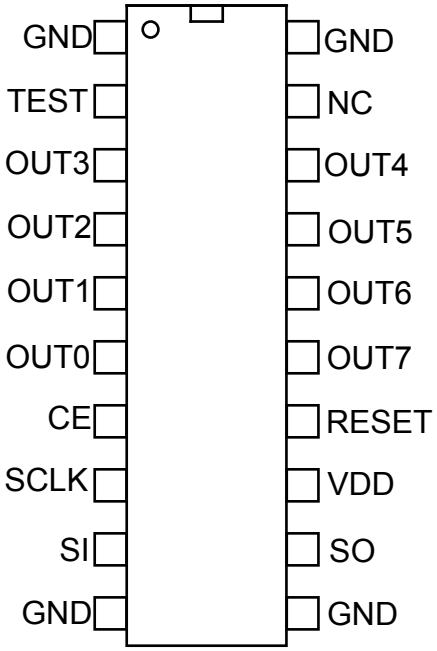
DIL 20 (300 mil JEDEC-STD)

DIM		mm		inch		
	min	typ	max	min	typ	max
a2			2.45			.096
b	0.35		0.49	.013		.019
b1	0.23		0.32	.009		.012
C		0.5			.020	
c1			45°	typ		
D	12.6		13.0	.496		.512
E	10.0		10.65	.393		.419
e		1.27			.050	
e3		11.43			.450	
F	7.4		7.6	.291		.300
G	8.8		9.15	.346		.360
L	0.5		1.27	.019		.050
M			0.75			.029

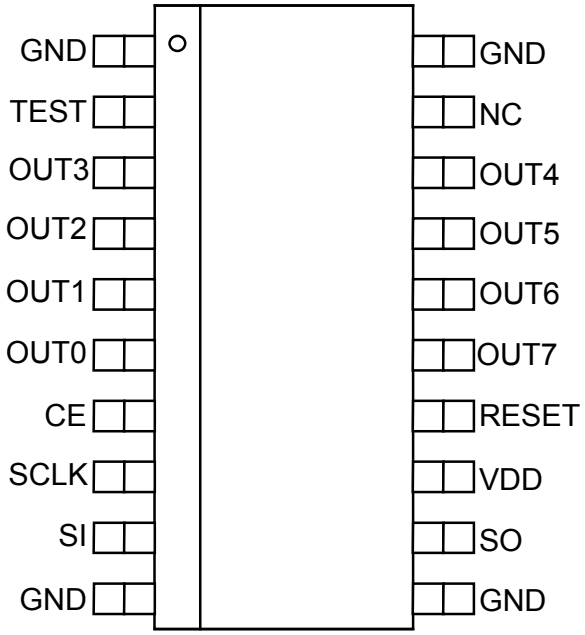


SO 20 (300 mil JEDEC-STD)

2.4 Package Pin-Out



DIL 20



SO 20

2.5 Package Pin Definition

VDD	Power Supply Voltage
GND	Ground
OUT_{0-7}	Open-Drain Low-Side Driver
SI	Serial Data Input
SO	Serial Data Output (High impedance when CE = High)
SCLK	Serial Data Input/Output Clock. (Data are clocked by the falling edge of the pulse.)
CE	Chip Enable - Active LOW. (Output Data is read back on the falling edge of the pulse, and only after 8 x n falling edges on SCLK is the output data clocked on the next rising edge.)
RESET	External Reset - Active LOW, or'd with internal Power On Reset.
TEST	Test Mode Enable - Active HIGH > 3V : Test Mode 1 > 16V : Test Mode 2

3 Detailed Electrical Description

3.1 Characteristics

3.1.1 DC Characteristics

Ref.Nr.	Parameter	Symbol	Condition	min	typ	max	Unit
1	Power Supply Current	I_{VDD}		-	-	2.0	mA
2	Power Supply Current (Sleep Mode)	I_{VDD}	VOUTX > 1.0V	-	<1.0	5.0	µA
3	Power On Reset Threshold	POR_{on}	VDD: 0V --> 5V **3)**	-	-	3.6	V
4	Thermal Cut-off Threshold	T_{HSoff}	$T_J > T_{HS}$ **2) 3)**	150.0	165.0	185.0	°C
5	Thermal Cut-off Reset Threshold	T_{HSon}	$T_J > T_{HS}$ **2) 3)**	125.0	140.0	155.0	°C
6	Thermal Surveillance Hysteresis	T_{HShys}	**3)**	20.0	40.0	60.0	°C

3.1.1.1 Input Characteristics

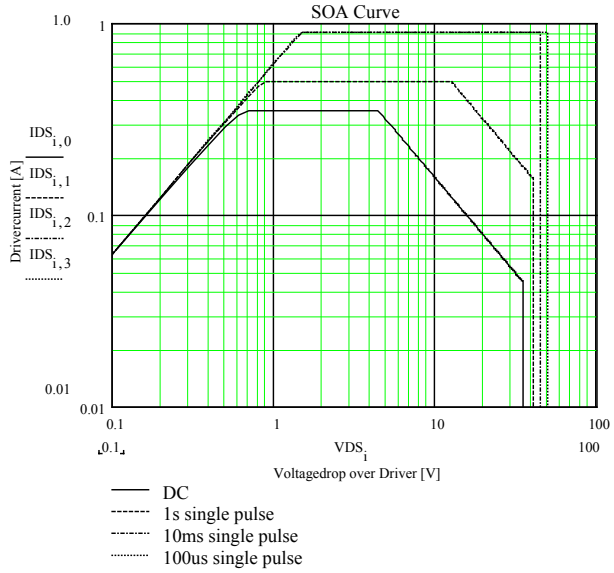
Ref. Nr.	Pin	LOW-Level		HIGH-Level		Hysteresis **3)**		Pull up		Pull down	
		min	max	min	max	min	max	min	max	min	max
1	SI	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	1.0µA		1.0µA
2	SCLK	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	1.0µA		1.0µA
3	CE	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-	1.0µA		1.0µA
4	RESET	-0.3V	0.3VDD	0.75VDD	VDD+0.3V	0.9V	1.7V	-		10.0µA	50.0µA
5	TEST	-0.3V	0.3VDD	0.75VDD	8V **4)**	-	-	-	-	10.0µA	50.0µA
6				16V	17V **5)**	-	-				
7	OUTx	-0.3V	2.5V	3.5V	V_{OUT}	-	-	-	-	30.0µA	90.0µA

3.1.1.2 Output Characteristics

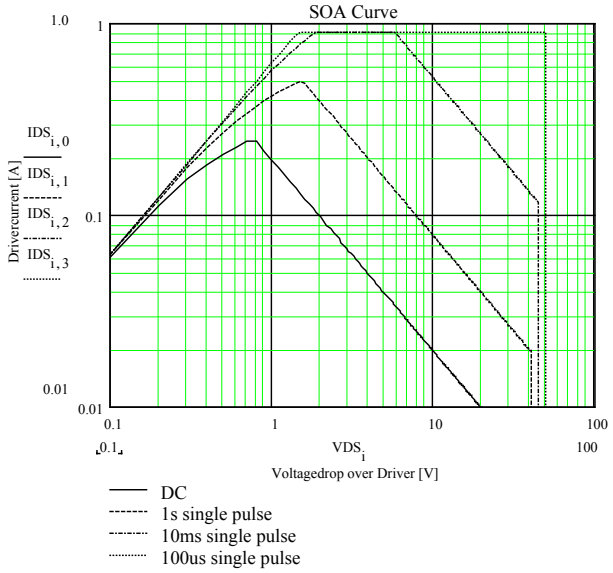
Ref.Nr.	Pin	Parameter	Symbol	Condition	min	typ	max	Unit
1	SO	LOW Level Output Voltage	V_{SOL}	I_{SO} = 1.6mA	-	-	0.4	V
2		HIGH Level Output Voltage	V_{SOH}	I_{SO} = -1.0mA	V_{DD} -1,3V	-	V_{DD}	V
3		Tristate-Leakage Current	I_{SOtri}	$0 \le V_{SO} \le V_{DD}$	-5.0	-	5.0	µA
4	OUTx	Short Circuit Output Current	I_{SC}	VOUTX = 3V T_{SCL}=20 ms	0.35	0.6	0.9	A
5		Output Voltage Limit	V_{OUTx}	OUT=HIGH	36.0	-	50.0	V
6		Output Resistance	R_{OUT}	Out = LOW, $0<I_{OUT}<200$ mA	-	1.5	3.0	Ω
7		Residual Output Current	I_{OUTLx}	Out=HIGH	0	1.0	10.0	µA

3.1.2 Safe Operating Area of OUTx

Only one driver active (T=25°C):



All drivers active (T=25°C):

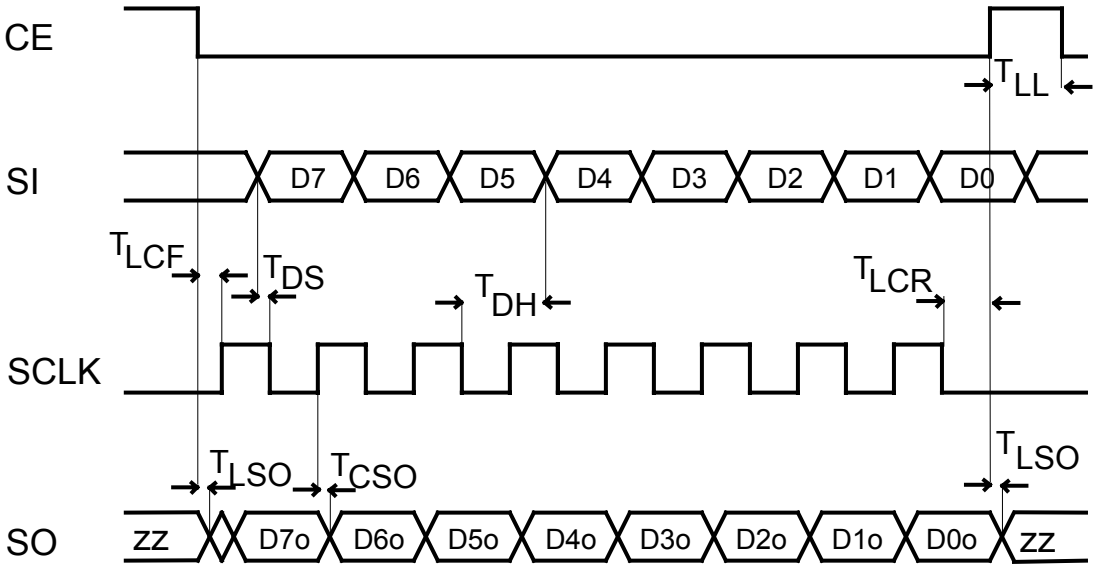


3.1.3 AC Characteristics

Ref.Nr.	Pin	Parameter	Symbol	Condition	min	typ	max	Unit
1	SCLK SI RESET CE TEST	Input capacitance		3)			5	pF
2	SO	Output marginal delay		3)			0.5	ns/pF
3	RESET	RESET Pulse Width	t_{RESon}	RESET -> L	0.31	0.62	0.93	ms
4	OUTx	Rate of Change of Output Voltage	dV_{OUT}/dt	R_L = 1kΩ 3)	-	10.0	-	V/µs
5		Output Capacitance	C_{OUT}	Out=HIGH, V_{OUT}= 5V 3)	-	40.0	60.0	pF
6				Out=HIGH, V_{OUT}=15V 3)	-	30.0	45.0	pF
7		Duration of Output Short Circuit Limit	T_{SCL}	$I_{OUT}>I_{SCL}$ 1)	18.5	37.0	55.5	ms
8		Propagation Delay Time CE --> OUTx	t_N	see Fig.4 R_L = 1kΩ 3)	-	10.0	20.0	µs
9	SCLK	Clock frequency	f_{SCLK}	3)			2	MHz

3.1.3.1 Interface Timing

Symbol	Parameter	min 3)	max 3)	Unit
T_{LSO}	Time between falling edge (10%) or rising edge (90%) of the CE signal and active (90%) or high impedance state of the SO output. Load capacitance at SO < 20pF.	20	100	ns
T_{LCF}	Time between falling edge (10%) of the CE signal and the first rising edge (10%) of the SCLK clock.	150		ns
T_{CSO}	Time between rising edge (10%) of the SCLK clock and the new data at SO output (10% or 90%). Load capacitance at SO <20pF.	10	60	ns
T_{DS}	Time between stable data at SI (90% or 10%) and falling edge at SCLK (90%) to clock the data in: Data setup time.	40		ns
T_{DH}	Time between falling edge at SCLK (90%) and changing of the data at SI (10% or 90%): Data hold time	20		ns
T_{LL}	Time between two load cycles: CE at high level (90%).	150		ns
T_{LCR}	Time between falling edge of SCLK (90%) and rising edge of CE (90%) signal.	20		ns



Notes:

1) When the output current exceeds the value of I_{SCL} an internal timer is initiated and the current limit is activated. If the current limit is still active after the time T_{SCL} the individual output is disabled by resetting the input latch.

2) As long as the thermal cut-off threshold TH_S is exceeded, all output drivers are in a high impedance condition. The contents of the latch are unaffected.

3) Not tested in production.

4) Test Mode 1

5) Test Mode 2

4 Functional Description

4.1 Block Diagram

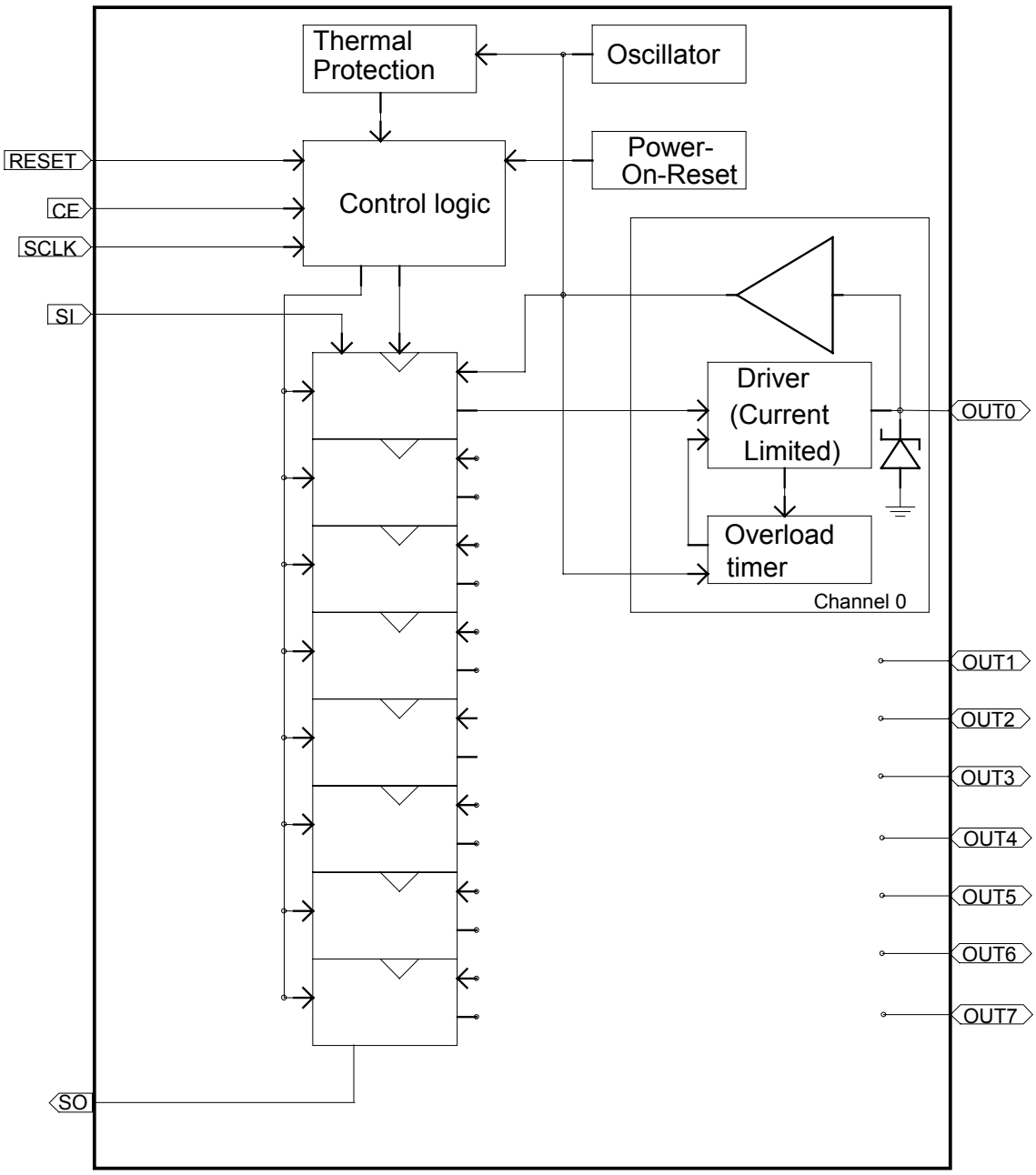


Figure 4.1-1

4.2 Detailed Functional Description

This IC was specially developed for Automobile applications. Application areas include driving relays, Lamps, bus systems etc. with medium power consumption. The 910.01 comprises a serial data bus and 8 identical power drivers. All outputs are short circuit protected, and a thermal cut-off protects the devices from thermal overstress.

By means of the RESET signal (RESET=Low) the IC can be switched into a low current consumption mode (Sleep Mode). In this mode all current consumption is disabled.

There are two possible data transfer protocols:

a) Parallel data input (see Figure 4.2-1 and Figure 4.5-1)

SI and SO are tied together and the device is activated by means of the chip enable (CE) line. On the falling edge of the CE signal the data is loaded into the shift register and SO goes to the low impedance state. With each rising edge of SCLK the data beginning with Bit 7 (D7) is clocked out at SO and with each falling edge new data is clocked from SI. On the rising edge of CE the data from the shift register is clocked through to the outputs. SO goes to the high impedance state (Tri-State as long as CE remains inactive HIGH). A LOW level on the input produces a LOW level on the open drain driver which switches to the low impedance state.

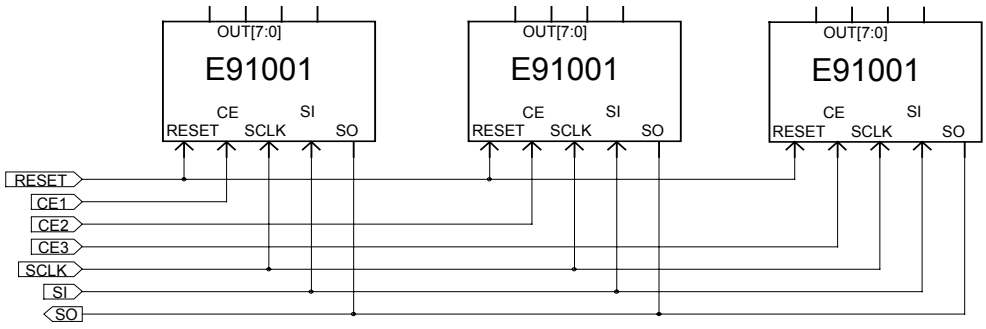


Figure 4.2-1

b) Serial data input (see Figure 4.2-2 and Figure 4.4-1)

The complete Daisy Chain of drivers are enabled in parallel by CE and clocked out by SCLK. On the falling edge of CE the status of each output is clocked into the shift register. On each rising edge of SCLK data is clocked out of SO, and with each falling edge of SCLK new data is clocked into SI. After 8 x n clock cycles new data has been read in and existing data clocked out. On the rising edge of CE new data is clocked through to the outputs. SO goes to the high impedance state (Tri-state as long as CE remains inactive HIGH). A LOW level on the input produces a LOW level on the open drain driver which switches to the low impedance state.

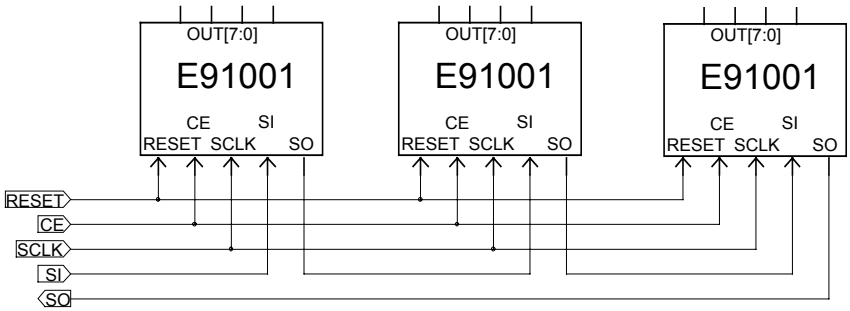


Figure 4.2-2

4.3 Protection Functions

In addition to the Power on reset function the IC incorporates three other protection functions; over temperature protection, short-circuit protection and open output recognition. No special failure status bit is provided for indicating failures since this information is not available on the 8 bit interface.

Power-On-Reset: After the application of the supply voltage all data latches and the timer are reset, and the outputs are disabled (inactive HIGH). The internal Power On Reset is OR'd with the external RESET input. In the RESET Mode the serial data output SO is inactive (LOW), as long as CE is active (LOW). Whereas SO goes into the high impedance Tri-State, if CE is inactive (HIGH). The external RESET is only invoked, if the pulse width exceeds the time t_{RESon}.(see Figure 4.5-2)

Short Circuit Protection: If the voltage drop across the output driver exceeds the short circuit threshold of 1V (R_{DSON} ca. 1,5Ω), the current limit is activated and after approximately 40ms, the output is disabled. After disabling the output, the short circuit memory is cleared and it is possible to re-activate the outputs by writing LOW bits into the shift register via the serial data input SI. In the event that a short circuit is still present the current limit is again activated and the output is again disabled after 40 ms.

After output disable due to the presence of a short circuit (OUTx = inactive HIGH) the serial output SO goes to a HIGH level, since SO always indicates the actual output status. Interrogating the SO status is the only way of establishing if a short circuit exists. When the output OUTx is selected by a LOW level on the SI serial data input (output OUTx enabled) and a HIGH level appears on the data output SO the presence of a short circuit on the enabled output is clear.

At switch on the output is operated as a constant current source by the internal limiting. When used with lamps they may be safely switched on because the internal limit operates for approximately 40 ms and disables the outputs. (see Figure 4.5-4)

Open Output Recognition: In the event of an open output the output voltage of OUTx is set to definite LOW level by the pull down transistor (OUTx = LOW). A LOW level also appears at the data output SO:

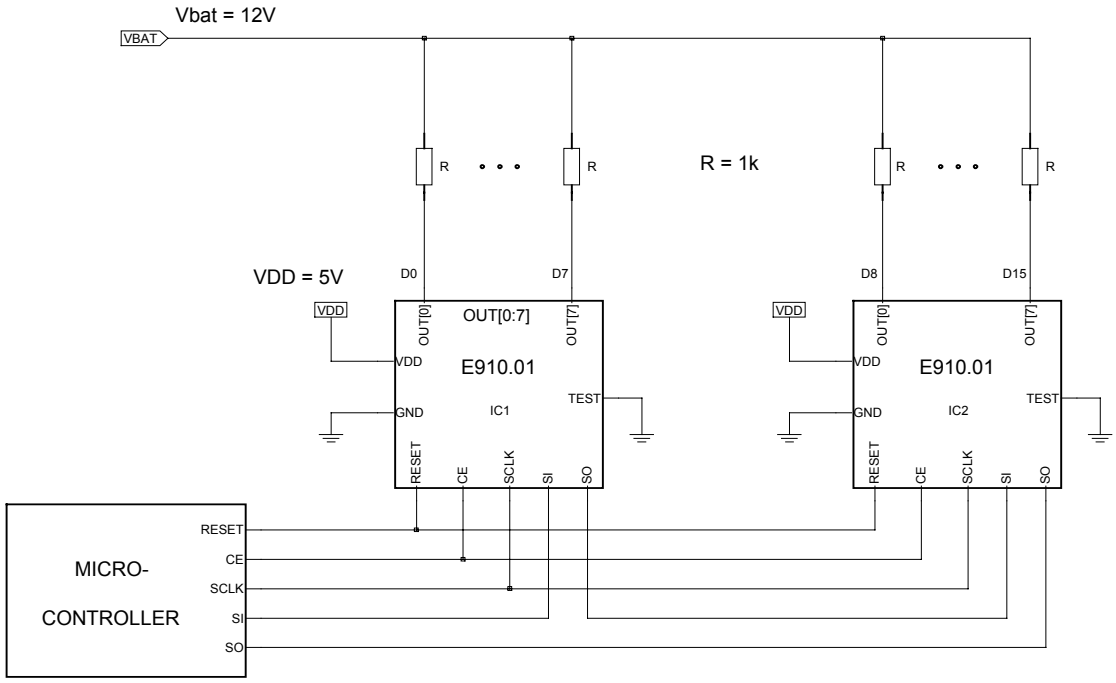
The actual method of establishing that an output is open is by interrogating the state of the data output SO. When an output OUTx is selected by means of a HIGH level on the SI pin (output OUTx disabled) a LOW level appears on the SO pin. Thus the open condition of the output is indicated. This function is the inverse of the short circuit condition above.

Over temperature Protection: If the chip temperature exceeds the protection threshold of typically 165°C all output drivers are disabled and the data stored in the latches are retained. When the temperature drops below the protection threshold of typically 140°C the previously stored condition is restored providing *no new* data have been loaded into the shift register by SI during this protection condition otherwise the stored data is overridden. This is also the case, when a RESET signal is received or when a falling edge on CE causes the shift register to be read. (see Figure 4.5-3)

The actual method of establishing that the device is in thermal protection shut down is by interrogating the state of the data output SO. When an output OUTx is selected by means of a LOW level on the SI pin (output OUTx enabled) a HIGH level appears on the SO pin for all outputs. Thus the thermal shutdown condition is indicated. It is highly unlikely that a short circuit condition can occur in all outputs simultaneously.

Test Modes:
If a voltage of greater than 3V and lower than 8V is applied to the TEST input, the device will switch into the Test Mode 1. In this mode the counter chain following the internal RC oscillator is shortened. The oscillator signal (divided by 2) appears on the output SO.
Test mode 2: If the voltage at the TEST input is greater than 16V additionally the over temperature protection circuit is set between 25°C and 85°C.

4.4 Application Circuit



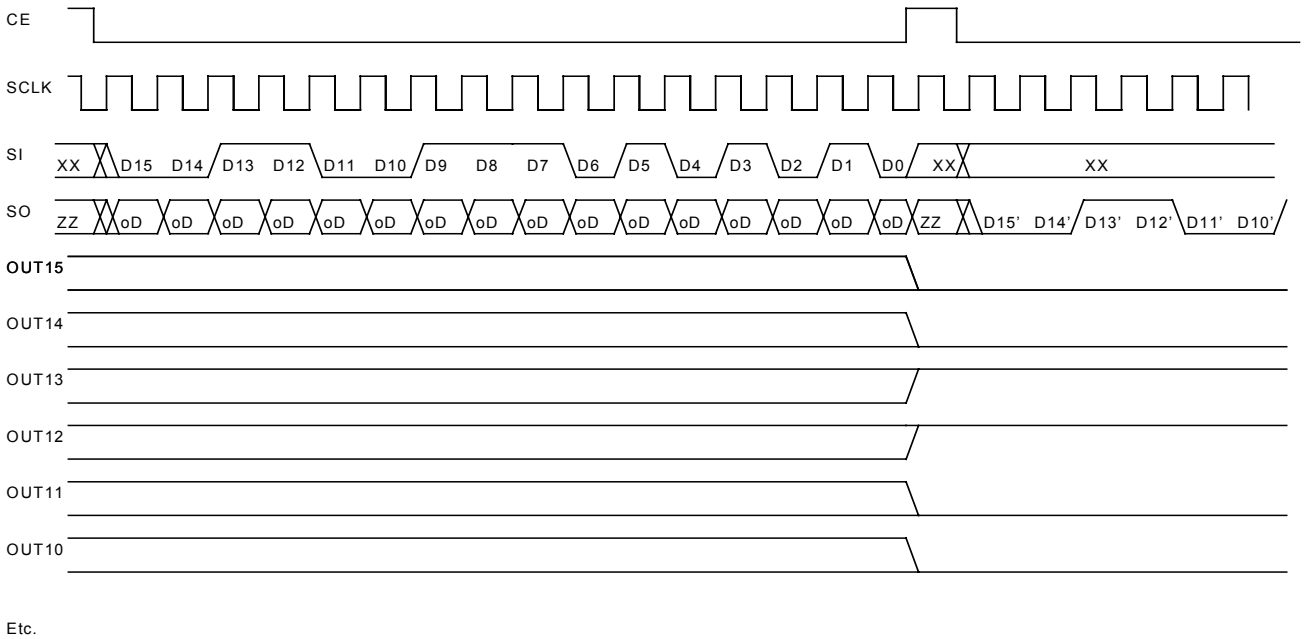


Figure 4.4-1

4.5 Timing Diagram

4.5.1 Operating Mode

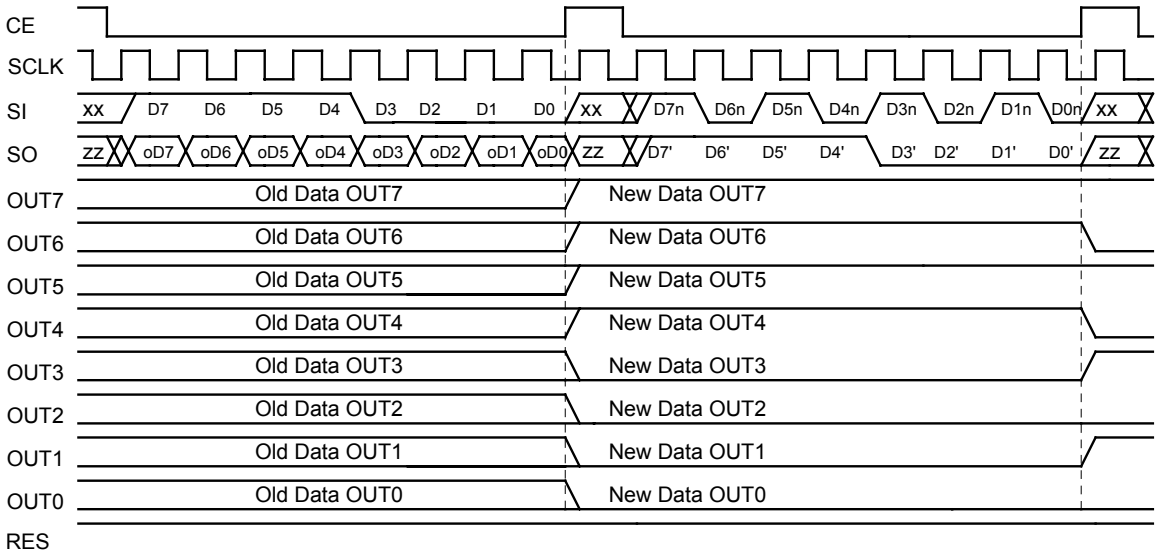


Figure 4.5-1

4.5.2 RESET Mode (Sleep Mode)

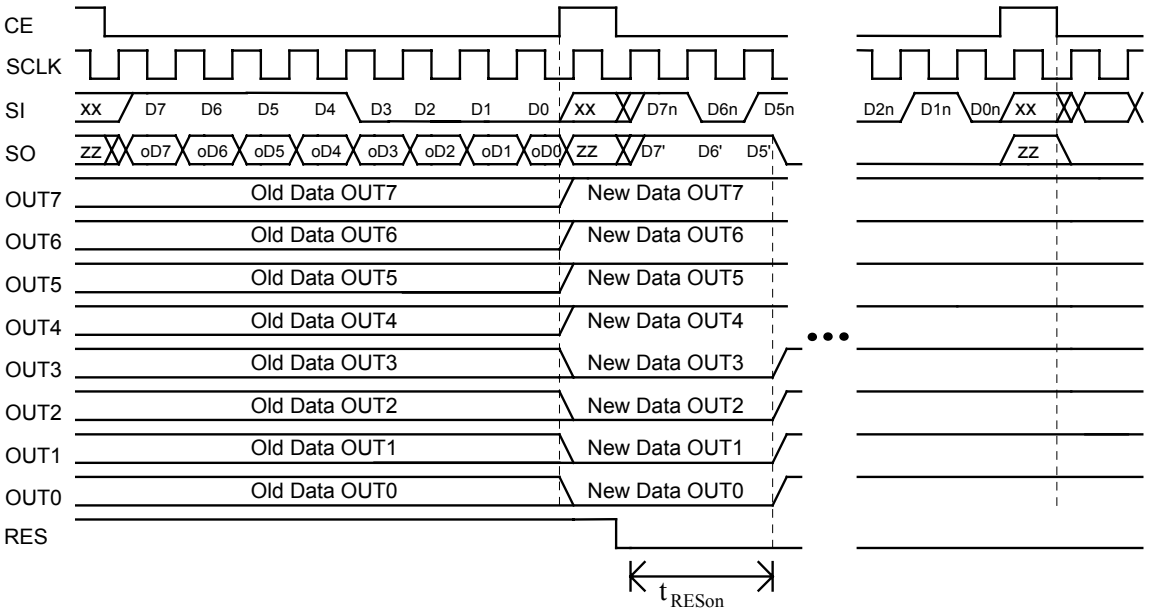


Figure 4.5-2

4.5.3 Thermal Cut-off

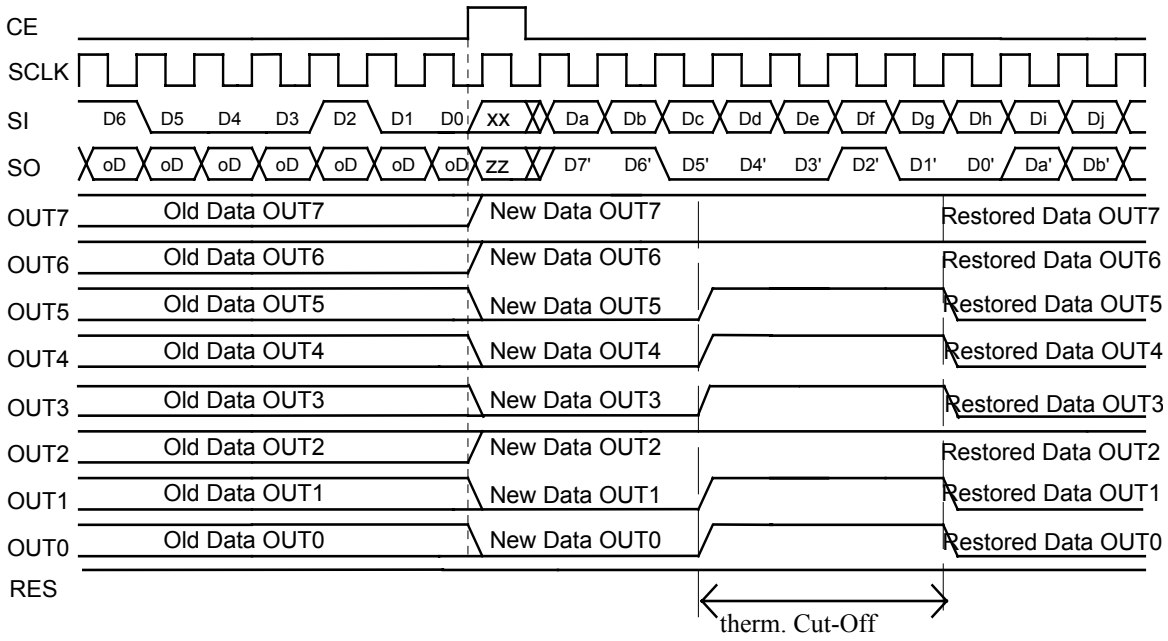


Figure 4.5-3

4.5.4 Short Circuit Condition

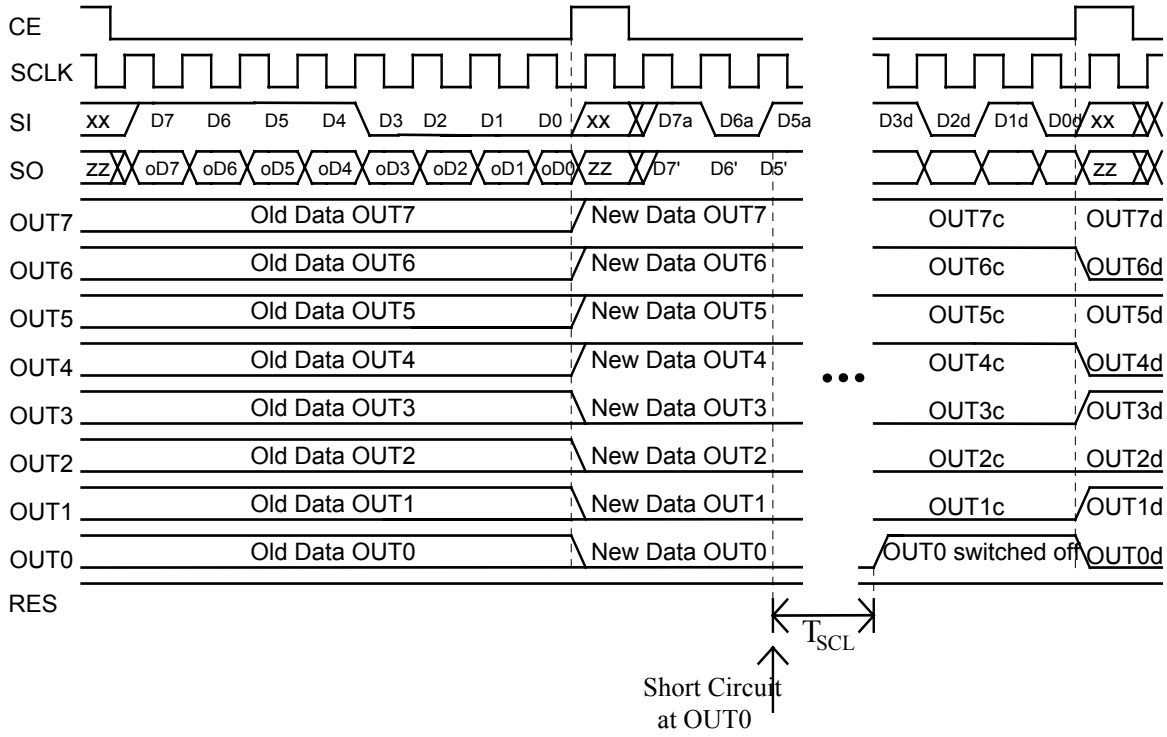


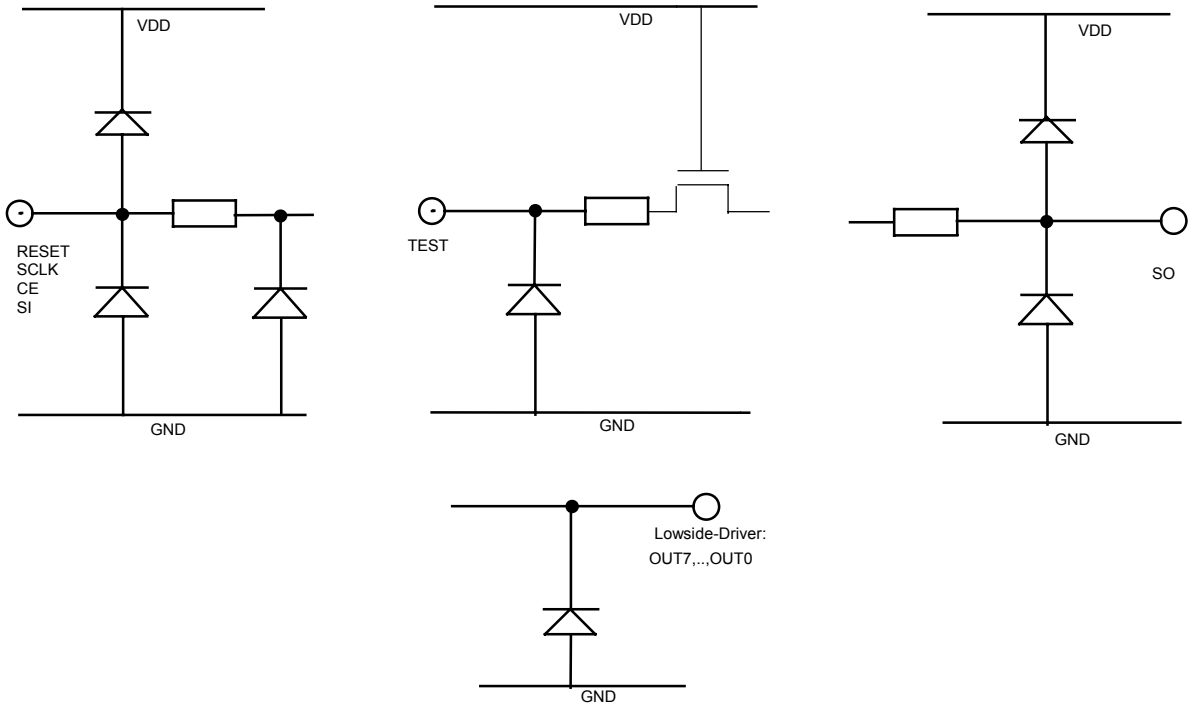
Figure 4.5-4

4.6 Noise Immunity

The 910.01 device meets the following requirements of DIN 40 839 part 1, when used in an application according to this specification :

Parameter	Condition	
Test pulse 1	t_1 = 5s / U_S = -100V	100 pulses
Test pulse 2	t_1 = 0,5s / U_S = 100V	1000 pulses
Test pulse 3a/b	DIN 40 839 Part 3 U_S = -150V / U_S = 100V	1000 Bursts
Test pulse 4	U_s =-6V U_a =-5V t_8 = 5s	10 pulses
Test pulse 5	R_i = 2_ t_D = 250ms t_r = 0,1ms U_P+U_S= 40V	10 pulses at 1 minute intervals

4.7 ESD Protection Circuit

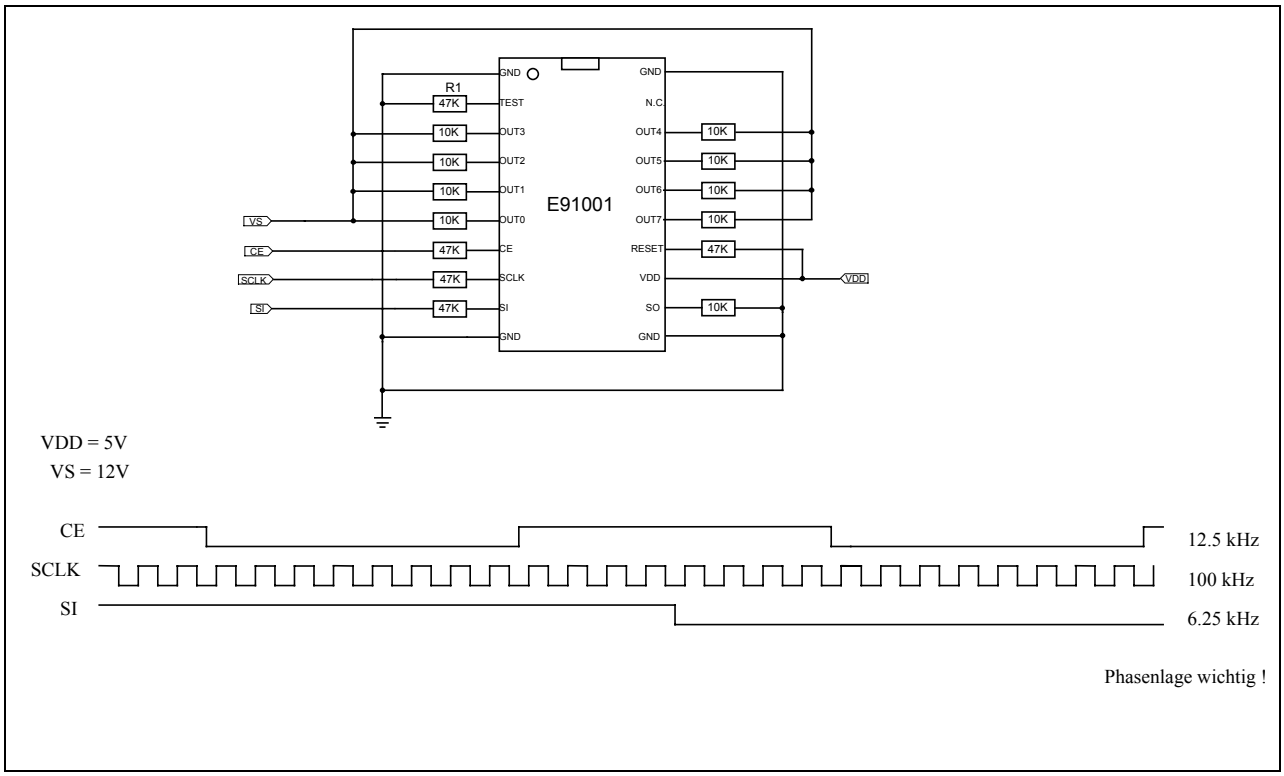


4.7.1 Test Method

The ESD Protection circuitry is measured using MIL-STD-883C Method 3015 (Human Body Model) with the following conditions :

VIN = 2000 Volt
REXT = 1500 Ohm
CEXT = 100 pF

5 Life Test Circuit



Life Test conditions

Temperature	:	125 °C
Condition	:	Dynamic

6 Record of Revisions

CHAPTER		REASON FOR AND DESCRIPTION OF CHANGE	DATE	APPROVAL	
	REV			ELMOS	CUST
	00	New format, B version	20.04.99	LK	
	00	Safe operating area	20.04.99	LK	
	00	Interface Timing	20.04.99	LK	
	00	In/Output Capacitance	20.04.99	LK	
	00	Introduction of Test mode 2	20.04.99	LK	
	00	Correction of timing diagram for application	21.04.99	JoF	
	00	..Parameters numbered	07.07.99	JoF	
1.5	01	Update of related ELMOS documents	23.09.03	JoF	
2.2	01	Recommended Operating Conditions: max limit changed from 85°C to 105°C plus remark for production test.	11.09.03	JoF	
2.2	01	Recommended Operating Conditions: output current Iout $\leq$ 300mA	11.09.03	JoF	
3.1.1.2	01	Ref. Nr. 6: condition updated (Iout < 200mA limit has been erased because of chap. 2.2)	11.09.03	JoF	
3.1.3	01	Ref. Nr. 4; condition updated RL=1kΩ	11.09.03	JoF	
3.1.3	01	Ref. Nr. 9 added: max. fSCLK=2MHz	11.09.03	JoF	
5-8	01	Update/Erase of chapters 5-7	23.09.03	JoF/FPe	