TTL
MSI

# TYPES SN54LS168A SN54LS169A, SN54S168, SN54S169, SN74LS168A, SN74LS169A, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

BULLETIN NO. DL-S 7712068, OCTOBER 1976—REVISED AUGUST 1977

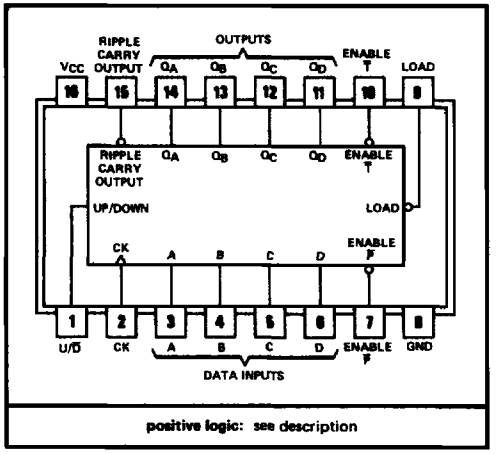
## 'LS168A, 'S168 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
## 'LS169A, 'S169 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

**Programmable Look-Ahead Up/Down Binary/Decade Counters**

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**

| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY | | TYPICAL POWER DISSIPATION |
|---|---|---|---|
| | COUNTING UP | COUNTING DOWN | |
| 'LS168A, 'LS169A | 35 MHz | 35 MHz | 100 mW |
| 'S168, 'S169 | 70 MHz | 55 MHz | 500 mW |

SERIES SN54LS', SN54S' . . . J OR W PACKAGE
SERIES SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see description

## description

*These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting* applications. The 'LS168A and 'S168 are decade counters and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the $Q_A$ output when counting up and approximately equal to the low portion of the $Q_A$ output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

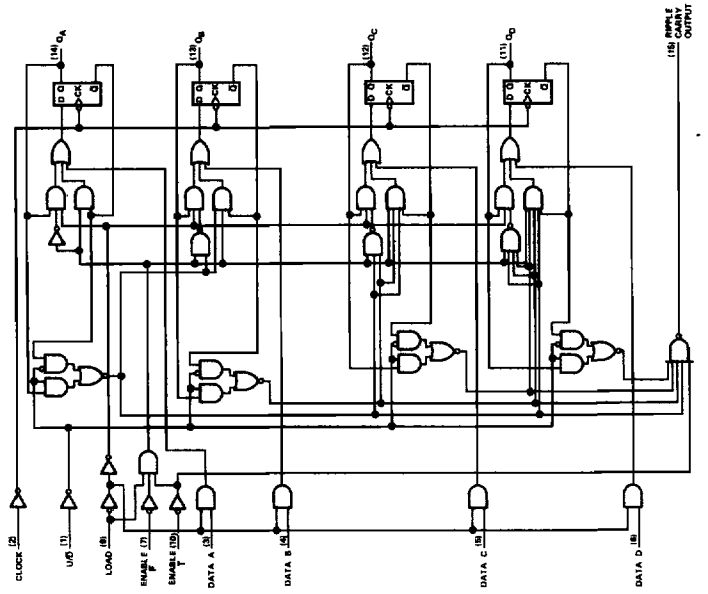
The 'LS168A and 'LS169A are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time and reduced input currents $I_{IH}$ and $I_{IL}$.



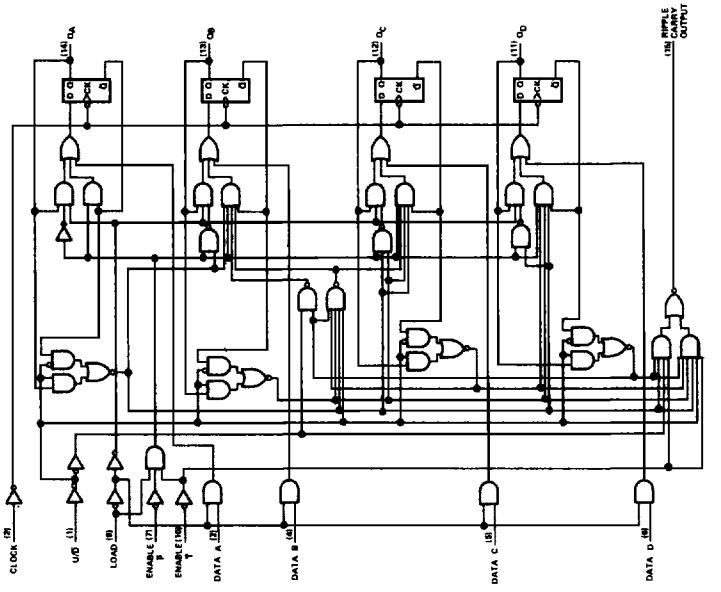
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## functional block diagrams

SN54LS169A, SN74LS169A, BINARY COUNTERS

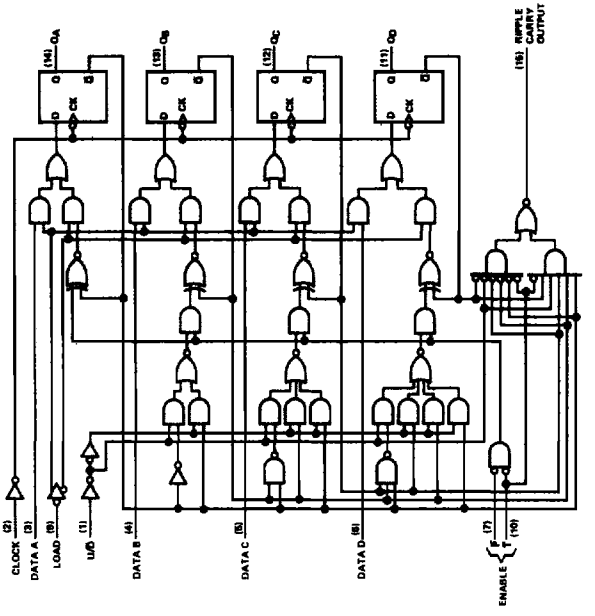



SN54LS168A, SN74LS168A, DECADE COUNTERS

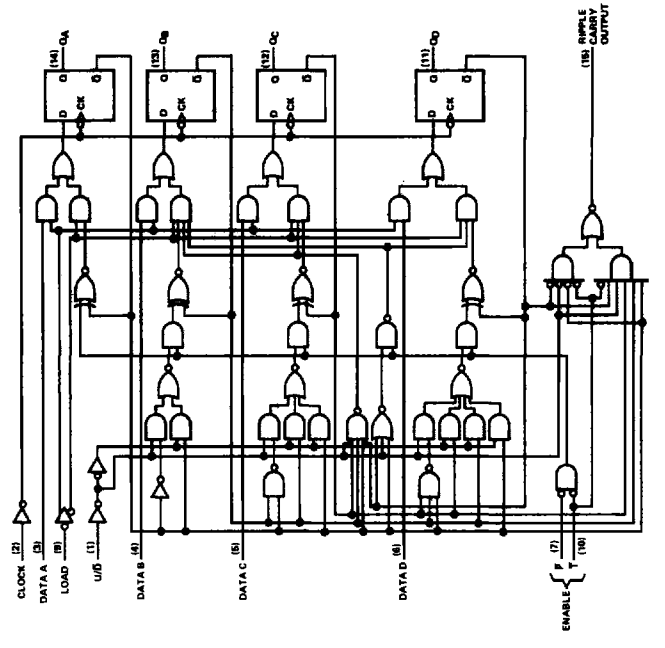


## functional block diagrams

SN54S169, SN74S169 BINARY COUNTERS




SN54S168, SN74S168 DECADE COUNTERS





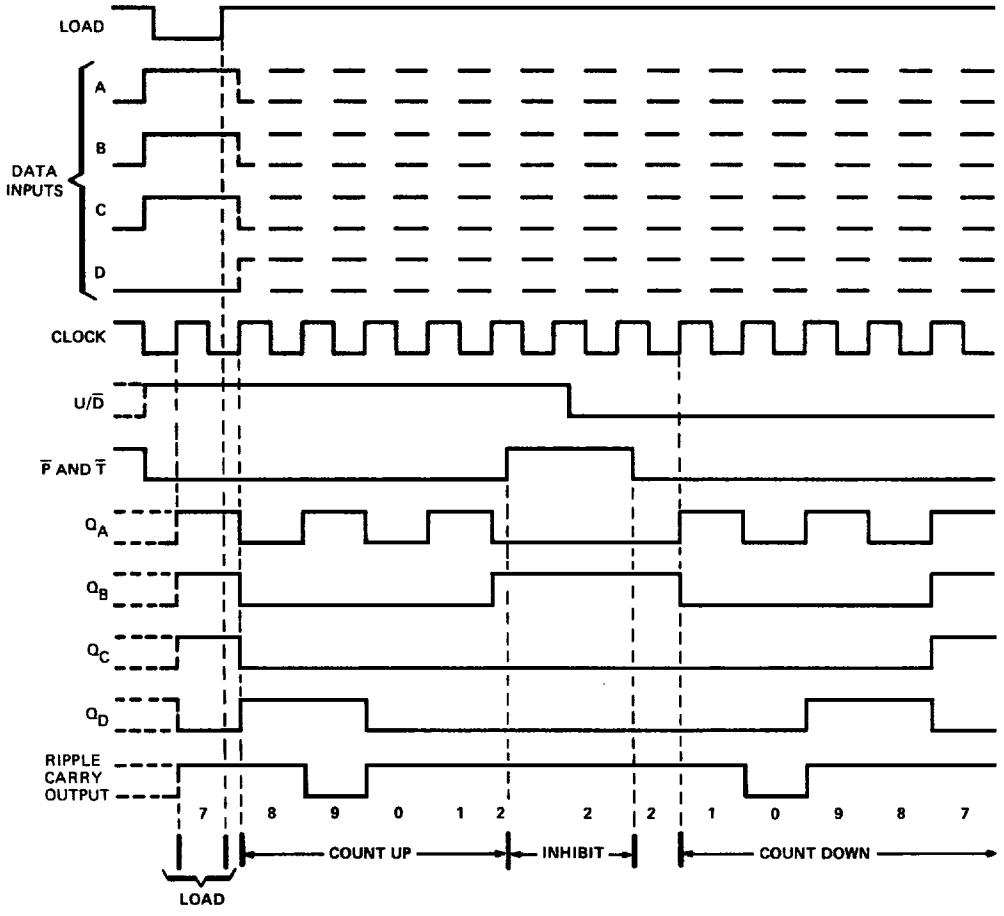

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## 'LS168A, 'S168 DECADE COUNTERS

### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

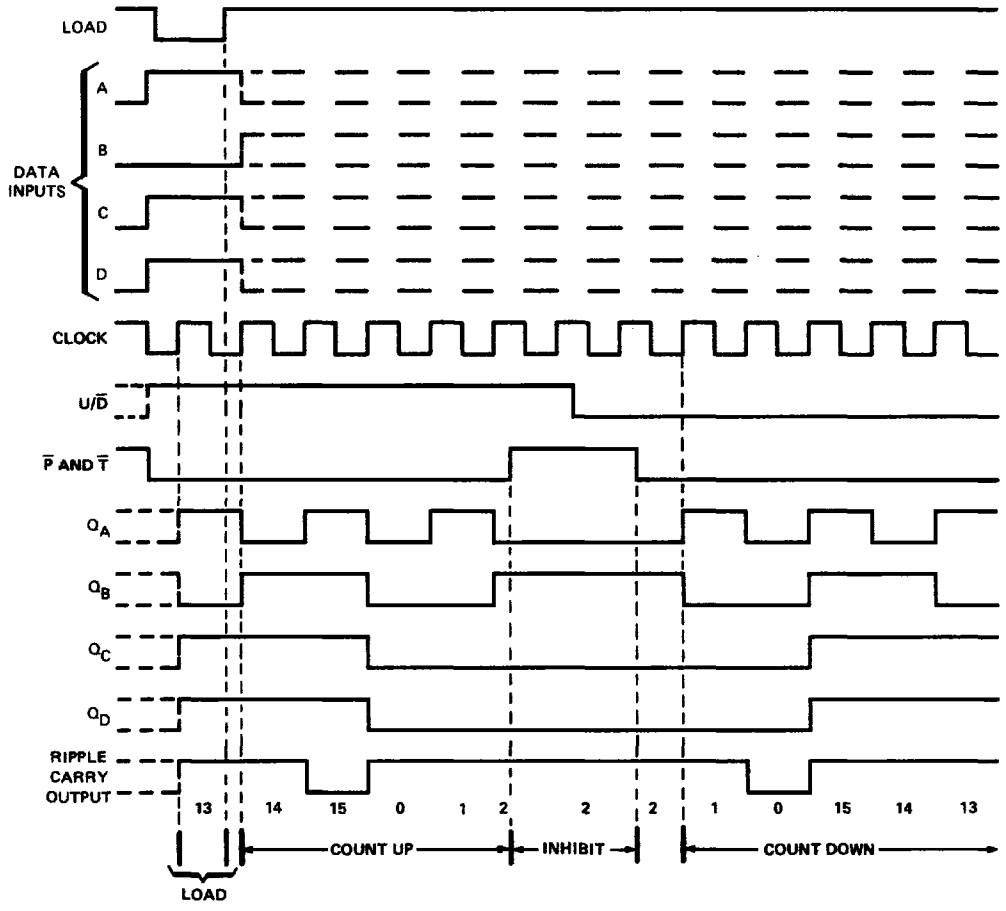


## 'LS169A, 'S169 BINARY COUNTERS

### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

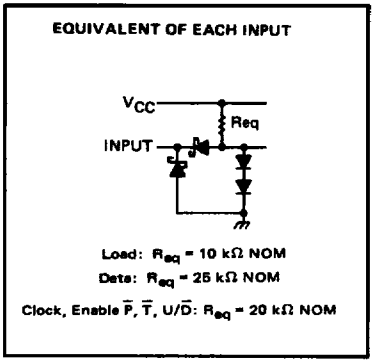
1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen

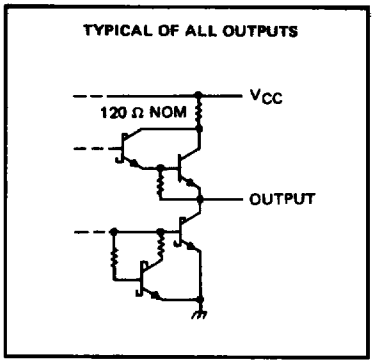





TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS168A, SN54LS169A . . . . . −55°C to 125°C
SN74LS168A, SN74LS169A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | SN54LS168A SN54LS169A | | | SN74LS168A SN74LS169A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | | 4 | | | 8 | mA |
| Clock frequency, $f_{clock}$ | | 0 | | 25 | 0 | | 25 | MHz |
| Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1) | | 25 | | | 25 | | | ns |
| Setup time, $t_{su}$ (see Figure 1) | Data inputs A, B, C, D | 20 | | | 20 | | | ns |
| | Enable P̄ or T̄ | 20 | | | 20 | | | |
| | Load | 25 | | | 25 | | | |
| | Up/Down | 30 | | | 30 | | | |
| Hold time at any input with respect to clock, $t_h$ (see Figure 1) | | 0 | | | 0 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |



TENTATIVE DATA

This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | SN54LS168A SN54LS169A | | | SN74LS168A SN74LS169A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | | Clock, $\overline{T}$ | | | | | 0.1 | | | 0.1 | |
| | | Load | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | High-level input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| | | Clock, $\overline{T}$ | | | | | 20 | | | 20 | |
| | | Load | | | | | 40 | | | 40 | |
| $I_{IL}$ | Low-level input current | A, B, C, D, $\overline{P}$, U/$\overline{D}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| | | Clock, $\overline{T}$ | | | | | −0.4 | | | −0.4 | |
| | | Load | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 2 | | 20 | 34 | | 20 | 34 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§*Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.*
NOTE 2: $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Figures 2 and 3 and Note 3 | 25 | 32 | | MHz |
| $t_{PLH}$ | Clock | Ripple carry | | | 23 | 35 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | |
| $t_{PLH}$ | Clock | Any Q | | | 13 | 20 | ns |
| $t_{PHL}$ | | | | | 15 | 23 | |
| $t_{PLH}$ | Enable $\overline{T}$ | Ripple carry | | | 10 | 14 | ns |
| $t_{PHL}$ | | | | | 10 | 14 | |
| $t_{PLH}$◇ | Up/Down | Ripple carry | | | 17 | 25 | ns |
| $t_{PHL}$◇ | | | | | 19 | 29 | |

¶$f_{max}$ ≡ Maximum clock frequency
$t_{PLH}$ ≡ propagation delay time, low-to-high-level output.
$t_{PHL}$ ≡ propagation delay time, high-to-low-level output.
◇*Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS168A or 15 for 'LS169A), the ripple carry output will be out of phase.*
NOTE 3: Load circuit is shown on page 3-11.

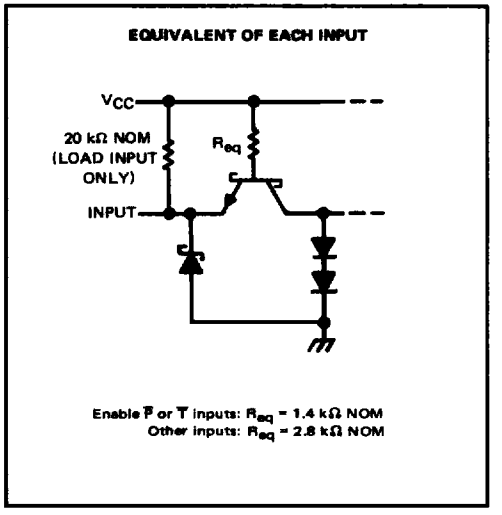
TENTATIVE DATA

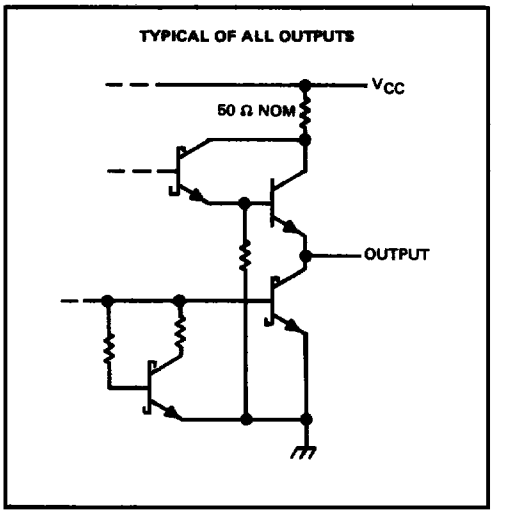
This page provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 4) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN54S168, SN54S169 (see Note 6) . . . . . −55°C to 125°C
SN74S168, SN74S169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

## recommended operating conditions

| | | SN54S168 SN54S169 | | | SN74S168 SN74S169 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −1 | | | −1 | mA |
| Low-level output current, $I_{OL}$ | | | | 20 | | | 20 | mA |
| Clock frequency, $f_{clock}$ | | 0 | | 40 | 0 | | 40 | MHz |
| Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1) | | 10 | | | 10 | | | ns |
| Setup time, $t_{su}$ (see Figure 1) | Data inputs A, B, C, D | 4 | | | 4 | | | ns |
| | Enable P̄ or T̄ | 14 | | | 14 | | | |
| | Load | 6 | | | 6 | | | |
| | Up/Down | 20 | | | 20 | | | |
| Hold time at any input with respect to clock, $t_h$ (see Figure 1) | | 1 | | | 1 | | | ns |
| Operating free-air temperature, $T_A$ (see Note 6) | | −55 | | 125 | 0 | | 70 | °C |

NOTES: 4. Voltage values, except interemitter voltage, are with respect to network ground terminal.
5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P̄ and T̄.
6. An SN54S168 or SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54S168 SN54S169 | | | SN74S168 SN74S169 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | 0.5 | | | 0.5 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current, Enable $\overline{T}$ | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | 100 | | | 100 | μA |
| | High-level input current, Other inputs | | | | 50 | | | 50 | |
| $I_{IL}$ | Low-level input current, Enable $\overline{T}$ | $V_{CC}$ = MAX, $V_I$ = 0.5 V | | | −4 | | | −4 | mA |
| | Low-level input current, Other inputs | | | | −2 | | | −2 | |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | −40 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | 100 | 160 | | 100 | 160 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

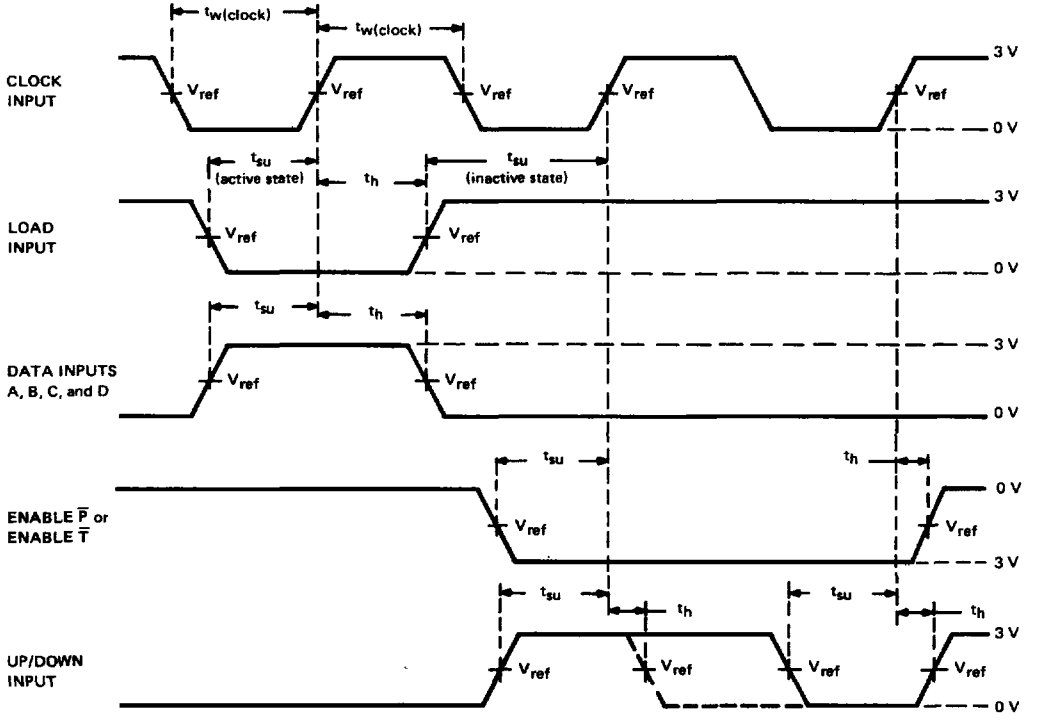
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | UP/DOWN = HIGH | | | UP/DOWN = LOW | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF, $R_L$ = 280 Ω, See Figures 2 and 3 and Note 7 | 40 | 70 | | 40 | 55 | | MHz |
| $t_{PLH}$ | Clock | Ripple carry | | | 14 | 21 | | 14 | 21 | ns |
| $t_{PHL}$ | | | | | 20 | 28 | | 20 | 28 | |
| $t_{PLH}$ | Clock | Any Q | | | 8 | 15 | | 8 | 15 | ns |
| $t_{PHL}$ | | | | | 11 | 15 | | 11 | 15 | |
| $t_{PLH}$ | Enable $\overline{T}$ | Ripple carry | | | 7.5 | 11 | | 6 | 12 | ns |
| $t_{PHL}$ | | | | | 15 | 22 | | 15 | 25 | |
| $t_{PLH}$◇ | Up/Down | Ripple carry | | | 9 | 15 | | 8 | 15 | ns |
| $t_{PHL}$◇ | | | | | 10 | 15 | | 16 | 22 | |

¶$f_{max}$ ≡ maximum clock frequency
$t_{PLH}$ ≡ propagation delay time, low-to-high-level output
$t_{PHL}$ ≡ propagation delay time, high-to-low-level output
◇Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'S169), the ripple carry output will be out of phase.
NOTE 7: Load circuit is shown on page 3-10.


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

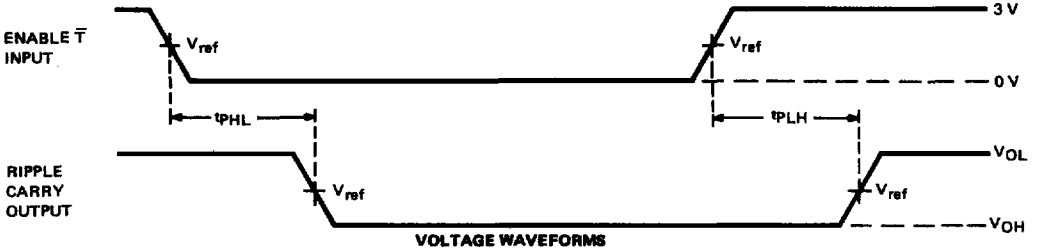
## PARAMETER MEASUREMENT INFORMATION




VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS168A and 'LS169A, $t_r \leq 15$ ns, $t_f \leq 6$ ns, and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. For 'LS168A and 'LS169A, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

FIGURE 1—PULSE WIDTHS, SETUP TIMES, HOLD TIMES

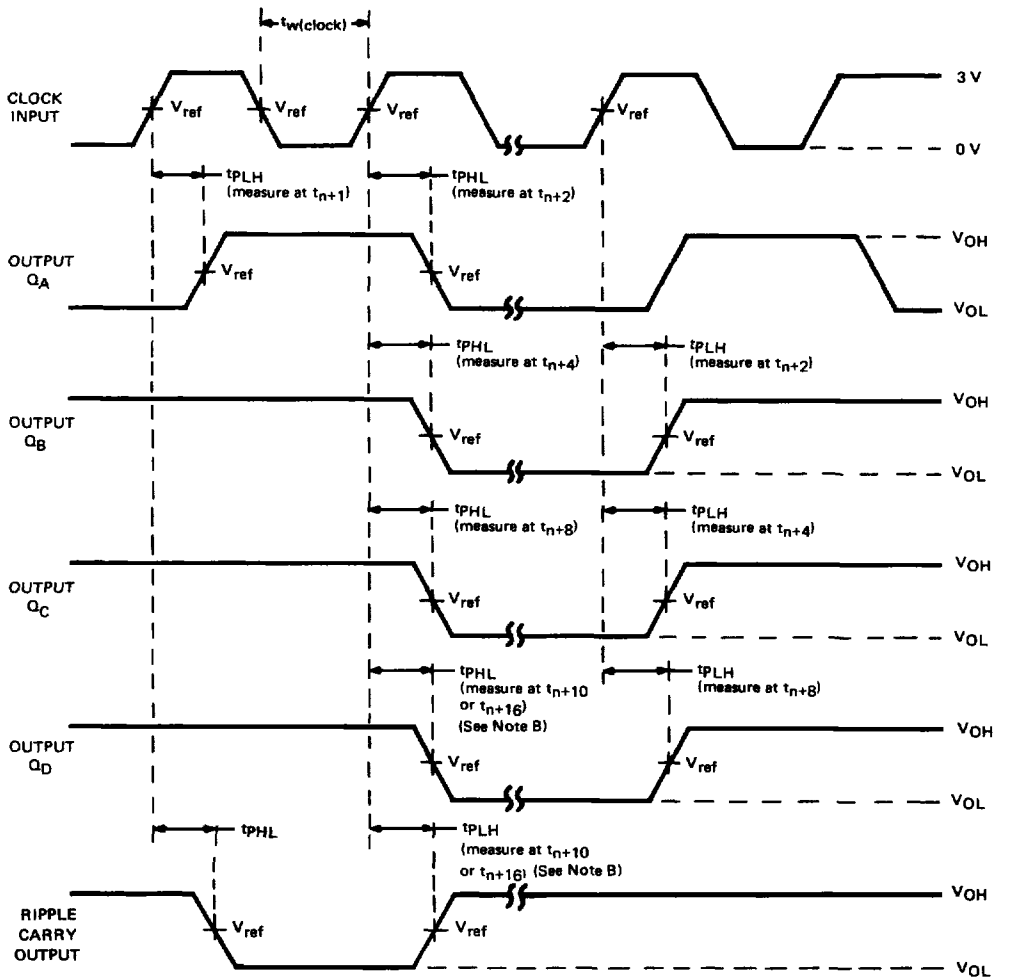



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS168A and 'LS169A, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. $t_{PLH}$ and $t_{PHL}$ from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count ($Q_A$ and $Q_D$ high for 'LS168A and 'S168, all Q outputs high for 'LS169A and 'S169).
C. For 'LS168A and 'LS169A, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS168A and 'S168, or 15 for 'LS169A and 'S169) the ripple carry output will be out of phase.

FIGURE 2—PROPAGATION DELAY TIMES TO CARRY OUTPUT

## PARAMETER MEASUREMENT INFORMATION




**UP-COUNT VOLTAGE WAVEFORMS**

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS168A and 'LS169A, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure $f_{max}$.

B. Outputs $Q_D$ and carry are tested at $t_{n+10}$ for the 'LS168A and 'S168, and at $t_{n+16}$ for the 'LS169A and 'S169, where $t_n$ is the bit-time when all outputs are low.

C. For 'LS168A and 'LS169A, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

**FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK**