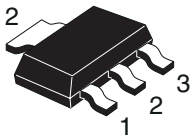
STN3PF06

P-channel 60 V - 0.20 Ω - 2.5 A - SOT-223
STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STN3PF06	60 V	< 0.22 Ω	2.5 A

- Extremely dv/dt capability
- 100% avalanche tested
- Application oriented characterization



SOT-223

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

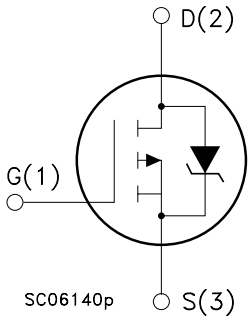


Table 1. Device summary

Order code	Marking	Package	Packaging
STN3PF06	N3PF06	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	2.5	A
I_D	Drain current (continuous) at T_C = 100 °C	1.5	A
I_{DM} (1)	Drain current (pulsed)	10	A
P_{TOT}	Total dissipation at T_C = 25 °C	2.5	W
	Derating factor	0.02	W/°C
dv/dt (2)	Peak diode recovery voltage slope	6	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-65 to 150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 3A$, di/dt ≤ 200 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb board max	50	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max(1)	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	260	°C

1. Surface mounted

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 10	µA µA
$I_{D(on)}$	On state drain current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} =10 V	2.5			A
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.5 A		0.20	0.22	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D= 1.25 A		1.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		850 230 75		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	I_D = 12 A, V_{DD} = 48 V, V_{GS} = 10 V *(see Figure 14)*		16 4 6	21	nC nC nC

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}= 30 V, I_D=6 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*		20 40		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}= 30 V, I_D=6 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*		40 10		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{clamp}= 48 V, I_D=12 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*		10 17 30		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				2.5 10	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1.5 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 12 A, di/dt = 100 A/µs V_{DD} = 30 V, T_j =150 °C		100 260 5.2		ns µC A

1. Pulse width limited by Tjmax
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

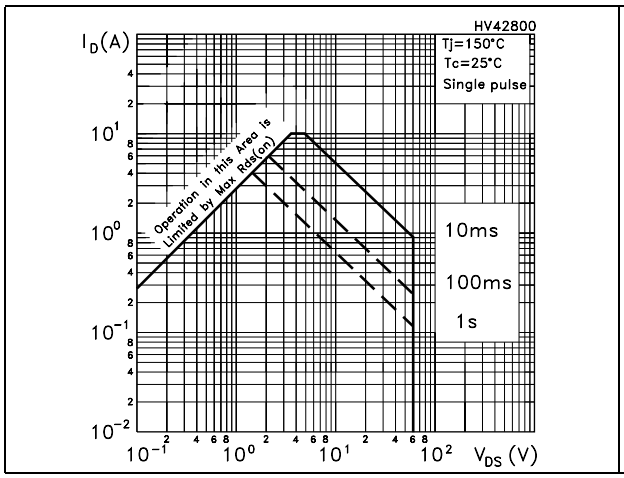


Figure 3. Thermal impedance

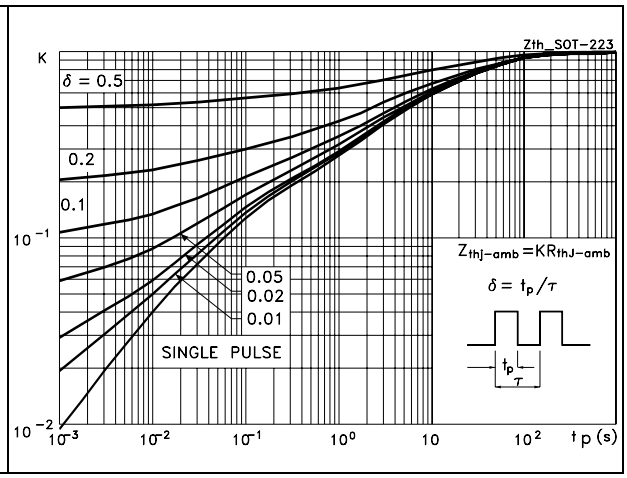


Figure 4. Output characteristics

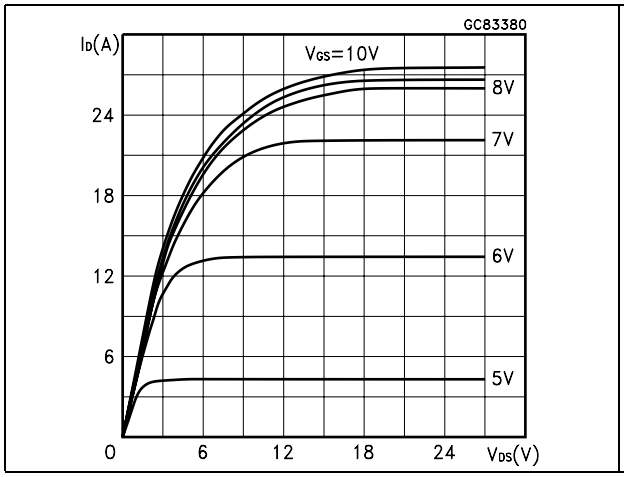


Figure 5. Transfer characteristics

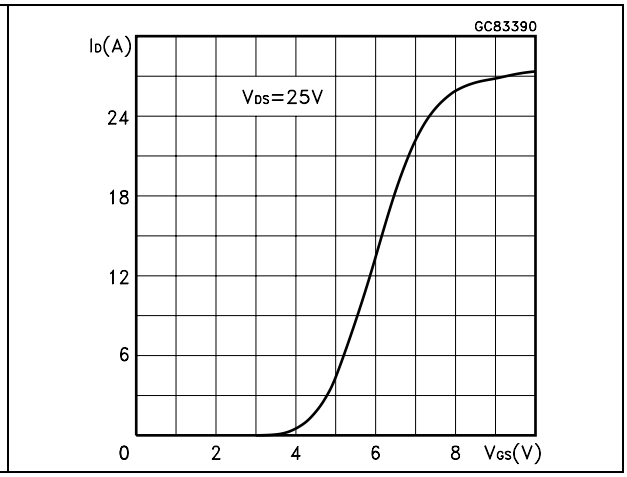


Figure 6. Transconductance

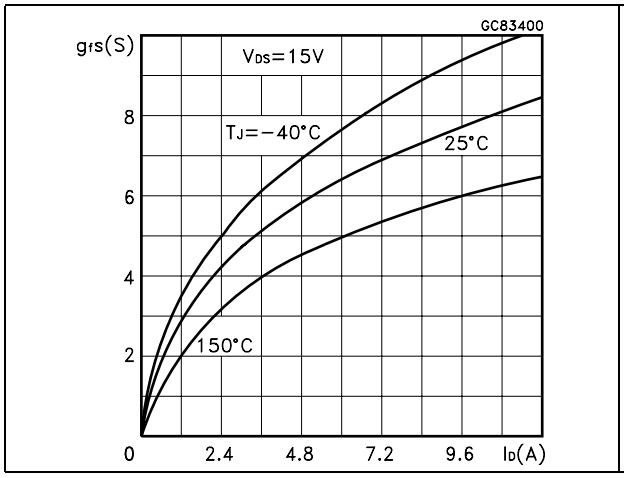


Figure 7. Static drain-source on resistance

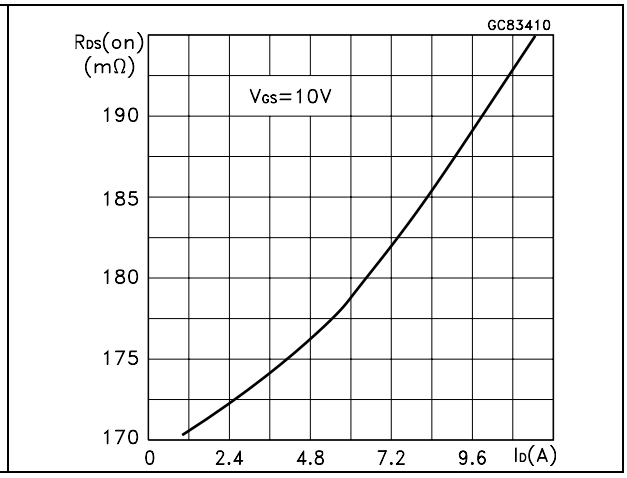


Figure 8. Gate charge vs gate-source voltage

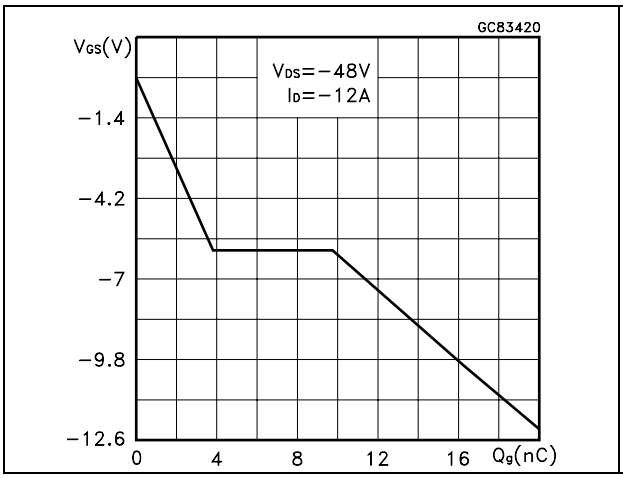


Figure 9. Capacitance variations

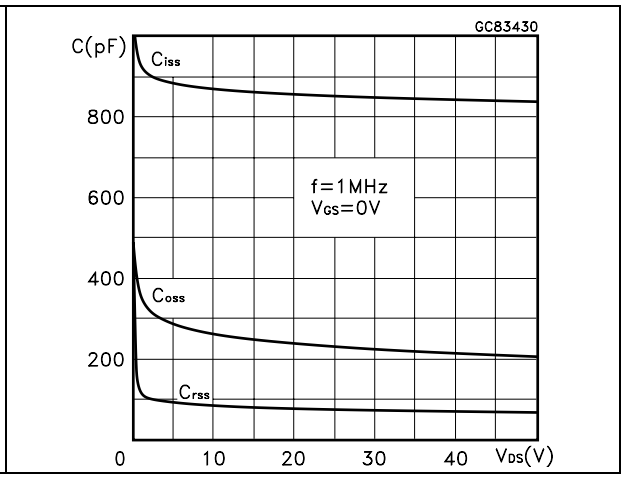


Figure 10. Normalized gate threshold voltage vs temperature

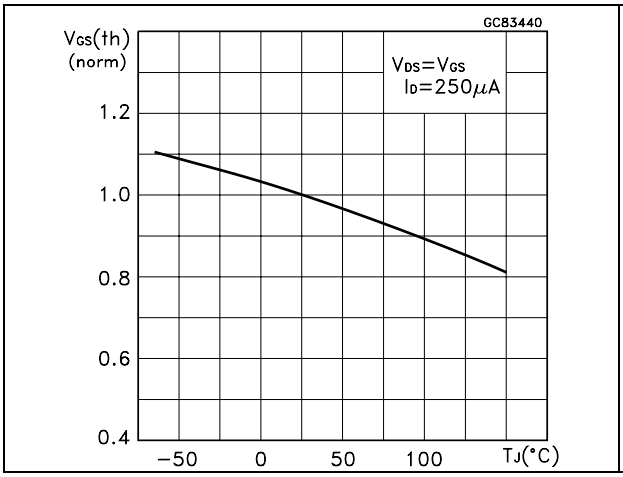


Figure 11. Normalized on resistance vs temperature

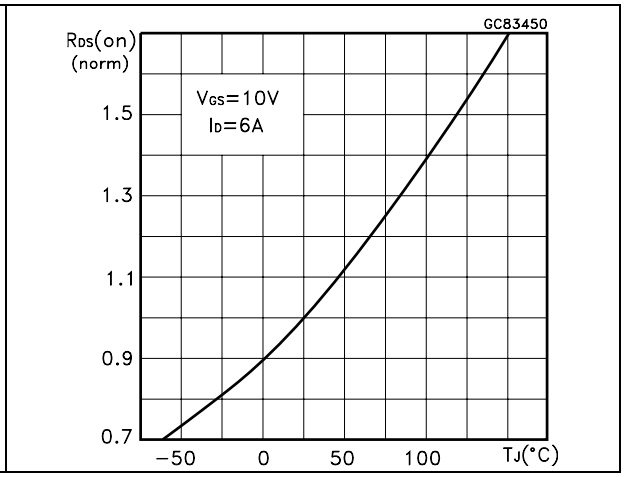
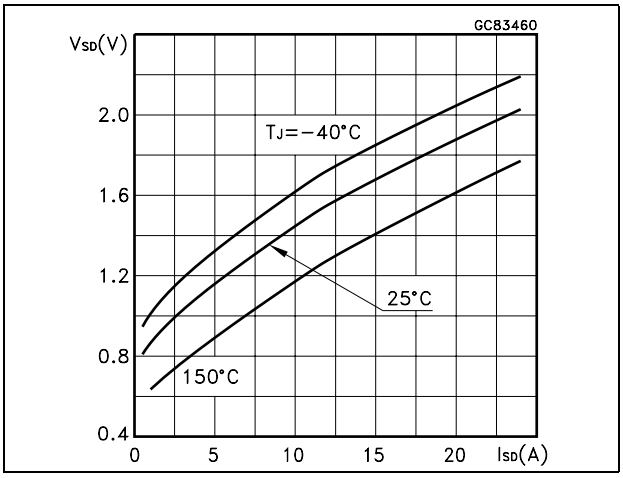


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

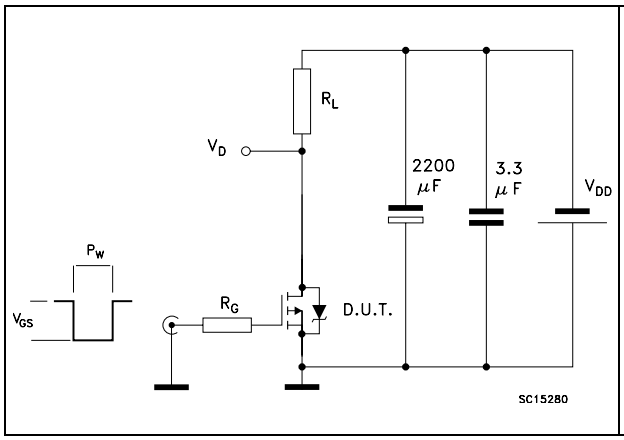


Figure 14. Gate charge test circuit

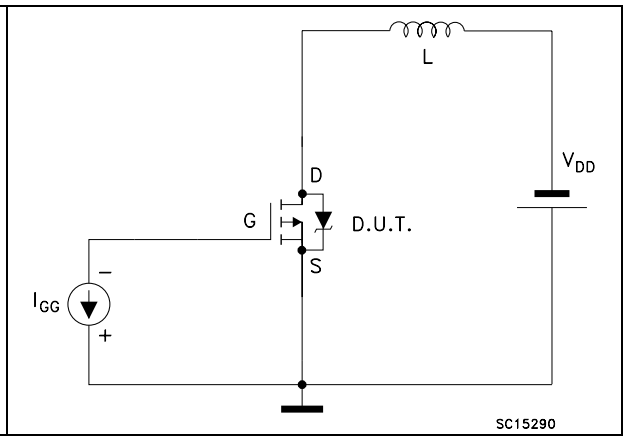
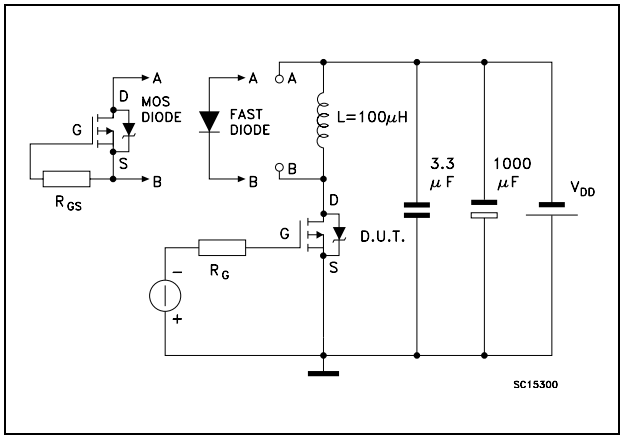


Figure 15. Test circuit for inductive load switching and diode recovery times

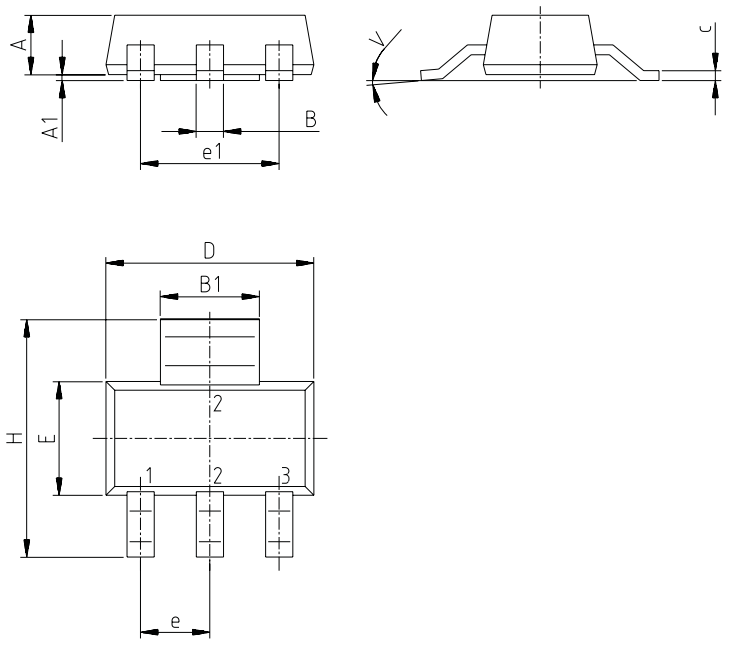


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



P008B

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
08-May-2007	3	The document has been reformatted
27-Mar-2008	4	Document status promoted from preliminary data to datasheet.

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