HT9435

P-Channel High Density Trench MOSFET

DESCRIPTION

The HT9435 uses advanced technology to provide excellent Rds (on), low switching loss and reasonable price.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

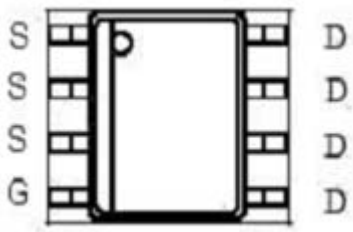
FEATURES

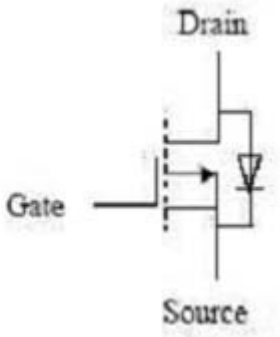
- -30V/-5.1A, R_{DS}(ON) = 50mΩ @ V_{GS} = -10V
- -30V/-3.6A, R_{DS}(ON) = 95mΩ @ V_{GS} = -4.5V
- Super high dense cell design for low R_{DS}(ON)
- Rugged and reliable
- SOP-8 package design

APPLICATIONS

- POWER Management in Note
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- LCD Display

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

(TA=25 °C Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Drain Current	Continuous (1)	I_D	-5.1	A
	Pulse (2)	I_{DM}	-20	
Drain-Source Diode Forward Current(1)		I_s	-2.6	A
Maximum Power Dissipation (1)		P_D	2.5	W
Operating junction temperature range		T_J	150	℃
Storage temperature range		T_{STG}	-55 to 150	℃

THERMAL RESISTANCE RATINGS

Thermal Resistance	Symbol	Maximum	Unit
Junction-to-Ambient	$R\theta_{JA}$	50	℃/W

Note :

1. Surface Mounted on FR4 Board , t ≤ 10sec
2. Pulse Test：Pulse width ≤ 300us , Duty Cycle ≤ 2%

ELECTRICAL CHARACTERISTICS

(TA=25 ℃Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0 V	-	-	-1	μA
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ± 25V	-	-	±100	nA
On Characteristics (1)						
Gate Threshold Voltage	V_{GS}(th)	V_{GS} = V_{DS}, I_D= -250μA	-1.2	-1.8	-2.4	V
Drain-Source On State Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D= -5.1A	-	40	50	mΩ
		V_{GS} = -4.5V, I_D= -3.6A	-	67	95	
Drain-Source Diode Characteristics (1)						
Diode Forward Voltage	VSD	I_S = -1.0A, V_{GS} = 0V	-	-	-1.0	V
Dynamic Parameters (2)						
Input Cap.	Ciss	V_{DS} = -15V, V_{GS} = 0V f = 1MHz	-	910	-	pF
Output Cap.	Coss		-	170	-	
Reverse Transfer Cap	Crss		-	120	-	
Switching Parameters (2)						
Total Gate Charge	Q_g	V_{DS} = -15V, V_{GS} = -10V, I_D = -1A	-	17.4	-	nC
		V_{DS} = -15V, V_{GS} = -4.5V, I_D = -1A		9.1	-	
Gate-Source Charge	Q_{gs}	V_{DS} = -15V, V_{GS} = -10V, I_D = -1A	-	3.1	-	
Gate-Drain Charge	Q_{gd}		-	3.5	-	
Turn-On Time	$T_{D(on)}$	V_{DS} = -15V, R_L= 15Ω I_D = -1A, V_{GEN} = -10V, R_G=10Ω	-	5.36	-	nS
	Tr		-	7.76	-	
Turn-Off Time	$T_{D(off)}$		-	15.84	-	
	Tf		-	9.84	-	

Note :

1. Pulse Test：Pulse width ≤ 300us , Duty Cycle ≤ 2%
2. Guaranteed by design, not subject to production testing

TYPICAL CHARACTERICTICS

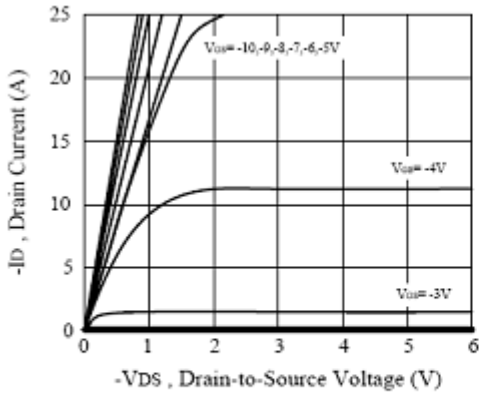


Figure 1. Output Characteristics

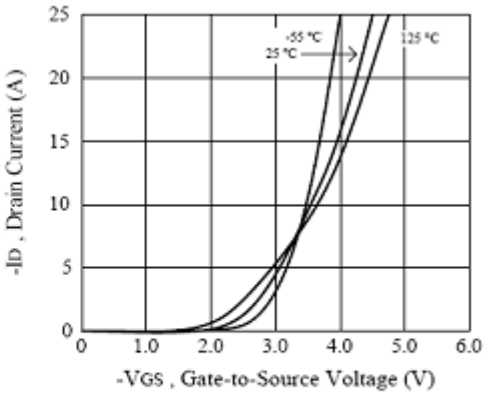


Figure 2. Transfer Characteristics

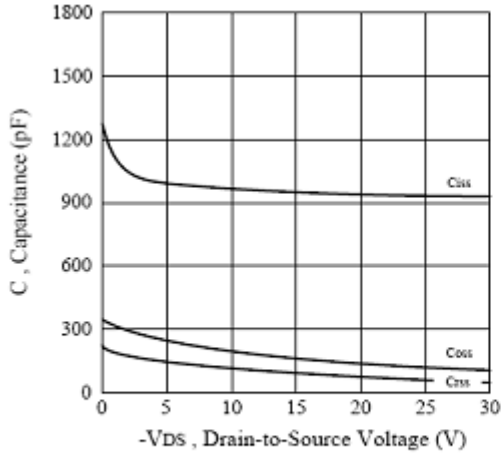


Figure 3. Capacitance

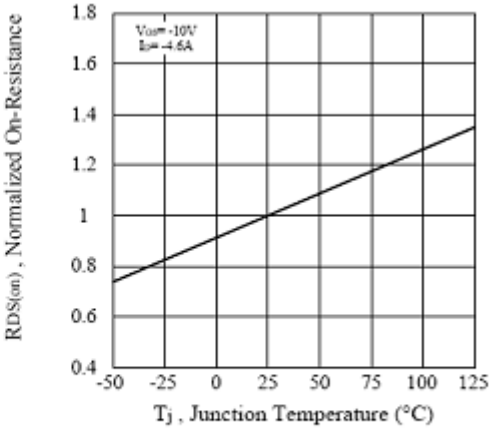


Figure 4. On-Resistance Variation with Temperature

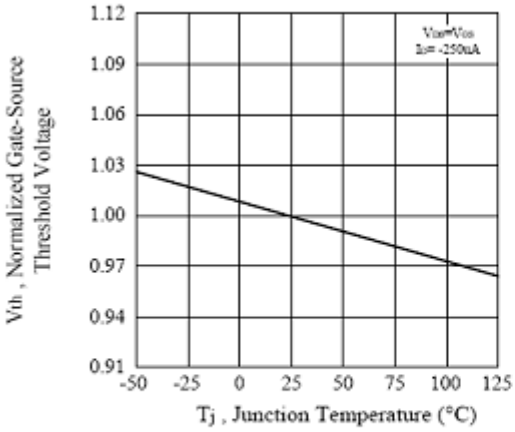


Figure 5. Gate Threshold Variation with Temperature

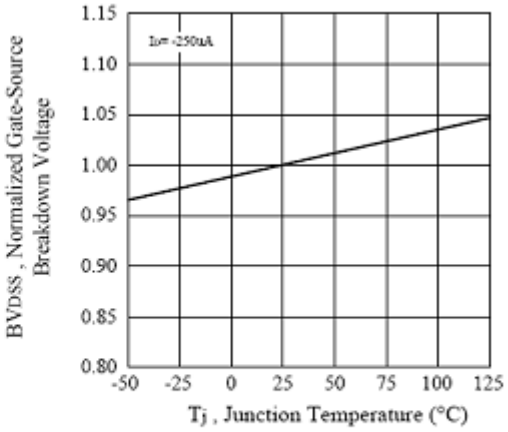


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERICTICS

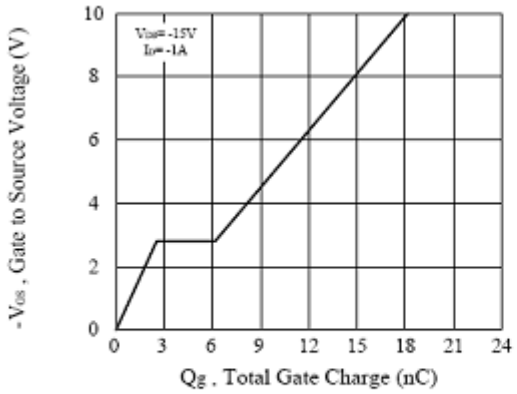


Figure 7. Gate Charge

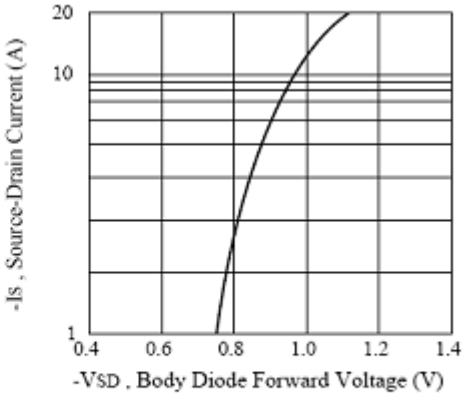


Figure 8. Body Diode Forward Voltage Variation with Source Current

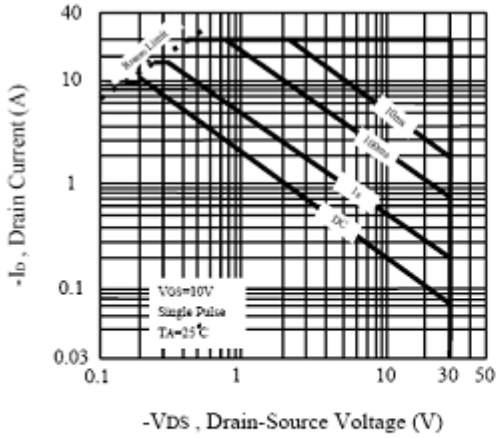


Figure 9. Maximum Safe Operating Area

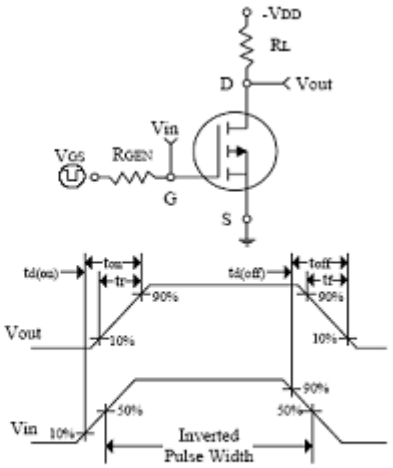


Figure 10. Switching Test Circuit and Switching Waveforms

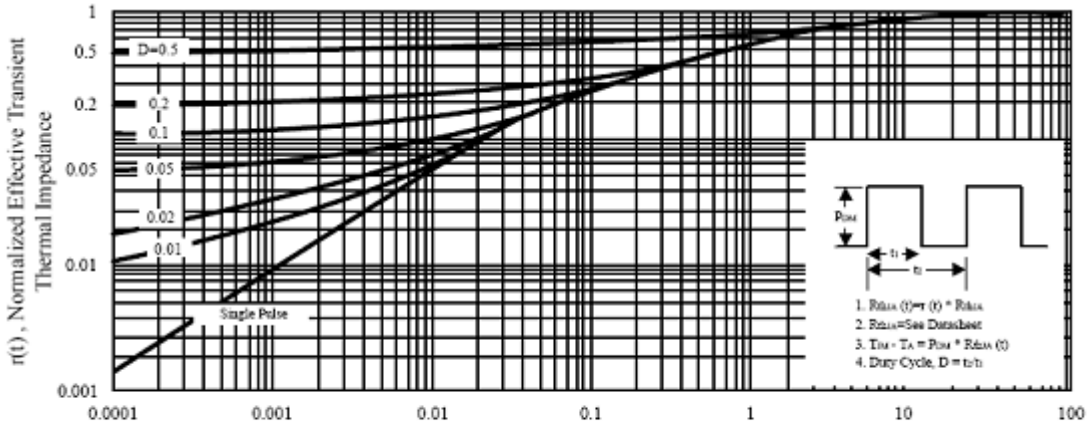
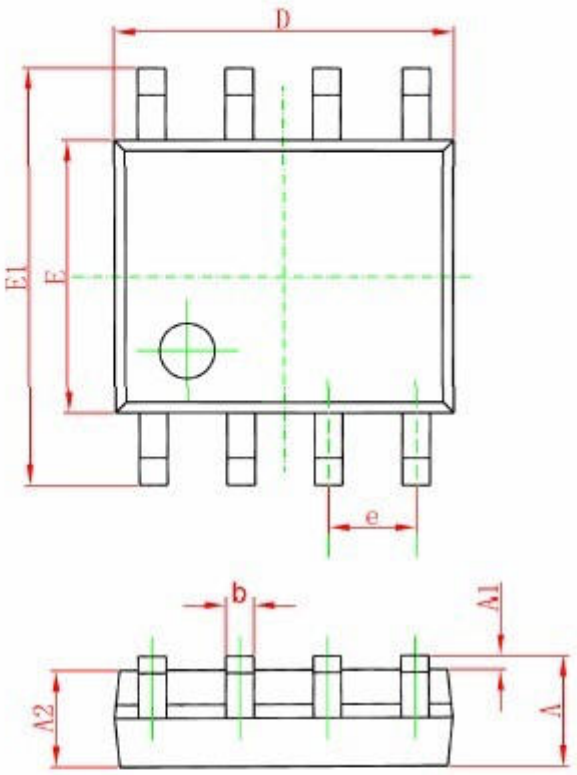


Figure 11. Normalized Thermal Transient Impedance Curve

PACKAGE DESCRIPTION

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°