T-79-15

MOTOROLA

TL071
TL072
TL074

Specifications and Applications Information

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

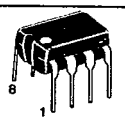
SILICON MONOLITHIC INTEGRATED CIRCUITS

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

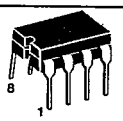
These low-noise JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low-noise and low harmonic distortion making them ideal for use in high-fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

- Low Input Noise Voltage — 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion — 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance — 10^{12} Ω Typ
- High Slew Rate — 13 V/μs Typ
- Wide Gain Bandwidth — 4.0 MHz Typ
- Low Supply Current — 1.4 mA per Amp

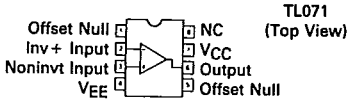


P SUFFIX
PLASTIC PACKAGE
CASE 626-05

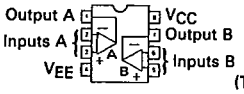


JG SUFFIX
CERAMIC PACKAGE
CASE 693-02

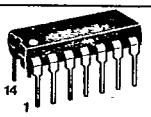
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



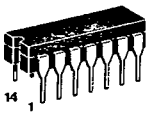
TL071 (Top View)



TL072 (Top View)

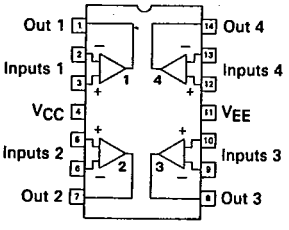


N SUFFIX
PLASTIC PACKAGE
CASE 646-06
(TL074 Only)



J SUFFIX
CERAMIC PACKAGE
CASE 632-08
(TL074 Only)

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



TL074 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	TL071ACD, BCD, CD	0 to +70°C	SO-8
	TL071ACJG, BCJG, CJG		Ceramic DIP
	TL071ACP, BCP, CP		Plastic DIP
	TL071MJG	−55 to +125°C	Ceramic DIP
Dual	TL072ACD, BCD, CD	0 to +70°C	SO-8
	TL072ACJG, BCJG, CJG		Ceramic DIP
	TL072ACP, BCP, CP		Plastic DIP
	TL072MJG	−55 to +125°C	Ceramic DIP
Quad	TL074ACD, BCD, CD	0 to +70°C	SO-14
	TL074ACJ, BCJ, CJ		Ceramic DIP
	TL074ACN, BCN, CN		Plastic DIP
	TL074MJ	−55 to +125°C	Ceramic DIP

TL071, TL072, TL074

MAXIMUM RATINGS

Rating	Symbol	TL07_ M	TL07_ C TL07_ AC TL07_ BC	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	+18 −18	V
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	±15	V
Output Short-Circuit Duration (Note 2)	t_S	Continuous		
Power Dissipation Plastic Package (N,P) Derate above T_A = +47°C Ceramic Package (J, JG) Derate above T_A = +82°C	P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	— — 680 10	680 10 680 10	mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25° unless otherwise noted).

Characteristic	Symbol	TL07_ M			TL07_ C TL07_ AC TL07_ BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0) TL071, TL072 TL074 TL07_ A TL07_ B	V_{IO}	— — — —	3.0 3.0 — —	6.0 9.0 — —	— — — —	3.0 3.0 3.0 2.0	10 10 6.0 3.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL07_ TL07_ A, TL07_ B	I_{IO}	— —	5.0 —	50 —	— —	5.0 5.0	50 50	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL07_ TL07_ A, TL07_ B	I_{IB}	— —	30 —	200 —	— —	30 30	200 200	pA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL07_ TL07_ A, TL07_ B	V_{ICR}	±11 —	+15, −12 —	— —	±10 ±11	+15, −12 +15, −12	— —	V
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k) TL07_ TL07_ A, TL07_ B	A_{VOL}	35 —	150 —	— —	25 50	150 150	— —	V/mV
Output Voltage Swing (Peak-to-Peak) (R_L = 10 k)	V_O	24	28	—	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq$ 10 k) TL07_ TL07_ A, TL07_ B	CMRR	80 —	100 —	— —	70 80	100 100	— —	dB
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k) TL07_ TL07_ A, TL07_ B	PSRR	80 —	100 —	— —	70 80	100 100	— —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	10	13	—	—	13	—	V/μs

TL071, TL072, TL074

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25° unless otherwise noted).

Characteristic	Symbol	TL07_ M			TL07_ C, TL07_ AC, TL07_ BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	18	—	—	18	—	nV/√Hz
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	—	0.01	—	—	0.01	—	pA/√Hz
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \leq$ 1.0 k $R_L \geq$ 2.0 k, f = 1000 Hz	THD	—	0.01	—	—	0.01	—	%
Channel Separation A_V = 100	—	—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} [Note 3]).

Characteristic	Symbol	TL07_ M			TL07_ C, TL07_ AC, TL07_ BC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0)	V_{IO}							mV
TL071, TL072		—	—	9.0	—	—	13	
TL074		—	—	15	—	—	13	
TL07_ A		—	—	—	—	—	7.5	
TL07_ B		—		—		—	5.0	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}							nA
TL07_		—	—	20	—	—	2.0	
TL07_ A, TL07_ B		—	—	—	—	—	2.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}							nA
TL07_		—	—	50	—	—	7.0	
TL07_ A, TL07_ B		—	—	—	—	—	7.0	
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k)	A_{VOL}							V/mV
TL07_		20	—	—	15	—	—	
TL07_ A, TL07_ B		—	—	—	25	—	—	
Output Voltage Swing (Peak-to-Peak)	V_O							V
(RL ≥ 10 k)		24	—	—	24	—	—	
($R_L \geq$ 2.0 k)		20	—	—	20	—	—	

NOTES (Continued):

3. T_{low} = −55°C for TL071M, TL072M, TL074M
= 0°C for TL071C, TL071AC, TL071BC
TL072C, TL072AC, TL072BC
TL074C, TL074AC
T_{high} = + 125°C for TL071M, TL072M, TL074M
= +70°C for TL071C, TL071AC, TL071BC
TL072C, TL072AC, TL072BC
TL074C, TL074AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to ambient temperatures as possible, pulse techniques must be used during test.

TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

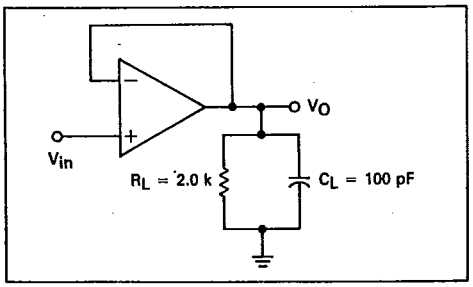


FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER

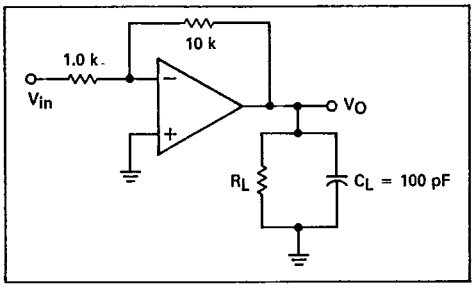


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

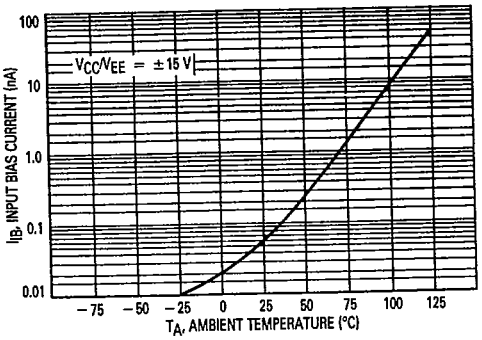


FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY

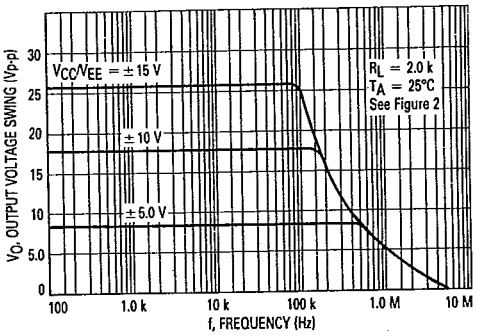


FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

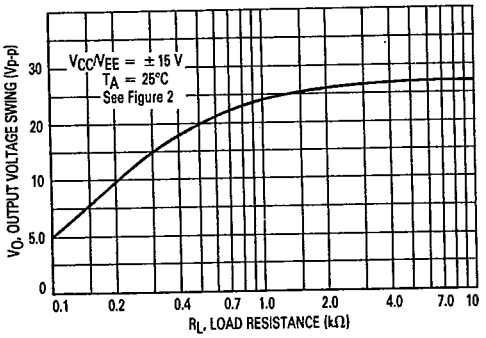


FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

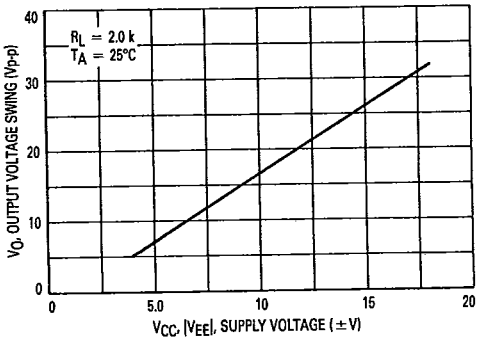


FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE

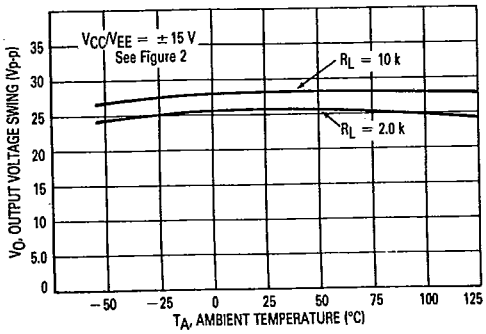
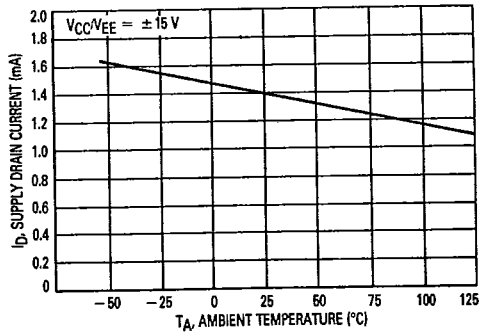


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE



2

FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

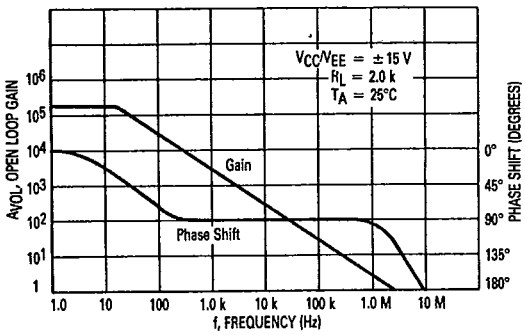


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

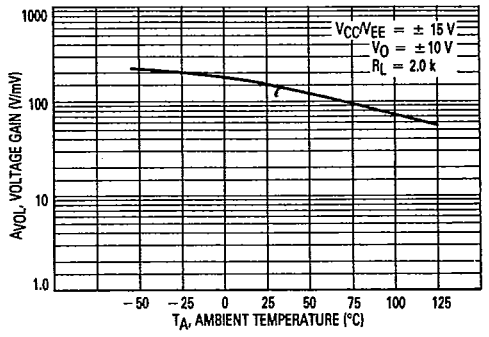


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

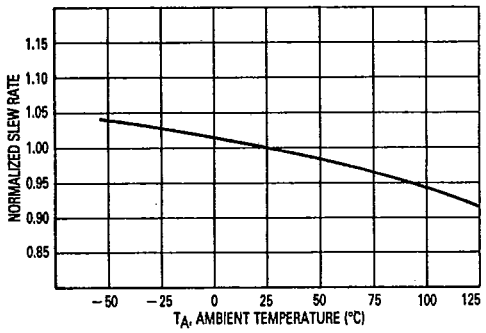


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

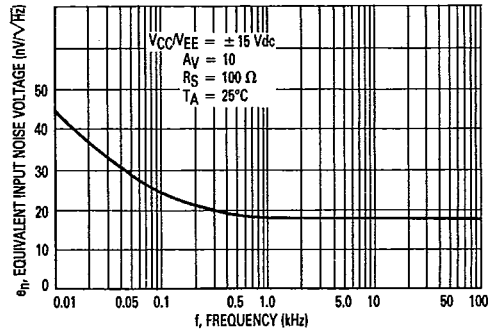
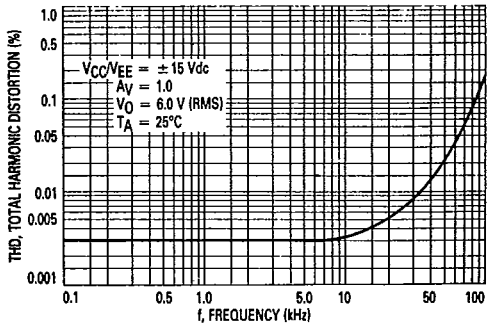


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



TL071, TL072, TL074

2

REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)

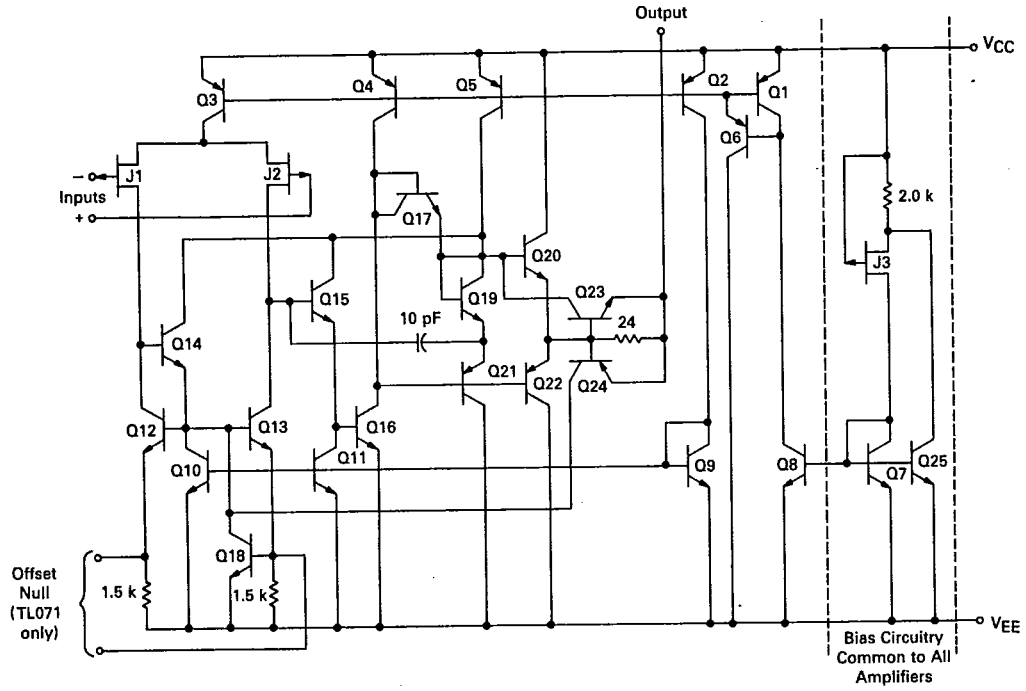


FIGURE 14 — AUDIO TONE CONTROL AMPLIFIER

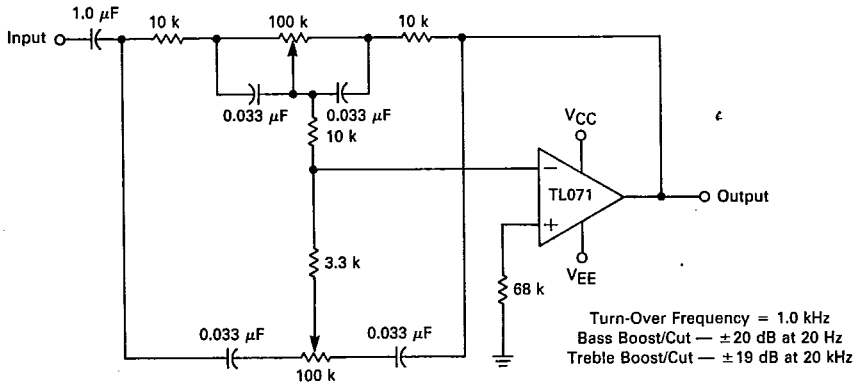


FIGURE 15 — HIGH Q NOTCH FILTER