



# REALTEK

**RTL8324**

**RTL8324-LF**

**24-PORT 10/100M ETHERNET SWITCH  
CONTROLLER WITH EMBEDDED MEMORY**

**DATASHEET**

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## **REVISION HISTORY**

<b>Revision</b>	<b>Release Date</b>	<b>Summary</b>
1.0	2005/03/21	First release.
1.1	2006/02/21	Add section 14 Thermal Data, page 82. Add section 8.28.3 Serial LED Bi-Color LED Mode, page 36. Remove the RRCP function.
1.2	2006/04/10	Correct EEPROM description (see Table 25, page 40). Add Absolute Maximum Ratings, page 79. Add pin description of internal pull-up or pull-down (see Table 1, page 6).

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## 1. General Description

The RTL8324 is a layer-2 switch controller that integrates 1.25Mbits of high-speed SSRAM, an 8K-entry MAC address lookup table, 24 Ethernet/Fast Ethernet MACs, and a switch engine into one chip.

With QoS, Trunking, VLAN, bandwidth control, remote control, and an 0.18 $\mu$ m process, the RTL8324 is a cost effective switch controller for a 24-Port 10/100 dumb switch application.

Port trunking is supported on all ports to increase bandwidth. Load balancing and fault tolerance provide top performance and reliability. The RTL8324 provides 2-level priority queues for multimedia or real-time network applications. The CoS (Class of Service) can be port-based, IEEE 802.1p tag-based, and/or TCP/IP header TOS/DS field-based. The RTL8324 supports up to 32 VLAN groups that may be configured as port-based VLANs and/or IEEE 802.1Q tagged VLANs. ARP broadcast and Leaky VLAN are also supported.

The RTL8324 supports diagnostics and analysis. Counters are included for: RX byte count, RX packet count, TX byte count, TX packet count, CRC error packet count, collision packet count, dropped packet count, and dropped byte count. The RTL8324 supports TX and RX bandwidth control on each port; 128Kbps, 256Kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, or 8Mbps may be selected in each direction.

The RTL8324 provides for a Scan LED Group to display each port's status, without extra component cost. A loop-detection function is provided to notify whether a network loop exists, either via a visual LED, or via a register flag for smart applications. LED displays for broadcast storm, trunking status, flow control, and traffic utilization are also provided.

Maximum packet length can be up to 1552 bytes. The RTL8324 supports the ability to drop 802.1D specified reserved group MAC addresses: (01-80-C2-00-00-04 to 01-80-C2-00-00-0F) according to pin strapping upon reset, or register setting. The RTL8324 default setting enables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered.

The RTL8324 supports IEEE 802.3x full duplex flow control and back pressure half duplex flow control. Full duplex flow control can be disabled both manually or automatically to ensure QoS control or bandwidth control operates correctly. Broadcast storm filtering prevents network crashes caused by abnormal broadcast activity.

As well as supporting IEEE 802.3u auto-negotiation, the RTL8324 supports PHY Read/Write registers to access PHY registers through an MDC/MDIO interface. This expands system configuration options.

The RTL8324 is designed with a link-list buffer management architecture and provides 4.8Gbps of bandwidth to achieve wire-speed performance. It also has an intelligent switching engine to prevent Head-of-Line blocking. Only a single 25MHz crystal is required for clock generation.

## 2. Features

- 24-port 10/100Mbps layer-2 Ethernet switch controller with embedded lookup table and packet buffer
- Supports SMII on all ports
- Built-in 8K entry MAC address lookup table plus 64-entry CAM to eliminate hash collision problems
- Built-in 1.25Mbit SSRAM packet buffer
- Non-blocking wire-speed forwarding and filtering (4.8Gbps throughput)
- Store and forward architecture and head-of-line blocking prevention
- All ports support Speed, Duplex, and 802.3x flow-control ability auto-negotiation
- Supports broadcast storm filtering control
- Supports Trunking function with load balancing and fault tolerance
- Supports up to 32 VLAN groups for port-based VLAN and 802.1Q tag VLAN
- Supports Leaky VLAN
- Two priority queues for three types of Class of Service (CoS)
  - ◆ Port-based
  - ◆ 802.1p priority tag
  - ◆ TCP/IP header's TOS/DS classifier
- Weighted round robin queue scheduling
- Priority tag insert and remove function
- Supports ASIC based IGMPv1 and IGMPv2 snooping function
- Supports pin strapping, EEPROM, or serial CPU configuration interface
- Supports PHY register read/write access
- Supports simple MIB counters
- TX/RX packet/byte, CRC error, and collision counter for diagnostics/statistics
- Supports per-port bandwidth control
- Supports loop detection and indication function
- Provides Scan LED, serial LED, and parallel LED interface for port properties and diagnostic display
- Provides configurable Port Mirror function.
- Needs only one low-cost 25MHz crystal or OSC input
- 0.18 $\mu$ m, 128-pin PQFP, 3.3V single power, 5V I/O tolerance

### 3. System Applications

- 10/100Mbps switch controller for a 24-Port 10/100 dumb or smart switch application.

### 4. Block Diagram

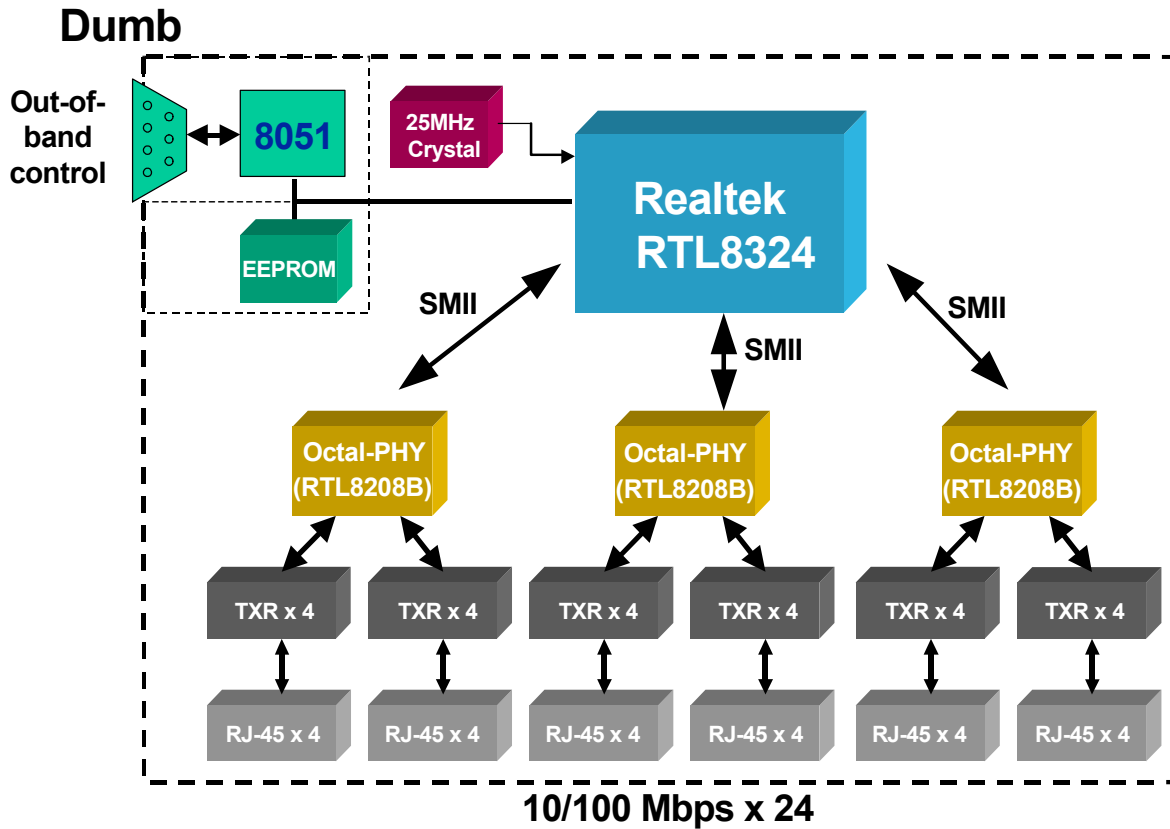


Figure 1. Block Diagram

## 5. Functional Block Diagram

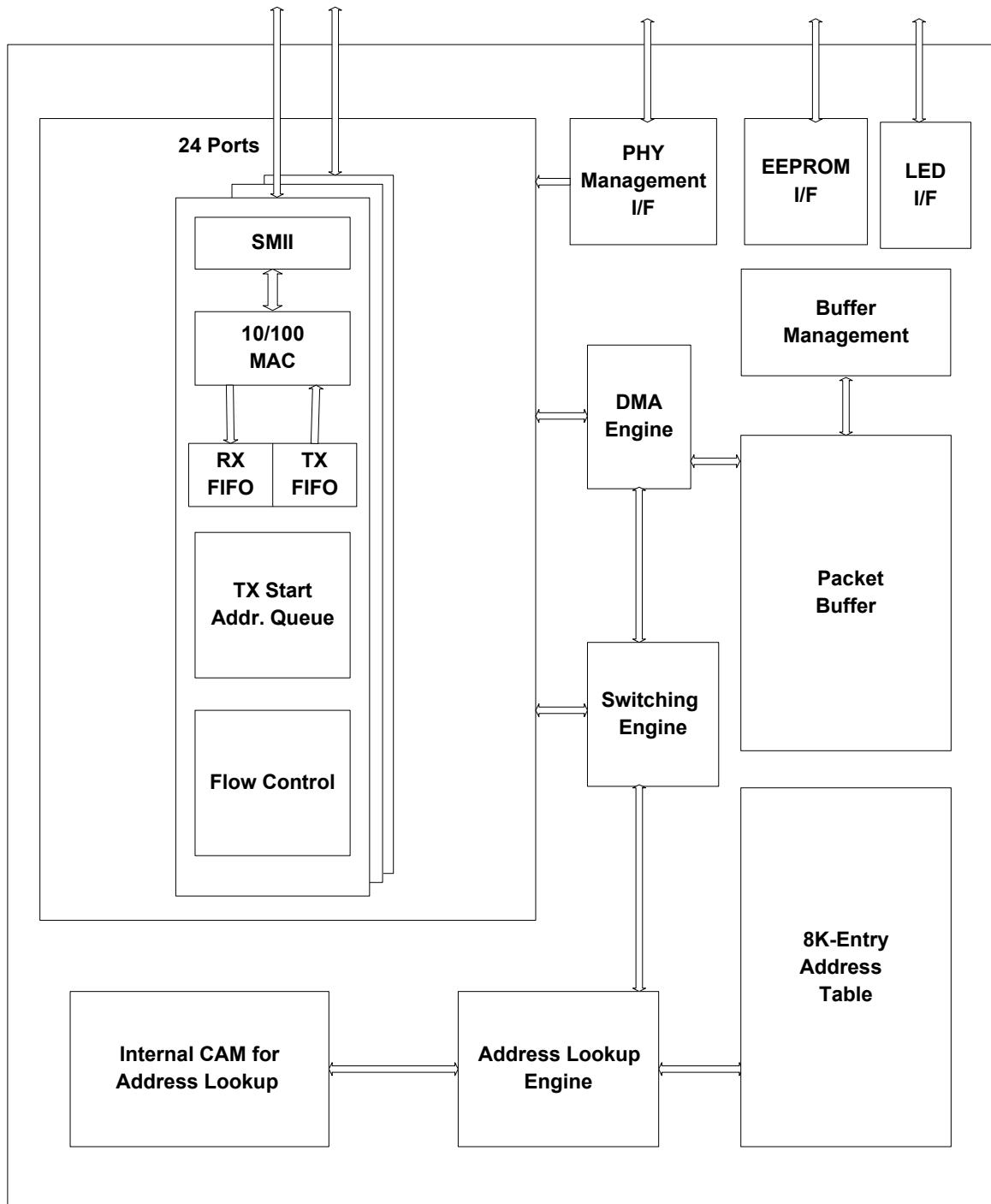


Figure 2. Functional Block Diagram



## 6. Pin Assignments

### 6.1. Pin Assignment Figure

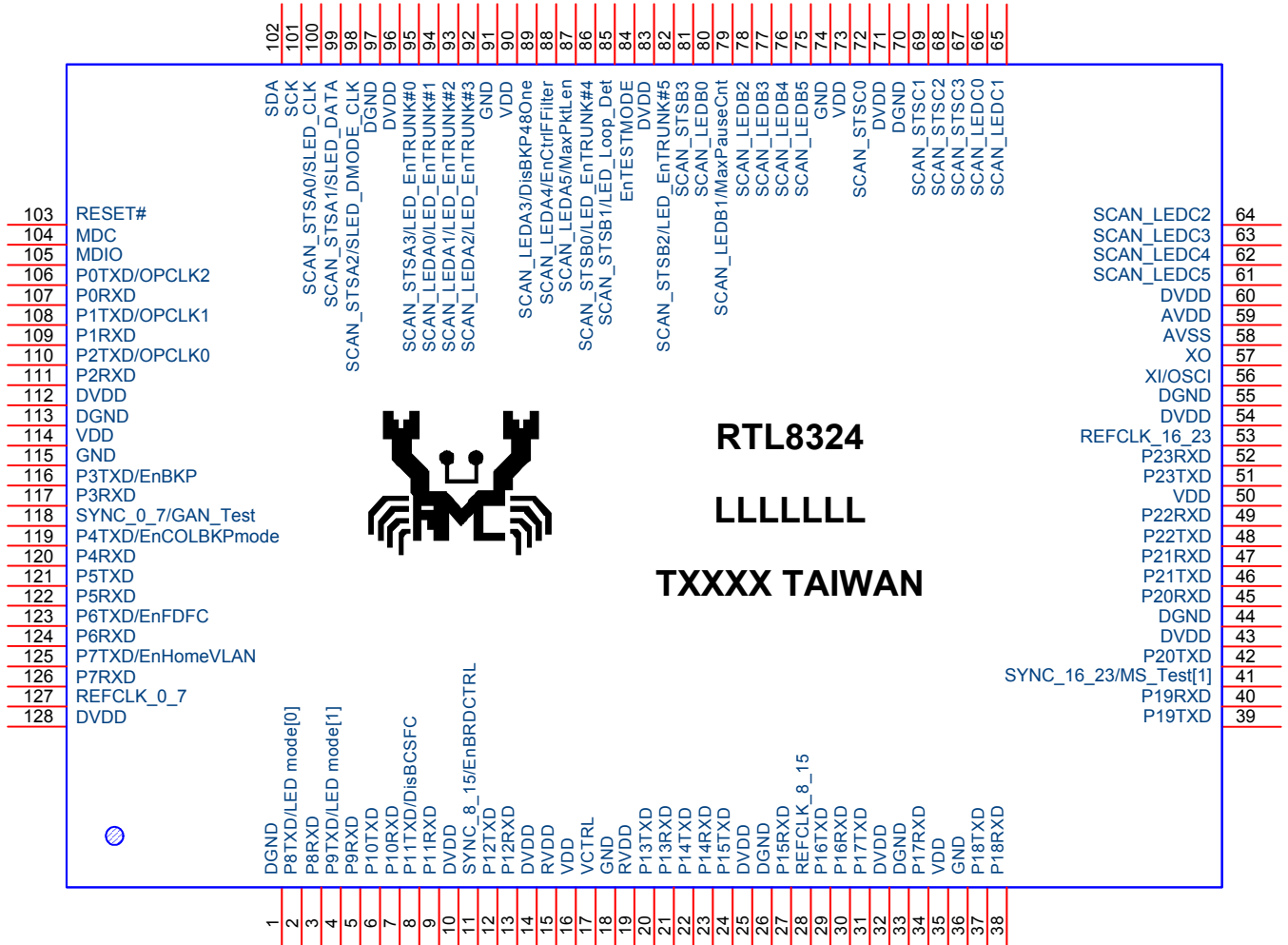


Figure 3. Pin Assignments

### 6.2. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 3.

### 6.3. Pin Assignment Table (128-Pin PQFP)

Type codes used: P = Power; G = Ground, I = Input, O = Output. PU= Internal Pull-up. PD= Internal Pull-down. Internal resistor = 40KΩ

**Table 1. Pin Assignment Table (PQFP-128)**

Pin No.	Type	Pin Name	Pin No.	Type	Pin Name
1	G	DGND	38	I <sub>PD</sub>	P18RXD
2	I/O <sub>PU</sub>	P8TXD/LED mode[0]	39	O <sub>PU</sub>	P19TXD
3	I <sub>PD</sub>	P8RXD	40	I <sub>PU</sub>	P19RXD
4	I/O <sub>PD</sub>	P9TXD/LED mode[1]	41	I/O <sub>PU</sub>	SYNC_16_23/MS_Test[1]
5	I <sub>PU</sub>	P9RXD	42	O <sub>PU</sub>	P20TXD
6	O <sub>PU</sub>	P10TXD	43	P	DVDD
7	I <sub>PD</sub>	P10RXD	44	G	DGND
8	O <sub>PD</sub>	P11TXD/DisBCSFC	45	I <sub>PD</sub>	P20RXD
9	I <sub>PD</sub>	P11RXD	46	O <sub>PD</sub>	P21TXD
10	P	DVDD	47	I <sub>PD</sub>	P21RXD
11	I/O <sub>PD</sub>	SYNC_8_15/EnBRDCTRL	48	O <sub>PD</sub>	P22TXD
12	O <sub>PD</sub>	P12TXD	49	I <sub>PD</sub>	P22RXD
13	I <sub>PD</sub>	P12RXD	50	P	VDD
14	P	DVDD	51	O <sub>PD</sub>	P23TXD
15	P	RVDD	52	I <sub>PD</sub>	P23RXD
16	P	VDD	53	O <sub>PD</sub>	REFCLK_16_23
17	O	VCTRL	54	P	DVDD
18	G	GND	55	G	DGND
19	P	RVDD	56	I	XI/OSCI
20	O <sub>PD</sub>	P13TXD	57	O	XO
21	I <sub>PD</sub>	P13RXD	58	G	AVSS
22	O <sub>PD</sub>	P14TXD	59	P	AVDD
23	I <sub>PD</sub>	P14RXD	60	P	DVDD
24	O <sub>PD</sub>	P15TXD	61	O <sub>PU</sub>	SCAN_LEDC5
25	P	DVDD	62	O <sub>PU</sub>	SCAN_LEDC4
26	G	DGND	63	O <sub>PU</sub>	SCAN_LEDC3
27	I <sub>PD</sub>	P15RXD	64	O <sub>PU</sub>	SCAN_LEDC2
28	O <sub>PD</sub>	REFCLK_8_15	65	O <sub>PU</sub>	SCAN_LEDC1
29	O <sub>PD</sub>	P16TXD	66	O <sub>PU</sub>	SCAN_LEDC0
30	I <sub>PD</sub>	P16RXD	67	O <sub>PU</sub>	SCAN_STSC3
31	O <sub>PD</sub>	P17TXD	68	O <sub>PU</sub>	SCAN_STSC2
32	P	DVDD	69	O <sub>PU</sub>	SCAN_STSC1
33	G	DGND	70	G	DGND
34	I <sub>PD</sub>	P17RXD	71	P	DVDD
35	P	VDD	72	O <sub>PU</sub>	SCAN_STSC0
36	G	GND	73	P	VDD
37	O <sub>PU</sub>	P18TXD	74	G	GND

Pin No.	Type	Pin Name
75	O <sub>PU</sub>	SCAN_LEDB5
76	O <sub>PD</sub>	SCAN_LEDB4
77	O <sub>PD</sub>	SCAN_LEDB3
78	O <sub>PD</sub>	SCAN_LEDB2
79	I/O <sub>PD</sub>	SCAN_LEDB1/MaxPauseCnt
80	O <sub>PU</sub>	SCAN_LEDB0
81	O <sub>PU</sub>	SCAN_STSB3
82	O <sub>PU</sub>	SCAN_STSB2/ LED_EnTRUNK#5
83	G	DVDD
84	O	EnTESTMODE
85	O <sub>PU</sub>	SCAN_STSB1/LED_Loop_Det
86	O <sub>PU</sub>	SCAN_STSB0/ LED_EnTRUNK#4
87	I/O <sub>PD</sub>	SCAN_LEDA5/MaxPktLen
88	I/O <sub>PD</sub>	SCAN_LEDA4/EnCtrlFilter
89	I/O <sub>PU</sub>	SCAN_LEDA3/DisBKP48One
90	P	VDD
91	G	GND
92	O <sub>PU</sub>	SCAN_LEDA2/LED_EnTRUNK#3
93	O <sub>PU</sub>	SCAN_LEDA1/LED_EnTRUNK#2
94	O <sub>PU</sub>	SCAN_LEDA0/LED_EnTRUNK#1
95	O <sub>PU</sub>	SCAN_STSA3/LED_EnTRUNK#0
96	P	DVDD
97	G	DGND
98	O <sub>PU</sub>	SCAN_STSA2/SLED_DMODE_CLK
99	O <sub>PU</sub>	SCAN_STSA1/SLED_DATA
100	O <sub>PU</sub>	SCAN_STSA0/SLED_CLK
101	I/O <sub>PU</sub>	SCK
102	I/O <sub>PU</sub>	SDA
103	I <sub>PU</sub>	RESET#
104	O <sub>PU</sub>	MDC
105	I/O <sub>PU</sub>	MDIO
106	O <sub>PL</sub>	P0TXD/OPCLK2
107	I <sub>PL</sub>	P0RXD
108	O <sub>PL</sub>	P1TXD/OPCLK1
109	I <sub>PL</sub>	P1RXD
110	O <sub>PL</sub>	P2TXD/OPCLK0
111	I <sub>PU</sub>	P2RXD
112	P	DVDD
113	G	DGND
114	P	VDD
115	G	GND
116	I/O <sub>PU</sub>	P3TXD/EnBKP
117	I <sub>PU</sub>	P3RXD

Pin No.	Type	Pin Name
118	I/O <sub>PU</sub>	SYNC_0_7/GAN_Test
119	I/O <sub>PD</sub>	P4TXD/EnCOLBKPmode
120	I <sub>PD</sub>	P4RXD
121	O <sub>PD</sub>	P5TXD
122	I <sub>PD</sub>	P5RXD
123	I/O <sub>PU</sub>	P6TXD/EnFDFC
124	I <sub>PD</sub>	P6RXD
125	I/O <sub>PD</sub>	P7TXD/EnHomeVLAN
126	I <sub>PD</sub>	P7RXD
127	O <sub>PU</sub>	REFCLK_0_7
128	P	DVDD

## 7. Pin Descriptions

Type codes used: P = Power; G = Ground, I = Input, O = Output, Pu = Internal pull up (40K ohm), Pd = Internal pull down (40K ohm).

### 7.1. *SMII Interface*

**Table 2. SMII Interface**

Pin Name	Type	Pin No.	Description
P0TXD	O	106	SMII Transmit Data Output:
P1TXD		108	SMII transmit data is formed in 10-bit serial words. Each word contains one
P2TXD		110	data byte (two nibbles of 4B coded data) and two
P3TXD		116	status bits.
P4TXD		119	The SMII operates at 125MHz using a global reference clock
P5TXD		121	(REFCLK) and frame synchronization signal (SYNC).
P6TXD		123	
P7TXD		125	SMII transmit data is input on these pins, where:
P8TXD		2	Ports 0~7 transmit data is sent synchronously to SYNC_0_7
P9TXD		4	and REFCLK_0_7.
P10TXD		6	
P11TXD		8	Ports 8~15 transmit data is sent synchronously to SYNC_8_15
P12TXD		12	and REFCLK_8_15.
P13TXD		20	
P14TXD		22	Ports 16~23 transmit data is sent synchronously to SYNC_16_23
P15TXD		24	and REFCLK_16_23.
P16TXD		29	
P17TXD		31	
P18TXD		37	
P19TXD		39	
P20TXD		42	
P21TXD		46	
P22TXD		48	
P23TXD		51	

Pin Name	Type	Pin No.	Description		
P0RXD	I	107	SMII Receive Data Input: SMII receive data is input on these pins. Where:  Ports 0~7 receive data is received synchronously to SYNC_0_7 and REFCLK_0_7.  Ports 8~15 receive data is received synchronously to SYNC_8_15 and REFCLK_8_15.  Ports 16~23 receive data is received synchronously to SYNC_16_23 and REFCLK_16_23.		
P1RXD		109			
P2RXD		111			
P3RXD		117			
P4RXD		120			
P5RXD		122			
P6RXD		124			
P7RXD		126			
P8RXD		3			
P9RXD		5			
P10RXD		7			
P11RXD		9			
P12RXD		13			
P13RXD		21			
P14RXD		23			
P15RXD		27			
P16RXD		30			
P17RXD		34			
P18RXD		38			
P19RXD		40			
P20RXD		45			
P21RXD		47			
P22RXD		49			
P23RXD	52				
SYNC_0_7 SYNC_8_15 SYNC_16_23	O	118 11 41	SMII Synchronization Output. SMII transmit/receive data 10-bit word frame synchronization. Where: SYNC_0_7 synchronizes data for ports 0~7. SYNC_8_15 synchronizes data for ports 8~15. SYNC_16_23 synchronizes data for ports 16~23.		
REFCLK_0_7 REFCLK_8_15 REFCLK_16_23		O		127 28 53	SMII Reference Clock Output. The SMII reference clock output is a 125MHz +/- 50ppm clock used to synchronize the SMII data. Ports 0~7 data is sent or received synchronously to SYNC_0_7. Ports 8~15 data is sent or received synchronously to SYNC_8_15. Ports 16~23 data is sent or received synchronously to SYNC_16_23.

## 7.2. Serial Management Interface (SMI)

**Table 3. Serial Management Interface (SMI)**

Pin Name	Type	Pin No	Description
MDC	O (Pu)	104	Serial Management Data Clock (MDC). MDC typically operates at 730KHz. MDC is in tri-state when RST# is active low.
MDIO	IO (Pu)	105	Serial Management Data Input/Output. MDIO is in tri-state when RST# is active low.

## 7.3. Serial EEPROM Interface

**Table 4. Serial EEPROM Interface**

Pin Name	Type	Pin No	Description
SCK	IO (Pu)	101	Serial EEPROM Interface Clock Output/ Serial CPU Access Clock Input. SCLK acts as an output pin after hardware reset for EEPROM read access. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then the SCLK will act as an input pin driven by an external CPU to access the RTL8324 internal registers. SCLK Frequency: Output: Operates at 100KHz Input: Max limit: 10MHz
SDA	IO (Pu)	102	Serial EEPROM Data Input/Output/Serial CPU Access Data Input/Output. After power on, this pin is EEPROM serial data IO. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then this pin acts as a serial CPU data IO.

## 7.4. System Pins

**Table 5. System Pins**

Pin Name	Type	Pin No	Description
RESET#	I (Pu)	103	System Reset. Active low to reset the system to a known state. After power-on reset (low to high), the configuration modes from Mode Control Pins (page 11) are strapped and determined.
XI/OSCI	I	56	Crystal Input/Oscillator Input. This is a 25Mhz +/-50 ppm crystal input or oscillator input. When crystal is used, a capacitor connected from this pin to ground is recommended.
XO	O	57	Crystal Output. When crystal is used, a capacitor connected from this pin to ground is recommended. When an oscillator is used, keep this pin floating.

## 7.5. Mode Control Pins

The Mode Control pin values are strapped on power on reset. The strapped values may be updated via EEPROM configuration if it exists. They can also be modified by internal register access from the CPU interface.

**Table 6. Mode Control Pins**

Pin Name	Pin No.	Type	Description
MaxPktLen (SCAN_LED5)	87	I/O (P-down)	Max. Valid Packet Length Control. 0: 1536 bytes (Default) 1: 1552 bytes
MaxPauseCnt (SCAN_LED1)	79	I/O (P-down)	Max Pause frame Count for Congestion Control. 0: 128 (Default) 1: Continuous
EnCOLBKmode (P4TXD)	119	I/O (P-down)	Enable Carrier-Based Back Pressure Mode. Half duplex back pressure flow control algorithm selection. 0: Carrier-based back pressure mode (Default) 1: Collision-based back pressure mode
EnCtrlFilter/ (SCAN_LED4)	88	I/O (P-down)	Enable 802.1D Specified Reserved Control Frame Filtering. When network control frames are received with the destination MAC address as the group MAC address: (01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F), the switch will drop the frames if the EnCtrlFilter=1. If EnCtrlFilter=0 the frames will be flooded. 0: Disable Filtering (Default) 1: Enable Filtering
EnHomeVLAN (P7TXD)	125	I/O (P-down)	Enable Home-VLAN Configuration. When enabled, the switch will be configured in Home-VLAN mode. The “Home-VLAN topology” is shown below: 0: Disable Home-VLAN Function (Default) 1: Enable (set VLAN as 22 VLANs with 2 overlapping port).
EnFDFC (P6TXD)	123	I/O (P-up)	Global Disable Full Duplex 802.3x Pause Flow Control Ability. Globally disables the 802.3x Pause ability flow control of all ports. 1: Enable 802.3x Pause flow control ability (Default) 0: Disable 802.3x Pause flow control ability
EnBKP (P3TXD)	116	I/O (P-up)	Global Disable Half Duplex Back Pressure Flow Control Ability. Globally disables the back pressure flow control ability of all ports. 1: Enable back pressure flow control ability (Default) 0: Disable back pressure flow control ability
EnBKP48One (SCAN_LED3)	89	I/O (P-up)	Enable Back Pressure 48 Pass One Algorithm. When the 48 Pass One algorithm is enabled, the switch will pass one incoming packet for every 48 collisions. 0: Disable 48 Pass One algorithm 1: Enable 48 Pass One algorithm (Default)

Pin Name	Pin No.	Type	Description
DisBCSFC (P11TXD)	8	I/O (P-down)	<p>Disable Broadcast Packet Strict Flood Control.</p> <p>Set to enable broadcast packet (DA: 'FF-FF-FF-FF-FF-FF') strict flood mode and configure to loose flood mode.</p> <p>Strict flood mode will drop all broadcast packets if any destination port is congested.</p> <p>Loose flood mode allows broadcast packets to be flooded to all non-congested ports.</p> <p>0: Enable Broadcast Packet Strict Flood (Strict flood mode) (Default) 1: Disable Broadcast Packet Strict Flood (Loose flood mode)</p>
EnBRDCTRL (SYNC_8_15)	11	I/O (P-down)	<p>Broadcast Storm Filtering Control.</p> <p>Enable broadcast storm filtering control.</p> <p>0: Disable Broadcast storm filtering control (Default) 1: Enable Broadcast storm filtering control</p>
LED mode[1:0] P9TXD P8TXD	4 2	I/O (P-down, P-up)	<p>00: Scan LED mode.</p> <p>01: Serial LED mode (single color) (default)</p> <p>10: Serial LED mode (bi-color)</p> <p>11: Reserved</p>



## 7.6. LED Pins

### 7.6.1. Scan LED Pins

**Table 7. Scan LED Pins**

Pin Name	Pin No.	Type	Description
Port 0_7 Scan_LED Group		I/O	Scan LED pins display for port0~port7 link status. In Scan LED mode, this LED group display each port's (1)Speed (2) Link/Active (3) Collision/Duplex status without external TTL.
SCAN_LED A5	87		
SCAN_LED A4	88		
SCAN_LED A3	89		
SCAN_LED A2	92		
SCAN_LED A1	93		
SCAN_LED A0	94		
SCAN_STSA3	95		
SCAN_STSA2	98		
SCAN_STSA1	99		
SCAN_STSA0	100		
Port 8_15 Scan_LED Group		I/O	Scan LED pins display for port8~port15 link status. In Scan LED mode, this LED group display each port's (1) Speed (2) Link/Active (3) Collision/Duplex status without external TTL.
SCAN_LED B5	75		
SCAN_LED B4	76		
SCAN_LED B3	77		
SCAN_LED B2	78		
SCAN_LED B1	79		
SCAN_LED B0	80		
SCAN_STSB3	81		
SCAN_STSB2	82		
SCAN_STSB1	85		
SCAN_STSB0	86		
Port 16_23 Scan_LED Group		I/O	Scan LED pins display for port16~port23 link status. In Scan LED mode, this LED group display each port's (1) Speed (2) Link/Active (3) Collision/Duplex status without external TTL.
SCAN_LED C5	61		
SCAN_LED C4	62		
SCAN_LED C3	63		
SCAN_LED C2	64		
SCAN_LED C1	65		
SCAN_LED C0	66		
SCAN_STSC3	67		
SCAN_STSC2	68		
SCAN_STSC1	69		
SCAN_STSC0	72		

## 7.6.2. Serial LED Pins

**Table 8. Serial LED Pins**

Pin Name	Pin No.	Type	Description
SLED_CLK (SCAN_STSA0)	100	O	Serial LED Shift Clock. In Serial LED mode, when Serial LED mode is enabled, periodically active to enable SLED_DATA to shift into the external shift register.
SLED_DATA (SCAN_STSA1)	99	O	Serial LED Data Output. In Serial LED mode, when Serial LED mode is enabled, serial LED data is shifted out when SLED_CLK is active.
SLED_DMODE _CLK (SCAN_STSA2)	98	I	Serial LED Diagnostic Mode Item Select Control Pulse Input. This is an external signal pulse input signal for diagnostic item selection. The diagnostic LED display item will change whenever there is a signal pulse clock input on this pin. The diagnostic items list and its display sequence is as follows: (1) DisablePort/RxError (active low) On: Port disabled Blinking: Error Packet Received (includes dropped packets) (2) FlowControl/FCActive (active low) On: Flow control ability enabled Blinking: Congestion flow control active (3) TrunkPort/TKFault (active low) On: Trunk Port Blinking: Trunk link fault port (4) HighPriorityPort (active low) On: High priority port (5) LoopDetectPort (active low) On: Loop event detected. (6) BroadcastStormAlarmPort (active low) On: Broadcast Storm detected (7) Reserved (8) Reserved

Pin Name	Pin No.	Type	Description
LED_EnTRUNK#0 (SCAN_STSA3)	95	O	Trunk Port Enabled LED output. 0 (On): Trunk Enabled 1 (Off): Trunk Disabled.
LED_EnTRUNK#1 (SCAN_LEDA0)	94		The LED blinks to indicate that there is a trunk member port link down. For Serial LED Mode: act as Trunk 0 (port 0~3) Enable LED.
LED_EnTRUNK#2 (SCAN_LEDA1)	93		For Serial LED Mode: act as Trunk 1 (port 4~7) Enable LED. For Serial LED Mode: act as Trunk 2 (port 8~11) Enable LED.
LED_EnTRUNK#3 (SCAN_LEDA2)	92		For Serial LED Mode: act as Trunk 3 (port 12~15) Enable LED. For Serial LED Mode: act as Trunk 4 (port 16~20) Enable LED.
LED_EnTRUNK#4 (SCAN_STSB0)	86		For Serial LED Mode: act as Trunk 5 (port 21~24) Enable LED.
LED_EnTRUNK#5 (SCAN_STSB2)	82		
LED_Loop_Det (SCAN_STSB1)	85	O	For Serial LED mode: act as Loop detect for global port. Loop Detect LED output. 0: Loop detected 1: Loop not detected

## 7.7. Power/Ground Pins

**Table 9. Power/Ground Pins**

Pin Name	Pin No	Type	Description
DVDD	10, 14 25, 32 43, 54 60, 71 83, 96, 112, 128	3.3V(I)	3.3V for I/O digital power.
DGND	1, 26 33, 44 55, 70 97, 113	GND	GND for I/O.
RVDD	15 19	3.3V(I)	3.3V for internal 3.3V to 1.8V regular power input.
VDD	16, 35 50, 73 90, 114	1.8V(I)	1.8V input for internal test used. Do not supply 1.8V if RVDD is used.
GND	18, 36 74, 91 115	GND	GND for Core power.

Pin Name	Pin No	Type	Description
VCTRL	17	1.8V(o)	Voltage control: This pin controls a PNP transistor to generate the 1.8V power supply for VDD pins. Normally keep this pin floating.
AVDD	59	3.3V(I)	3.3V for PLL power.
AVSS	58	GND	GND for PLL.

## 7.8. Test Pins

**Table 10. Test Pins**

Pin Name	Pin No.	Type	Description
EnTESTMODE	84	I/O (Pd)	Test pin. Normally not pulled up or down.
MS_Test[1]	41	I/O (P-Up)	Must use 1K resistor to pull up to 3.3V.
GAN_Test (SYNC_0_7)	118	I/O	Must use 1K resistor to pull up to 3.3V.
OPCLK2 (P0TXD)	106	I/O (P-down)	Test pin. Normally not pulled up or down.
OPCLK1 (P1TXD)	108	I/O (P-down)	Test pin. Normally not pulled up or down.
OPCLK0 (P2TXD)	110	I/O (P-down)	Test pin. Normally not pulled up or down.

## 8. Functional Description

### 8.1. *Reset*

#### 8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse (44ms) will be generated and the RTL8324 will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the RST# signal
- Auto load the configuration from EEPROM if EEPROM is detected (approx. 10ms)
- Complete the embedded SSRAM BIST process (approx. 24 ms)
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the serial CPU interface
- Start MDC/MDIO configuration and polling

*Note 1: To guarantee register access is valid and correct, the RTL8324 registers should not be accessed before the reset initialization process is finished.*

*Note 2: The connected PHY should have completed the reset process before the RTL8324 starts the MDC/MDIO configuration and polling process.*

#### 8.1.2. Software Reset

The software reset command resets the system control circuit and restarts auto-negotiation. It keeps the user configured settings. Hardware pin strapping, EEPROM auto load, and SSRAM BIST are NOT done when using the software reset command.

### 8.2. *MAC to PHY Interface*

The MAC to PHY interface supports SMII for all ports.

### ***8.3. Fast Ethernet Port (SMII Interface)***

Ports 0~23 are 10/100M Fast Ethernet ports supporting a Serial Media Independent Interface (SMII). The RTL8324 provides three SMII synchronous 125MHz clock outputs for three octal PHYs.

### ***8.4. MAC Address Table Search and Learning***

The RTL8324 MAC address lookup table consists of an 8K-entry hash table and 64-entry Content Addressable Memory (CAM). The RTL8324 uses the last 13 bits of the MAC address to index the 8K-entry lookup table for address searching and learning. If the mapped location in the 8K entries is occupied, then the RTL8324 will compare the destination MAC address with the contents of the CAM for address searching, and store the source MAC address in the CAM for address learning. The 64-entry CAM helps avoid address hash collisions and improves switch performance.

### ***8.5. MAC Table Aging Function***

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if it is not updated by the address learning process within a set aging time period. The default aging timer of the MAC address lookup table is between 200 ~ 300 seconds.

### ***8.6. Illegal Frame Filtering***

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded. The maximum packet length may be 1536 or 1552 bytes.

This function is controlled by register 0x0001 [1:0].

Hardware Strapping Pin: MaxPKLen (87).

### ***8.7. IEEE 802.1D Reserved Group Addresses Filtering Control***

The RTL8324 supports the ability to drop 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-04 to 01-80-C2-00-00-0F. The default setting disables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered. MAC address 01-80-C2-00-00-03 is not filtered.

This function is controlled by register 0x0300 [2].

Hardware Strapping Pin: EnCtrlFFilter (88).

### ***8.8. Backoff Algorithm***

The RTL8324 implements the truncated exponential backoff algorithm compliant with the IEEE 802.3 standard. The collision counter is restarted after 16 consecutive collisions.

## 8.9. *Inter-Packet Gap*

The Inter-Packet Gap is 9.6 $\mu$ s for 10Mbps Ethernet, 960ns for 100Mbps Fast Ethernet.

The RTL8324 supports Transmit Inter-Packet Gap compensation for the frequency shift tolerance of the on-board oscillator.

This function is controlled by register 0x0001 [2].

## 8.10. *Buffer Management*

An embedded 1.25Mbit SSRAM is built-in as a packet storage buffer. To efficiently utilize the packet buffer, the RTL8324 divides the SSRAM into 1280 x 128-byte page-based buffers that are linked by a descriptor link list. For an Ethernet packet, a minimum of one, and maximum of 12 pages can be used. The system supports non-blocking wire-speed switching via 24 10/100M ports.

## 8.11. *Flow Control*

The RTL8324 supports IEEE 802.3x full-duplex flow control, and half-duplex back pressure congestion control.

### 8.11.1. **IEEE 802.3x Pause Flow Control**

IEEE 802.3x flow control is auto-negotiated between the remote device and the RTL8324 by writing the flow control ability, via MDIO, to an external connected PHY.

If a good PAUSE frame is received from any PAUSE flow-control-enabled port with DA=0180C2000001, the corresponding port of the RTL8324 will stop its packet transmission until a PAUSE timer timeout, or another PAUSE frame with zero PAUSE time is received.

The maximum transmitted Pause frame count during a congestion event is controllable. (1) limited to a 128 count (2) unlimited count. The limited count is used to avoid unexpectedly long pause time locks for some network topology traffic.

This function is controlled by register 0x0001 [3].

Hardware Strapping Pin: MaxPauseCnt (79).

### 8.11.2. Half Duplex Back Pressure Flow Control

The RTL8324 supports two back pressure flow control schemes to force incoming packet backoff when the switch destination port is congested. This back pressure mode is controlled by register 0x0001 [7] and Hardware Strapping Pin: EnCOLBKPMODE (119).

**Collision-based back pressure:** Uses a 4-byte jam pattern to force collisions with each incoming packet to force the link partner to back off transmissions according to CSMA/CD until the destination port congestion event is cleared. The RTL8324 uses a special half-duplex back pressure design; after 48 forced collisions it unconditionally receives and forwards one packet successfully. This prevents the connected repeater from being partitioned due to excessive collisions.

**Carrier-sense-based back pressure:** When a congested event is asserted, the RTL8324 continuously sends 4k jam packets with a minimum Inter-Packet Gap to prevent the link partner from transmitting more packets.

### 8.12. Broadcast Storm Filtering Control

The Broadcast Storm Filtering Control function enables each port to drop broadcast packets (Destination MAC ID is ‘ff ff ff ff ff ff’) after a *continuous received broadcast packets counter* count of 64. The counter is reset to 0 every 800ms or when receiving non-broadcast packets (Destination MAC ID is not ‘ff ff ff ff ff ff’).

This Broadcast Storm Filtering Control function is controlled by register 0x0607 [4].

Hardware Strapping Pin: EnBRDCTRL (11).

### 8.13. Head-Of-Line Blocking Prevention

The RTL8324 incorporates a simple mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8324 first checks the destination address of an incoming packet. If the destination port is congested, then the RTL8324 discards this packet to avoid blocking following packets destined for a non-congested port.



## ***8.14. Port Trunking and Fault Recovery Support***

Port Trunking is the ability to aggregate several 10/100Mbps ports into a single logical link. There are 6 trunk groups supported by the RTL8324. They are identified as:

Trunk 0: (Port 0, 1, 2, 3)

Trunk 1: (Port 4, 5, 6, 7)

Trunk 2: (Port 8, 9, 10, 11)

Trunk 3: (Port 12, 13, 14, 15)

Trunk 4: (Port 16, 17, 18, 19)

Trunk 5: (Port 20, 21, 22, 23)

They are individually enabled by Register 0x0307[6:1], EnTrunk[5:0] during hardware reset. Each trunk supports a trunking port status LED. The LED will be active low when the trunking function is enabled.

The RTL8324 trunking port always sends packets over the same link path in the trunk with a given source and destination MAC address to prevent frames from getting out of order, but the reverse path may follow a different link.

### **8.14.1. Load Balancing**

The load balancing scheme between links in a trunk group is determined by an Index[2:0] value that is calculated by a DA and SA hash algorithm.

Mapping algorithm. Given a number between 8 values of Index[2:0]:

If link up port is 4. Index value {(7, 6), (5, 4), (3, 2), (1, 0)} maps to LinkUpPort[3:0]

If link up port is 3. Index value {(7, 6, 5), (4, 3, 2), (1, 0)} maps to LinkUpPort[2:0]

If link up port is 2. Index value {(7, 6, 5, 4), (3, 2, 1, 0)} maps to LinkUpPort[1:0]

If link up port is 1. Index value {(7, 6, 5, 4, 3, 2, 1, 0)} maps to LinkUpPort[0]

### **8.14.2. Trunk Fault Auto Recovery**

If a physical port of a trunk group is link down, then the EnTrunkLED will blink to warn of a link-down fault event. The Fault flag will be reported on register 0x0102 (System Fault Indication Register).

The RTL8324 will auto-start the Auto Fault Recovery scheme to distribute the trunk load to the remaining link up ports.

## 8.15. IGMP Snooping Support

The RTL8324 supports ASIC-based IGMP (Internet Group Management Protocol) snooping. This can be enabled via register 0x0308[0]. No other external CPU handling is required. It supports the ability to parse the IGMP control protocol packets and IP multicast data packets and learn the multicast router port and group address member ports into the multicast address table.

The RTL8324 differentiates between IGMP control protocol packets according to the message type:

- Router protocol packets (IGMP query packets and multicast routing protocol packets) are broadcast to all ports
- Group member protocol packets (IGMP v1, v2, Report and Leave packets) are sent directly to multicast router ports

IP multicast data packets involve multicast group table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to all member ports and router ports. If the multicast address is not stored in the address table (i.e. lookup miss), the packet is broadcast to all ports of the broadcast domain.

The multicast table is combined with a L2 MAC table with a maximum of 8k entries. For a given multicast entry, the valid port member bit will auto age out after about 5 minutes if the port does not receive a corresponding group address IGMP report packet.

## 8.16. VLAN Function

The RTL8324 supports a VLAN function to segregate the switch into 32 VLANs. Each VLAN is a broadcast domain and each VLAN may be flexibly configured from 0 to 24 port members. Both port-based and tag-based VLAN functions are supported. The PVID, Tagging Control, and Ingress/Egress rules are manually configured on the VLAN Table at registers 0x030B~0x037C. The VLAN table format is shown as follows:

**Table 11. VLAN Table Format**

VLAN Entry Index	VID (12-Bit)	Port Member Set (26-bit Bitmap)
0		
1		
2		
:		
31		

‘VID’ defines the 802.1Q VLAN ID. The value of ‘VID’ may NOT be ‘0x000’ or ‘0xfff’.

A VLAN is used to divide the broadcast domain to cut broadcast scope. The VLAN Frame Forwarding Rules are defined as follows:

- A received broadcast/multicast frame will be flood forwarded to VLAN member ports only ('Port Member Set' in the VLAN table) of the VLAN except the source port.
- A received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded unless Leaky VLAN control is enabled.
- All VLAN groups share the same layer-2 learned MAC address table (Shared Learning).

### **8.16.1. Port-Based VLAN**

By setting the 0x030B register to disable the En8021Qaware control bit, port-based VLAN is enabled and 802.1Q VLAN tagging is ignored. All other VLAN table configurations are the same as tag-based VLAN functions. The VLAN classification of an incoming packet on a port-based VLAN is defined by the port PVID. The RTL8324 uses the Port VLAN Identifier (PVID) to search the VLAN table for the VLAN member.

### **8.16.2. IEEE 802.1Q Tag-Based VLAN**

By setting the 0x030B register to enable the En8021Qaware control bit, 802.1Q tag-based VLAN is enabled.

VLAN classification is the first step before VLAN table lookup. The method of assigning a unique VID value to a received packet is as follows:

1. For a VLAN-tagged packet.

If the tagged 12-bit VID  $\neq 0$ , then the tagged VID value is used.

If the tagged VID = 0 (Null VID, priority tag), then the port's PVID value is used.

2. For a non-VLAN-tagged packet, the port's 12-bit PVID value is used.

*Note: The 'insert PVID' function for non-VLAN-tagged packets is controlled by registers 0x037D~0x037E).*

After a unique 12-bit VID is assigned, the RTL8324 checks the VLAN table ingress/egress rule, and then forwards the packet to valid destination ports.

### **8.16.3. Ingress/Egress Filtering Control Parameters**

Two VLAN filtering rule control parameters are provided on register 0x030B:

- Acceptable frame type control: Admits all frames or admits only VLAN-tagged frames
- Ingress filtering control: Enables filtering of frames received from a port that is not in this port's VLAN group

#### 8.16.4. Leaky VLAN

The Leaky VLAN feature enables specific frames to be forwarded between different VLANs.

For example, if the VLAN table entry is:

VLAN 1: Port members = {Port 1, 2, 3}

VLAN 2: Port members = {Port 4, 5, 6}

Normally, broadcast, multicast, and unicast packets are not allowed to be switched between these two VLANs. Port 1 broadcast packets will only flood to Port 2 and 3. A Port 1 unicast packet is not allowed to be forwarded to a member of VLAN 2.

If the Leaky VLAN function is enabled, three types of packets may be forwarded to destination ports outside the current VLAN.

1. Unicast Packet: May be forwarded to a destination port (L2 table lookup hit) on a different VLAN
2. ARP Broadcast Packet: May be broadcast to all ports on a switch
3. IP Multicast Packet: May be flooded to all the multicast address group member set, ignoring the VLAN member set domain limitation

These types of leaky control are used when:

- A switch is divided into multiple VLANs and host to host communication is required between the different VLANs without using a router
- You want to improve router performance

#### 8.16.5. Insert/Remove VLAN Priority Tag

The RTL8324 supports Output Priority tagging control via register set 0x0319~0x031B. There are four types of VLAN tagging:

1. Remove the VLAN tag from all tagged packets
2. Insert a priority tag into untagged high-priority packets (Set priority field: 7, VID field: 0 for high priority packets)
3. Insert a priority tag into all untagged packets (Set priority field: 7, VID field: 0 for high priority packet. Set priority field: 0, VID field: 0 for low priority packets)
4. Don't touch (No modification made to the packet)

*Note: This function may be enabled whether the VLAN function is enabled or not.*

## **8.17. QoS Function**

The RTL8324 can recognize QoS priority information in an incoming packet and send the packet to different priority queues for different service priority. The RTL8324 identifies the packet's priority based on three types of QoS priority information:

1. Port-based priority
2. IEEE 802.1p/Q VLAN tag
3. TCP/IP TOS/DiffServ (DS) priority field

These three types of QoS can be configured via hardware pins, EEPROM, or Registers 0x0400 ~ 0x0402.

The RTL8324 supports two priority level queues. The queue service rate is based on the Weighted Round Robin algorithm. The packet-based service weight ratio of high-priority and low-priority queuing can be set to 4:1, 8:1, 16:1 or 'Always high priority first'.

### **8.17.1. Port-Based Priority**

When port-based priority is applied, any packet received from a high priority port will be treated as a high priority packet.

### **8.17.2. IEEE 802.1p/Q-Based Priority**

When 802.1p tag priority is applied, the RTL8324 recognizes 802.1Q VLAN tagged packets and extracts the 3-bit User Priority information from the VLAN tag. The RTL8324 sets the User Priority threshold to 3. VLAN tagged packets with User Priority values 4~7 are treated as high priority packets, and other User Priority values (0~3) as low priority packets (follows the IEEE 802.1p standard).

### 8.17.3. Differentiated Services Based Priority

When TCP/IP's TOS/DiffServ (DS) based priority is applied, the RTL8324 recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for IPv4 is the Type-of-Service (TOS) octet. Recommended DiffServ Codepoints are defined in RFC2597 for classifying traffic into different service classes. The RTL8324 extracts the codepoint value of the DS field from IPv4 packets and identifies the priority of the incoming IP packet following the definitions listed below:

High Priority. DS-field = 101110 (EF, Expected Forwarding)

001010; 010010; 011010; 100010 (AF, Assured Forwarding)

11x000 (Network Control)

Low Priority. DS-field = Other values

VLAN tagged packet formats are shown below:

6 bytes	6 bytes	2 bytes	3 bits	1 bit	12 bits		4 bytes
DA	SA	81-00	User Priority (0~3: Low-pri; 4~7: High-pri)	CFI	VLAN Identifier	Data	CRC

**Figure 4. 802.1Q VLAN Tag Frame Format**

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	4 bits	6 bits	2 bits		4 bytes
DA	SA	802.1Q Tag (Optional)	08-00	Version IPv4: 0100	IHL	TOS[0:5]: DS-field	----	Data	CRC

**Figure 5. IPv4 Frame Format**

### 8.17.4. Flow Control Auto Turn Off

The RTL8324 can automatically turn off IEEE 802.3x flow control and back pressure flow control for 1~2 seconds whenever the port receives a high priority packet. Flow control is re-enabled when no priority packets are received for 1~2 seconds. This auto-turn off function is enabled via Register 0x0400[2].

## 8.18. Ingress and Egress Bandwidth Control

The RTL8324 supports bandwidth control on all ports. Each port's bandwidth is configurable on both ingress and egress traffic independently. Port bandwidth may be configured to 128kbps, 256kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, or 8Mbps.

When the ingress or egress traffic bandwidth exceeds the configured threshold, flow control is triggered to limit the throughput. The control description is shown in register 0x020A ~0x0215.

## 8.19. Simple MIB Counter Support

Three 32-bit MIB counters (Counter 1, Counter 2, and Counter 3) are implemented on each port for basic traffic management and diagnostic purposes.

The MIB object of each counter is configurable. The MIB object selection on each counter is shown in Table 12. A detailed description is given in 10.8 MIB Counter Register, page 48.

**Table 12. MIB Object Selection**

MIB Object	Counter 1	Counter 2	Counter 3
RX Packet Count	V	-	-
RX Byte Count	V	-	-
TX Packet Count	-	V	-
TX Byte Count	-	V	-
Drop Packet Count	-	-	V
Drop Byte Count	-	-	V
CRC Error Packet Count	V	V	V
Collision Count	V	V	V

## 8.20. Network Loop Connection Fault Detection

The RTL8324 periodically transmits a Realtek-EtherType (=0x8899) protocol frame to detect network loop faults.

- Normal transmission time interval is five minutes
- If a port detects a loop, the loop event flag will be set (register 0x0101) and the transmission time interval will change to one second to speed up the new topology change detection
- The loop event flag will be cleared and the transmission time interval will return to five minutes if the port does not receive a self-loop detect packet for 3 seconds

### Loop Detect Packet Format

The Loop Detect Packet Format is shown below:

**Table 13. Loop Detect Packet Format**

0	8	16	24	~	32
DA (6) [=0xfffffffffff]					
DA			SA (6)[=Switch MAC]		
SA					
RealtekEtherType (2) [=0x8899]		Protocol (1) [=03]		Pad 0000	
Pad 00000000					
⋮					
⋮					
CRC (4)					



## 8.21. Realtek Echo Protocol

The Realtek Echo Protocol (REP) supports the Layer 2 Echo test. It is easy for a host to do network connection diagnostics through a simple test packet, with or without other hosts on the network. No IP assignment is required.

When the RTL8324 receives a REP packet, it replies by sending the original REP frame to the source MAC address with the DA and SA exchanged.

### Realtek Echo Protocol Frame

The REP frame format is shown below:

0	8	16	24	~	32
DA (6) [=0xffffffff]					
DA			SA (6)[=Switch MAC]		
SA					
RealtekEtherType (2) [=0x8899]		Protocol (1) [=02]		Pad 0000	
Pad 00000000					
:					
:					
CRC (4)					

**Figure 6. Realtek Echo Protocol Frame**

## 8.22. Disable Port

A port can be disabled via the Port Disable Control Register (register 0x0608~0x0609). When a port is disabled, the port will cease all packet transmission and reception. The physical link status is not changed.

## 8.23. Port Properties Configuration

The RTL8324 supports a flexible method to configure port properties via the PHY MII register. Configurable properties include Media Speed (10M/100M), Duplex Mode, and 802.3x PAUSE flow control. The properties of each can be configured by auto-negotiation or forced mode (auto negotiation disabled).

The port link state will be reported in the port Link Status register. The configuration description is shown in registers 0x060A ~ 0x0624.

The following shows how to configure the Pause and Asymmetric Pause ability on port property register (0x060A~0x0615) to get an expected negotiation result.

**Table 14. Configuring Pause and Asymmetric Pause**

PAUSE	Asymmetric PAUSE	Expected PAUSE Result
0	0	Disable
0	1	Asymmetric to Link Partner
1	0	Symmetric(Default)
1	1	Asymmetric to Link Local or Symmetric

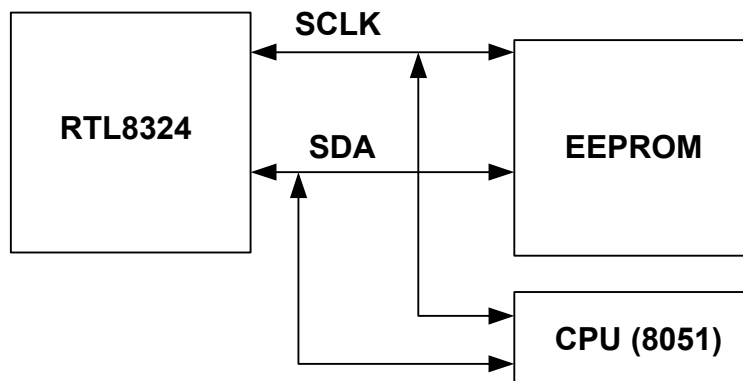
When a port is configured to ‘Forced Mode’ (auto negotiation disabled), the following table shows how to configure flow control ability (TX pause/RX pause) on port property registers (0x060A~0x0615) to get an expected negotiation result.

**Table 15. TX/RX Pause Ability in Forced Mode**

(0x060A~0x0615) bit[6] Asymmetric PAUSE	(0x060A~0x0615) bit[5] Asymmetric PAUSE	RTL8324 Flow Control Ability
0	0	RX pause ability only
0	1	No Flow Control ability
1	0	TX pause ability only
1	1	Both TX/RX pause ability

## 8.24. Serial CPU Interface

The RTL8324 supports a serial CPU interface (Slave mode) that shares the same hardware pin (SCK, SDA) as the EEPROM interface (Master mode). The EEPROM and Serial interface can coexist by assigning a different device ID. Define EEPROM device ID=1010-000, RTL8324 device ID=1010-100. The interface is compatible with EEPROM 24LC04.



**Figure 7. Serial CPU Interface**

The serial CPU interface is enabled after the EEPROM download has finished. When operating in serial CPU mode the SCK is an input pin. The SDA is an IO pin with internal pull high.

### 8.24.1. Serial-CPU Access Format

In Serial CPU mode, 16-bit and 32-bit data access are both supported by the RTL8324. The Serial Read Write access format is as follows.

- 16-bit Address (MSB first)
- 16/32-bit data Burst Read (Low byte (Byte0) first; MSB first)
- 16/32-bit data Burst Write (Low byte (Byte0) first; MSB first)

*Note: Each burst is one byte.*

### Start and Stop Definition (START; STOP)

A high-to-low transition of SDA with SCLK high is a START condition and it must precede any other command.

A low-to-high transition of the SDA line while the clock (SCLK) is HIGH determines a STOP condition. All operations must end with a STOP.

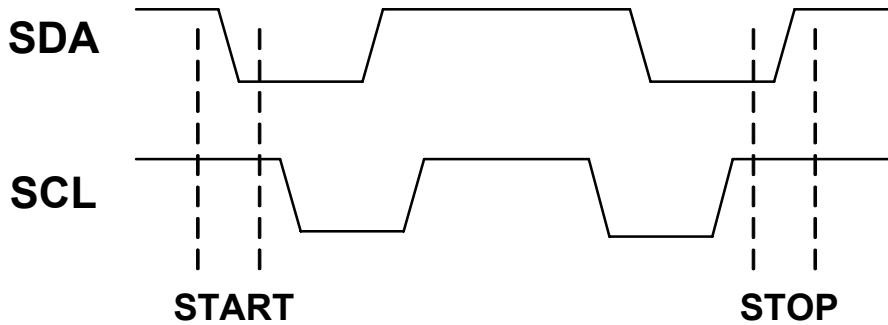


Figure 8. Start and Stop Definition

### Output Acknowledge (ACK)

When addressed, each receiving device is obliged to generate an acknowledgment after reception of each byte.

The master device must generate an extra clock pulse that is associated with this acknowledgement bit.

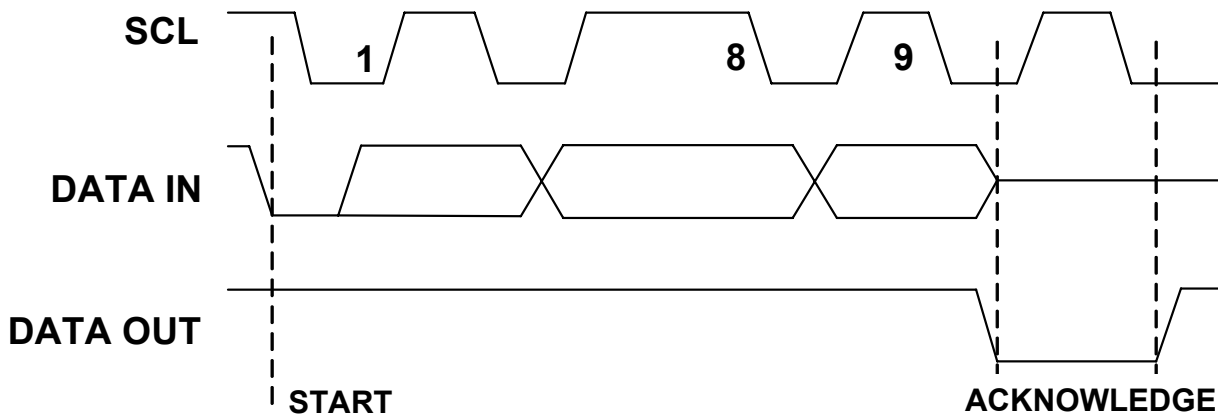


Figure 9. Output Acknowledge (ACK)

### Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

**Serial CPU 16-Bit Read/Write Format**
**Table 16. Serial CPU 16-Bit Read/Write Format**

Bit Width	1	4	3	1	1	8	1	8	1	8	1	8	1	1
Operation	Start Bit	Control code	Chip Select	RW	Ack	Reg. Addr. [7:0] (MSB first)	Ack	Reg. Addr. [15:8] (MSB first)	Ack	Reg. Data. [7:0] (MSB first)	Ack	Reg. Data. [15:8] (MSB first)	Ack	Stop Bit
16-bit Read	Start	1010	100	1	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Read Data	0 (*B)	Read Data	1 (*B)	Stop
16-bit Write	Start	1010	100	0	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Write Data	1 (*A)	Stop

Note: \*A = ACK by RTL8324. \*B = ACK by CPU

**Serial CPU 32-Bit Read Format**
**Table 17. Serial CPU 32-Bit Read Format**

Bit Width	1	4	3	1	1	8	1	8	1	8	1	8	1	8	1	8	1	1
Operation	Start Bit	Control code	Chip Select	RW	Ack	Reg. Addr. [7:0] (MSB first)	Ack	Reg. Addr. [15:8] (MSB first)	Ack	Reg. Data. [7:0] (MSB first)	Ack	Reg. Data. [15:8] (MSB first)	Ack	Reg. Data. [23:16] (MSB first)	Ack	Reg. Data. [31:24] (MSB first)	Ack	Stop Bit
32-bit Read	Start	1010	100	1	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Read Data	0 (*B)	Read Data	0 (*B)	Read Data	0 (*B)	Read Data	1 (*B)	Stop

Note: \*A = ACK by RTL8324. \*B = ACK by CPU

## 8.25. PHY Serial Management Interface

The RTL8324 supports PHY management through the serial MDIO and MDC signal (SMI) to start the auto-negotiation process. After a power-on reset, the RTL8324 writes its abilities to the advertisement registers 0, and 4 of the connected PHY and commands the PHY to restart the auto negotiation process. The PHY device address setting is defined as:

Address 16~31 for Fast Ethernet ports 0~15

Address 8~15 for Fast Ethernet ports 16~23

After restarting auto-negotiation, the RTL8324 will continuously read the link status and abilities of local and link partners to determine the link state.

Port properties (speed, duplex, 802.3x flow control) can be configured via auto-negotiation or force mode. The configuration is described in register 0x060A ~ 0x0615. The final link status is reported in register 0x0619~0x0624.

### 8.25.1. SMI (MDC, MDIO) Interface

#### SMI (MDC, MDIO) Management Packet Format

**Table 18. SMI (MDC, MDIO) Management Packet Format**

		Management Frame Fields							
		PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
<b>Read</b>		1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z
<b>Write</b>		1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z

### 8.25.2. PHY Register Indirect Access

The RTL8324 supports the ability to randomly access PHY registers through a set of control registers at 0x0500~0x0502. Users need to define the PHY address ID, PHY Register ID, Data content of the write command, and operating command type (Read or Write) on the above registers. Then the RTL8324 will auto process the PHY Read/Write access through the MDC/MDIO interface.

#### Read PHY Register Procedure

Configure PHY Access Control Register (0x0500)

Read the result on PHY Access Read Data Register (0x0502)

#### Write PHY Register Procedure

Write the PHY Access Write Data Register (0x0501)

Configure the PHY Access Control Register (0x0500)

#### PHY Address ID Definition

The PHY address ID corresponds to the port location. The PHY address ID of Ports 0~15 are 0x10, 0x11, 0x12 ....., 0x1F, Ports 16~23 are 0x08, 0x09.....0x0F

## 8.26. LED Interfaces

The RTL8324 provides a flexible per-port LED display to show the per-port link status and diagnostic information. Both a parallel and serial interface are provided to drive the LEDs.

During power on reset, the parallel LED signals are driven low and the serial interface shifts to a low value for about two seconds to turn on all the LEDs for testing purposes.

## 8.27. Parallel LED Interface

The parallel interface only provides a system status LED.

LED signals include: LED\_loopDet, LED\_EnTrunk[5:0].

## 8.28. Serial LED Interface

The serial interface, SLED\_CLK, and SLED\_DATA provide clock and data to enable the external shift registers 74164 to capture the per-port link status and diagnostic information.

Another pin, LED\_DMODE\_CLK, provides the diagnostic items selection control. Each pulse signal input from this pin changes the diagnostic item to be displayed on the diagnostic LED.

Each port provides three port-state LEDs (StateLED) and one diagnostic LED (DiagLED). The LED display type can be flexibly configured and can be enabled or disabled to achieve the optimal BOM cost.

The LED display configuration is controlled by register 0x0005h ‘LED Display Configuration Register’, and can also be configured via EEPROM.

The StateLED display is defined by StatLED\_mode[2:0] on register 0x0005. The available display types are shown in the following table.

**Table 19. Serial LED Interface**

StatLEDn_mode[2:0]	000	001	010	011	100	101	110	111
StateLEDn Display Type	Link /Act	100Spd	Duplex /Col	Link/Act /100Spd	Duplex	Act	Link	Col

The display items of the diagnostic LED (DiagLED) are internally defined and are as follows:

**Table 20. Diagnostic LED Display**

Item	Description
(DiagItem_0) DisablePort/RxError	ON: Disabled port Blinking: RX CRC error
(DiagItem_1) FlowControl/FCActive	ON: Flow control enabled Blinking: Flow control active
(DiagItem_2) TrunkPort/TKFault	ON: Trunking enabled port Blinking: Trunk fault warning
(DiagItem_3) HighPriorityPort	ON: High priority port
(DiagItem_4) LoopDetectPort	ON: Network loop connection fault detect
(DiagItem_5) BroadcastStormAlarmPort	ON: Broadcast Storm Alarm port
(DiagItem_6) NULL	Reserved
(DiagItem_7) NULL	Reserved

The DiagLED display item is changed by a trigger signal input from hardware pin ‘LED\_DMODE\_CK’. The change sequence order of the DiagLED is:

DiagItem\_0 → DiagItem\_1 → DiagItem\_2 → ..... → DiagItem\_7 → Loop to DiagItem\_0

### 8.28.1. Serial LED Display Panel Example (4 LEDs, Register 0x0005)

**Enable Serial LED Display Mode:**

→ set EnSerialMode: 1

**Define Per-port 4 LED Display Mode:**

→ Configuration. set EnLED[3:0]: 1111

**Define the statLED display type as: StatLED0=Link/Act, StatLED1=10/100M, StatLED2=Duplex/Collision:**

→ Configuration. set StatLED0\_mode[2:0]=000, StatLED1\_mode[2:0]=001, StatLED2\_mode[2:0]=010

Follow the same method to configure the per-port 1 LED, per-port 2 LED, and per-port 3 LED display mode, with or without enabling the diagnostic LED.

The LED panel is shown in Figure 10.

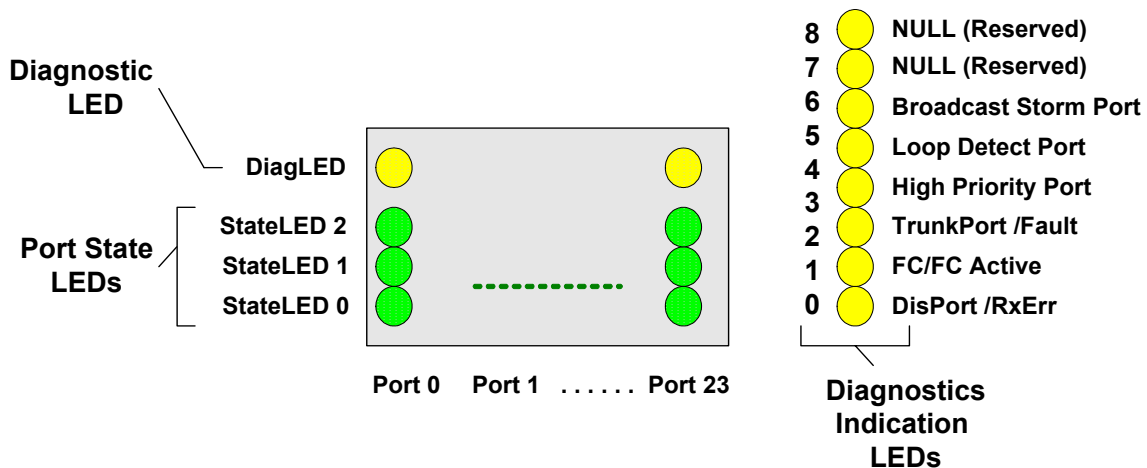


Figure 10. Serial LED Display

### 8.28.2. Serial LED Shift Out Sequence Order

The Serial LED output sequence is defined as follows: (first bit → ... → last bit).

Each port has four LEDs. There are eight diagnostic LEDs:

```

→ [P0 StateLED0] → [P0 StateLED1] → [P0 StateLED2] → [P0 DiagLED0]
→ [P1 StateLED0] → [P1 StateLED1] → [P1 StateLED2] → [P1 DiagLED0]
→ ----- → ----- → ----- → -----
→ [P23 StateLED0] → [P23 StateLED1] → [P23 StateLED2] → [P23 DiagLED0]
→ [Reserved_(DiagS0)] → [Reserved_(DiagS1)] → [Reserved_(DiagS2)] → [Reserved_(DiagS3)]
→ [Reserved_(DiagS4)] → [Reserved_(DiagS5)] → [Reserved_(DiagS6)] → [Reserved_(DiagS7)]
    
```

### 8.28.3. Serial LED Bi-Color LED Mode

For RTL8324 3-bit Bi-color LED mode, Link/Act and Spd are used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarities.

Spd	Link/Act	Indication	Bi-Color state
0	0	No Link	Off
0	1	100Mb/s Link up	Green
1	0	10Mb/s Link up	Yellow

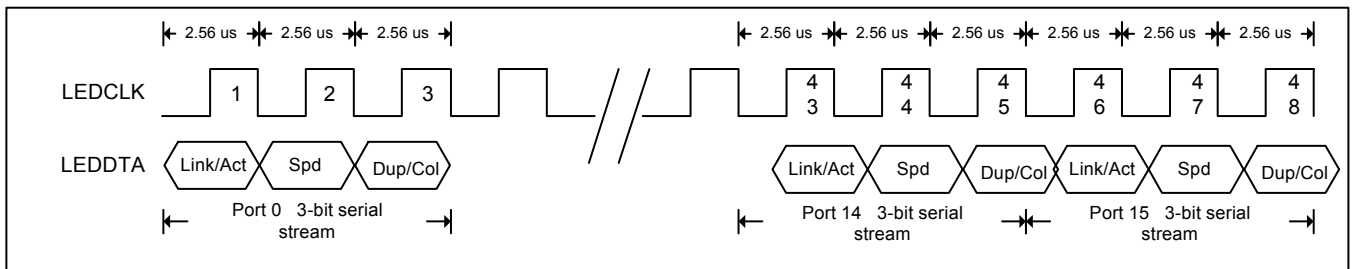
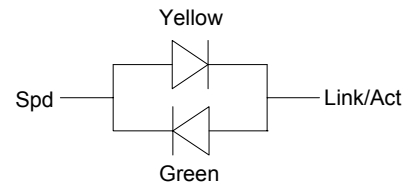


Figure 11. 3-Bit Serial Stream Mode

## 8.29. SCAN LED Interface

The RTL8324 supports Scan LED display mode. The forms of LED status streams, as shown below, are controlled by HW pin LEDMODE[1:0] = 2b'00, and are latched upon reset.

Table 21. Scan LED Status

LED Status	Description
Spd	Speed Indicator High for 100Mbps and low for 10Mbps
Link/Act	Link, Activity Indicator High for link established Blinks when the corresponding port is transmitting or receiving
Col/Fulldup	Full duplex, Collision Indicator High for full duplex, and low for half duplex mode Blinks when there are collisions on the corresponding port

The RTL8324 provides three Scan LED groups that display each port's status:

#### Group A

(Scan\_LED\_A[5:0], Scan\_STSA[3:0]) displays status for port0~port7

#### Group B

(Scan\_LED\_B[5:0], Scan\_STSB[3:0]) displays status for port8~port15



**Group C**

(Scan\_LEDC[5:0], Scan\_STSC[3:0]) displays status for port16~port23.

Scan\_LEDA[5:0], Scan\_LEDB[5:0] and Scan\_LEDC[5:0] operate with the same timing phase. The Scan LED timing diagram is shown below:

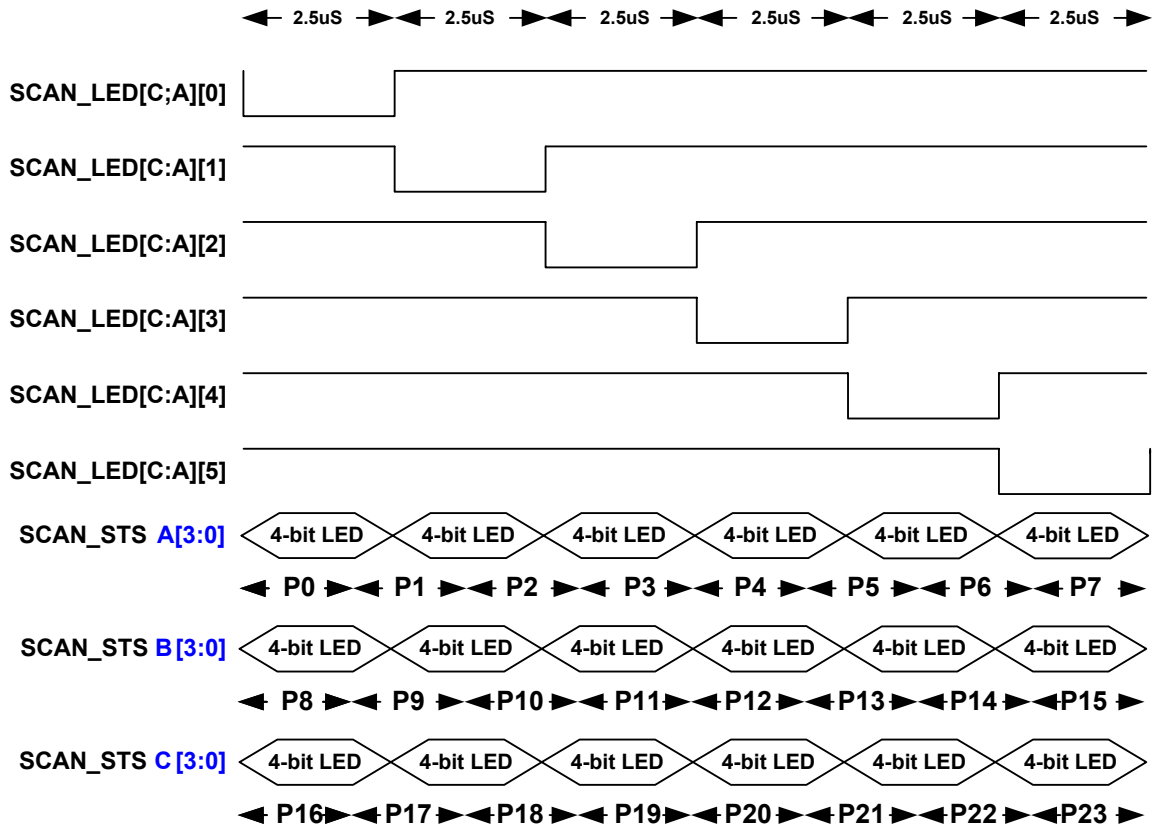
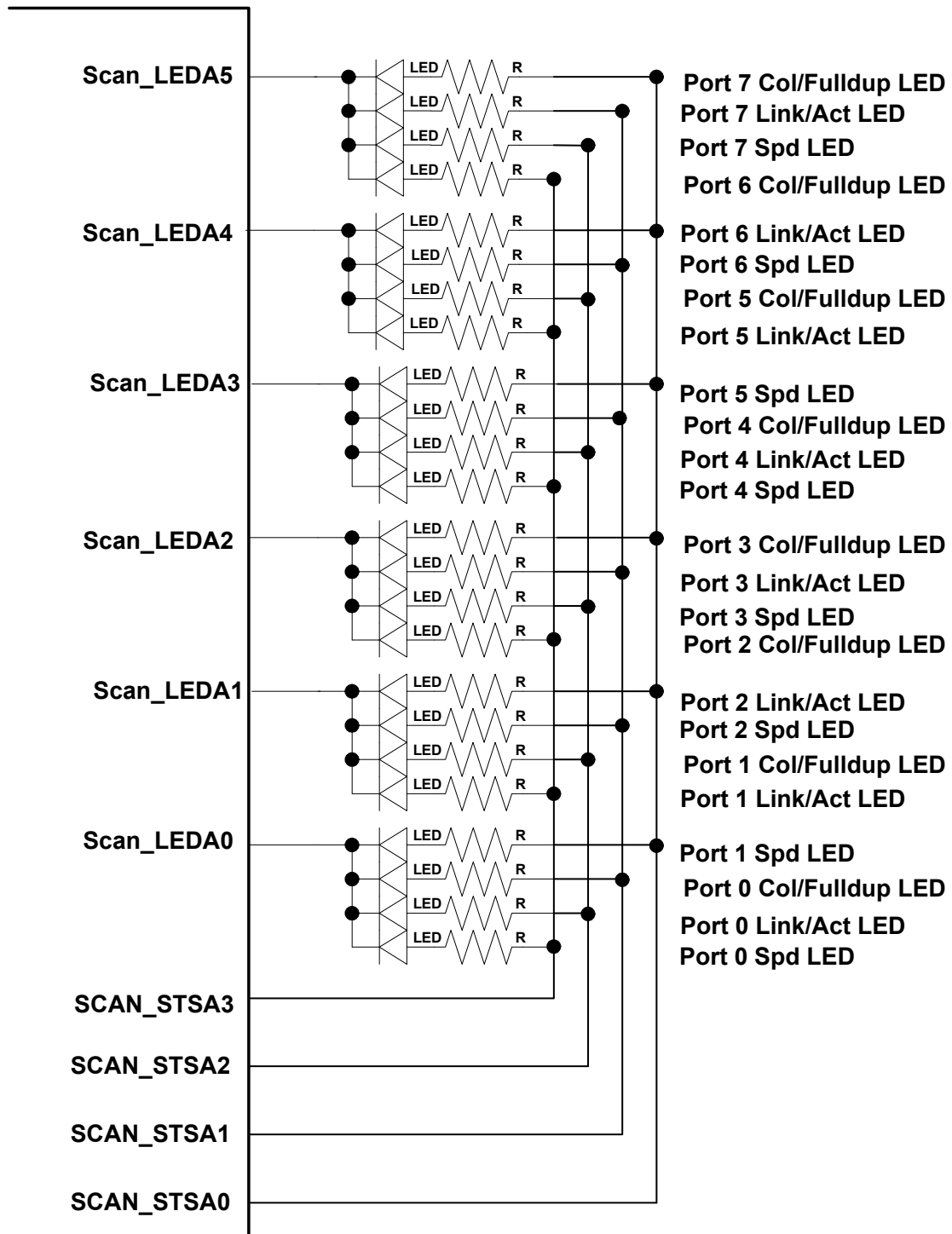
**Scan LED Timing Diagram**


Figure 12. Scan LED Timing Diagram

**External Circuit for Scan LED**
**RTL8324**

**Figure 13. External Circuit for Scan LED**

### 8.30. Port Mirroring

Port mirroring is used to forward traffic to a selected port based on one or more of the following:

- All traffic received from one or multi selected source ports (source mirroring)
- All traffic transmitted to one selected destination port (destination mirroring)

**Table 22. Port Mirror Control Register for P23-P0**

Register	Bits	Name	Description	RW	Default
0x0219	15:0	EnPortMirror(0)[15:0]	Enables the port-based mirror function. Bit n corresponds to port n. Write '1' to enable a port's mirror function	RW	0
0x021A	7:0	EnPortMirror(1)[7:0]	Enables the port-based mirror function. Used for MD_24FX Bit n corresponds to port n. Write '1' to enable a port's mirror function	RW	0

**Table 23. RX Mirror Port Register for P23-P0**

Register	Bits	Name	Description	RW	Default
0x021B	15:0	Mirror_RX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n RX data to mirrored port.	RW	0
0x021C	7:0	Mirror_RX(1)[7:0]	Used for MD_24FX Bit n corresponds to port n. Write '1' to duplicate port n RX data to mirrored port.	RW	0

**Table 24. TX Mirror Port Register for P23-P0**

Register	Bits	Name	Description	RW	Default
0x021D	15:0	Mirror_TX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n TX data to mirrored port.	RW	0
0x021E	7:0	Mirror_TX(1)[7:0]	Used for MD_24FX Bit n corresponds to port n. Write '1' to duplicate port n TX data to mirrored port.	RW	0

## 9. Serial EEPROM Configuration (24LC04)

The EEPROM configuration bits are directly mapped to some of the internal registers. For example, EEPROM addresses 0x04h and 0x05h directly map to internal register 0x0005 ‘LED Display Configuration’.

The mapping rule is: EEPROM 0x00h: REG. 0x0002[7:0], EEPROM 0x01h: REG. 0x0002[15:8].

### 9.1. EEPROM Configuration vs. Internal Register Mapping

**Table 25. EEPROM Configuration vs. Internal Register Mapping**

EEPROM Physical Address (8-Bit Data Entry) (24LC04)	Description	Corresponding Internal Register Address Mapping	Internal Default
01~00	Reserved	0x0002	0A80
03~02	Reserved	0x0003	0155
05~04	LED Display Configuration 0	0x0005	0E88
07~06	Reserved		
09~08	Reserved		
0B~0A	Reserved		
0D~0C	Realtek Protocol Control	0x0200	0000
0F~0E	Reserved		
11~10	Reserved		
13~12	Switch MAC ID 0	0x0203	0000
15~14	Switch MAC ID 1	0x0204	0000
17~16	Switch MAC ID 2	0x0205	0000
19~18	Chip ID 0	0x0206	0000
1B~1A	Vender ID 0	0x0207	0000
1D~1C	Vender ID 1	0x0208	0000
1F~1E	Reserved		
21~20	Reserved		
23~22	ALT Configuration	0x0300	0004
25~24	Port Trunking Configuration	0x0307	0000
27~26	IGMP Control Register	0x0308	0000
29~28	VLAN Control Register	0x030B	0000
2B~2A	Reserved		
2D~2C	Reserved		
2F~2E	QoS Control Register	0x0400	0010
31~30	Port Priority Configuration 0	0x0401	0000
33~32	Port Priority Configuration 1	0x0402	0000
35~34	Reserved		
37~36	Reserved		
39~38	Global Port Control Register	0x0607	0010
3B~3A	Port property Configuration 0	0x060A	AFAF
3D~3C	Port property Configuration 1	0x060B	AFAF
3F~3E	Port property Configuration 2	0x060C	AFAF

<b>EEPROM Physical Address (8-Bit Data Entry) (24LC04)</b>	<b>Description</b>	<b>Corresponding Internal Register Address Mapping</b>	<b>Internal Default</b>
41~40	Port property Configuration 3	0x060D	AFAF
43~42	Port property Configuration 4	0x060E	AFAF
45~44	Port property Configuration 5	0x060F	AFAF
47~46	Port property Configuration 6	0x0610	AFAF
49~48	Port property Configuration 7	0x0611	AFAF
4B~4A	Port property Configuration 8	0x0612	AFAF
4D~4C	Port property Configuration 9	0x0613	AFAF
4F~4E	Port property Configuration 10	0x0614	AFAF
51~50	Port property Configuration 11	0x0615	AFAF
53~52	Internal use	0x0616	--
55~54	Reserved		
57~56	Reserved		
59 ~~~ 5F	Reserved		
61~60	Designer Diagnostic Configuration	0xFFFF	0000

## 10. Internal Register Descriptions

Symbols:

R: Read

V: Configurable

W: Write

P: Partially Configurable

RW: Read/Write

X: Not Configurable

### 10.1. System Configuration Register

Table 26. System Configuration Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0000	0	System Reset	RW	0	X	X
	1	Switch Parameter Register	R(W)	0x84A0	X	X
	2	EEPROM Check ID	R	0	X	V
	3	Reserved	R	0x0100	X	V
	4	LED MODE	RW	0001	X	X
	5	LED Display Configuration 0	RW	1E88	X	V
	6	LED Display Configuration 1	RW	0C00	X	V

### 10.2. System Status Register

Table 27. System Status Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0100	0	Board Trapping Status	R (/W)	0C01	X	X
	1	Loop Detect Status Register(32 bit Reg )	R	0	X	X
	2	System Fault Flag Register	R	0	X	X

### 10.3. Management Configuration Register

Table 28. Management Configuration Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0200	0	Realtek Protocol Control	RW	0001	X	V
	1	Reserved	RW	0	X	V
	2	Reserved	RW	0	X	V
	3	Switch MAC ID (0)	R	0	X	V

Register Base Address	Offset	Description	RW	Default	Pin	EE
	4	Switch MAC ID (1)	R	0	X	V
	5	Switch MAC ID (2)	R	0	X	V
	6	Chip ID (RO)	R	0	X	V
	7	Vender ID (0) (RO)	R	0	X	V
	8	Vender ID (1) (RO)	R	0	X	V
	9	Reserved				
	0A	Port Rate Control Register	RW	0	X	X
	0B	Port Rate Control Register	RW	0	X	X
	0C	Port Rate Control Register	RW	0	X	X
	0D	Port Rate Control Register	RW	0	X	X
	0E	Port Rate Control Register	RW	0	X	X
	0F	Port Rate Control Register	RW	0	X	X
	10	Port Rate Control Register	RW	0	X	X
	11	Port Rate Control Register	RW	0	X	X
	12	Port Rate Control Register	RW	0	X	X
	13	Port Rate Control Register	RW	0	X	X
	14	Port Rate Control Register	RW	0	X	X
	15	Port Rate Control Register	RW	0	X	X
	16	Reserved				
	17	EEPROM RW Command Register	RW	0	X	X
	18	EEPROM RW Data Register	R(/W)	0	X	X
	19	Port Mirror Control Register for P15-P0	RW	0	X	X
	1A	Port Mirror Control Register for P23-P16	RW	0	X	X
	1B	RX Mirror port mask for P15-P0	RW	0	X	X
	1C	RX Mirror port mask for P23-P16	RW	0	X	X
	1D	TX Mirror port mask for P15-P0	RW	0	X	X
	1E	TX Mirror port mask for P23-P16	RW	0	X	X

## 10.4. Address Lookup Table (ALT) Control Register

Table 29. Address Lookup Table (ALT) Control Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0300	0	ALT Configuration	RW	0	P	P
	1	Address Learning Control (0)	RW	0	X	X
	2	Address Learning Control (1)	RW	0	X	X
	3	Unknown SA Management 0 (RO) (0)	R	--	X	X
	4	Unknown SA Management 0 (RO) (1)	R	--	X	X
	5	Unknown SA Management 0 (RO) (2)	R	--	X	X
	6	Unknown SA Management 1(RO)	R	--	X	X
	7	Port Trunking Configuration	RW	8200	P	V
	8	IGMP Control Register	RW	8200	V	V

Register Base Address	Offset	Description	RW	Default	Pin	EE
	9	IP Multicast Router Discovery	R	0	X	X
	0A	Reserved				
	0B	VLAN Control Register	RW	0	P	V
	0C	Port VLAN ID Assignment (0)	RW	0100	X	X
	0D	Port VLAN ID Assignment (1)	RW	0302	X	X
	0E	Port VLAN ID Assignment (2)	RW	0504	X	X
	0F	Port VLAN ID Assignment (3)	RW	0706	X	X
	10	Port VLAN ID Assignment (4)	RW	0908	X	X
	11	Port VLAN ID Assignment (5)	RW	0B0A	X	X
	12	Port VLAN ID Assignment (6)	RW	0D0C	X	X
	13	Port VLAN ID Assignment (7)	RW	0F0E	X	X
	14	Port VLAN ID Assignment (8)	RW	1110	X	X
	15	Port VLAN ID Assignment (9)	RW	1312	X	X
	16	Port VLAN ID Assignment (10)	RW	1514	X	X
	17	Port VLAN ID Assignment (11)	RW	1716	X	X
	18	Reserved				
	19	VLAN TX Priority Tagging Control (0)	RW	FFFF	X	X
	1A	VLAN TX Priority Tagging Control (1)	RW	FFFF	X	X
	1B	VLAN TX Priority Tagging Control (2)	RW	FFFF	X	X
	1C	Reserved				
		Port VLAN Configuration ( 32*[0,1,2])	RW		X	X
	1D	VLAN_0_Entry_Configuration_0 (member[15:0])	RW	0001	X	X
	1E	VLAN_0_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	1F	VLAN_0_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	20	VLAN_1_Entry_Configuration_0 (member[15:0])	RW	0002	X	X
	21	VLAN_1_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	22	VLAN_1_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	23	VLAN_2_Entry_Configuration_0 (member[15:0])	RW	0004	X	X
	24	VLAN_2_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	25	VLAN_2_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	26	VLAN_3_Entry_Configuration_0 (member[15:0])	RW	0008	X	X
	27	VLAN_3_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	28	VLAN_3_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	29	VLAN_4_Entry_Configuration_0 (member[15:0])	RW	0010	X	X
	2A	VLAN_4_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	2B	VLAN_4_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	2C	VLAN_5_Entry_Configuration_0 (member[15:0])	RW	0020	X	X
	2D	VLAN_5_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	2E	VLAN_5_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	2F	VLAN_6_Entry_Configuration_0 (member[15:0])	RW	0040	X	X
	30	VLAN_6_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	31	VLAN_6_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	32	VLAN_7_Entry_Configuration_0 (member[15:0])	RW	0080	X	X



Register Base Address	Offset	Description	RW	Default	Pin	EE
	33	VLAN_7_Entry_Configuration_1 (member[23:16])	RW	00C0	X	X
	34	VLAN_7_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	35	VLAN_8_Entry_Configuration_0 (member[15:0])	RW	0100	X	X
	36	VLAN_8_Entry_Configuration_1 (member[23:16])	RW	01C0	X	X
	37	VLAN_8_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	38	VLAN_9_Entry_Configuration_0 (member[15:0])	RW	0200	X	X
	39	VLAN_9_Entry_Configuration_1 (member[23:16])	RW	02C0	X	X
	3A	VLAN_9_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	3B	VLAN_10_Entry_Configuration_0 (member[15:0])	RW	0400	X	X
	3C	VLAN_10_Entry_Configuration_1 (member[23:16])	RW	04C0	X	X
	3D	VLAN_10_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	3E	VLAN_11_Entry_Configuration_0 (member[15:0])	RW	0800	X	X
	3F	VLAN_11_Entry_Configuration_1 (member[23:16])	RW	08C0	X	X
	40	VLAN_11_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	41	VLAN_12_Entry_Configuration_0 (member[15:0])	RW	1000	X	X
	42	VLAN_12_Entry_Configuration_1 (member[23:16])	RW	10C0	X	X
	43	VLAN_12_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	44	VLAN_13_Entry_Configuration_0 (member[15:0])	RW	2000	X	X
	45	VLAN_13_Entry_Configuration_1 (member[23:16])	RW	20C0	X	X
	46	VLAN_13_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	47	VLAN_14_Entry_Configuration_0 (member[15:0])	RW	4000	X	X
	48	VLAN_14_Entry_Configuration_1 (member[23:16])	RW	40C0	X	X
	49	VLAN_14_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	4A	VLAN_15_Entry_Configuration_0 (member[15:0])	RW	8000	X	X
	4B	VLAN_15_Entry_Configuration_1 (member[23:16])	RW	80C0	X	X
	4C	VLAN_15_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	4D	VLAN_16_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	4E	VLAN_16_Entry_Configuration_1 (member[23:16])	RW	00C1	X	X
	4F	VLAN_16_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	50	VLAN_17_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	51	VLAN_17_Entry_Configuration_1 (member[23:16])	RW	00C2	X	X
	52	VLAN_17_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	53	VLAN_18_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	54	VLAN_18_Entry_Configuration_1 (member[23:16])	RW	00C4	X	X
	55	VLAN_18_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	56	VLAN_19_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	57	VLAN_19_Entry_Configuration_1 (member[23:16])	RW	00C8	X	X
	58	VLAN_19_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	59	VLAN_20_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	5A	VLAN_20_Entry_Configuration_1 (member[23:16])	RW	00D0	X	X
	5B	VLAN_20_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	5C	VLAN_21_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	5D	VLAN_21_Entry_Configuration_1 (member[23:16])	RW	00E0	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	5E	VLAN_21_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	5F	VLAN_22_Entry_Configuration_0 (member[15:0])	RW	FFFF	X	X
	60	VLAN_22_Entry_Configuration_1 (member[23:16])	RW	FFFF	X	X
	61	VLAN_22_Entry_Configuration_2 (VID[11:0])	RW	F000	X	X
	62	VLAN_23_Entry_Configuration_0 (member[15:0])	RW	FFFF	X	X
	63	VLAN_23_Entry_Configuration_1 (member[23:16])	RW	FFFF	X	X
	64	VLAN_23_Entry_Configuration_2 (VID[11:0])	RW	F000	X	X
	65	VLAN_24_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	66	VLAN_24_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	67	VLAN_24_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	68	VLAN_25_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	69	VLAN_25_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	6A	VLAN_25_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	6B	VLAN_26_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	6C	VLAN_26_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	6D	VLAN_26_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	6E	VLAN_27_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	6F	VLAN_27_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	70	VLAN_27_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	71	VLAN_28_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	72	VLAN_28_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	73	VLAN_28_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	74	VLAN_29_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	75	VLAN_29_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	76	VLAN_29_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	77	VLAN_30_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	78	VLAN_30_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	79	VLAN_30_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	7A	VLAN_31_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	7B	VLAN_31_Entry_Configuration_1 (member[23:16])	RW	0000	X	X
	7C	VLAN_31_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	7D	Insert per-port VID enabling register	RW	0	X	V
	7E	Insert per-port VID enabling register	RW	0	X	V

## 10.5. Queue Control Register

**Table 30. Queue Control Register**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0400	0	QoS Control Register	RW	0	V	V
	1	Port Priority Configuration (0)	RW	0	V	V
	2	Port Priority Configuration (1)	RW	0	V	V
	8	Reserved				

## 10.6. PHY Access Control Register

**Table 31. PHY Access Control Register**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0500	0	PHY Access Addressing Control	R(W)	0	X	X
	1	PHY Access Write Data	RW	--	X	X
	2	PHY Access Read Data	R	--	X	X

## 10.7. Port Control Register

**Table 32. Port Control Register**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0600	0~6	Reserved				
	7	Global Port Control Register	RW	0010	V	V
	8	Port Access Authority Control (0)	RW	0	X	X
	9	Port Access Authority Control (1)	RW	0	X	X
	A	Port Property Configuration Register 0 (Port 0, 1)	RW	AFAF	X	V
	B	Port Property Configuration Register 1 (Port 2, 3)	RW	AFAF	X	V
	C	Port Property Configuration Register 2 (Port 4, 5)	RW	AFAF	X	V
	D	Port Property Configuration Register 3 (Port 6, 7)	RW	AFAF	X	V
	E	Port Property Configuration Register 4 (Port 8, 9)	RW	AFAF	X	V
	F	Port Property Configuration Register 5 (Port 10, 11)	RW	AFAF	X	V
	10	Port Property Configuration Register 6 (Port 12, 13)	RW	AFAF	X	V
	11	Port Property Configuration Register 7 (Port 14, 15)	RW	AFAF	X	V
	12	Port Property Configuration Register 8 (Port 16, 17)	RW	AFAF	X	V
	13	Port Property Configuration Register 9 (Port 18, 19)	RW	AFAF	X	V
	14	Port Property Configuration Register 10 (Port 20, 21)	RW	AFAF	X	V
	15	Port Property Configuration Register 11 (Port 22, 23)	RW	AFAF	X	V
	16	Reserved				
	17	Reserved				
	18	Reserved[15:2], SyncOk [1:0]	R		X	X
	19	Port Link Status Register 0 (Port 0, 1)	R	0	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	1A	Port Link Status Register 1 (Port 2, 3)	R	0	X	X
	1B	Port Link Status Register 2 (Port 4, 5)	R	0	X	X
	1C	Port Link Status Register 3 (Port 6, 7)	R	0	X	X
	1D	Port Link Status Register 4 (Port 8, 9)	R	0	X	X
	1E	Port Link Status Register 5 (Port 10, 11)	R	0	X	X
	1F	Port Link Status Register 6 (Port 12, 13)	R	0	X	X
	20	Port Link Status Register 7 (Port 14, 15)	R	0	X	X
	21	Port Link Status Register 8 (Port 16, 17)	R	0	X	X
	22	Port Link Status Register 9 (Port 18, 19)	R	0	X	X
	23	Port Link Status Register 10 (Port 20, 21)	R	0	X	X
	24	Port Link Status Register 11 (Port 22, 23)	R	0	X	X
	25	Reserved				
	26	Reserved				
	27	Reserved				
	28	Reserved				

## 10.8. MIB Counter Register

**Table 33. MIB Counter Register**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	0	Port MIB Counter Object Selection Register 0 (Port 0, 1)	RW	0555	X	X
	1	Port MIB Counter Object Selection Register 1 (Port 2, 3)	RW	0555	X	X
	2	Port MIB Counter Object Selection Register 2 (Port 4, 5)	RW	0555	X	X
	3	Port MIB Counter Object Selection Register 3 (Port 6, 7)	RW	0555	X	X
	4	Port MIB Counter Object Selection Register 4 (Port 8, 9)	RW	0555	X	X
	5	Port MIB Counter Object Selection Register 5 (Port 10, 11)	RW	0555	X	X
	6	Port MIB Counter Object Selection Register 6 (Port 12, 13)	RW	0555	X	X
	7	Port MIB Counter Object Selection Register 7 (Port 14, 15)	RW	0555	X	X
	8	Port MIB Counter Object Selection Register 8 (Port 16, 17)	RW	0555	X	X
	9	Port MIB Counter Object Selection Register 9 (Port 18, 19)	RW	0555	X	X
	A	Port MIB Counter Object Selection Register 10 (Port 20, 21)	RW	0555	X	X
	B	Port MIB Counter Object Selection Register 11 (Port 22, 23)	RW	0555	X	X
	C	Reserved				

### 10.8.1. Port MIB Counter 1 Register (RX Counter) (32-bits)

**Table 34. Port MIB Counter 1 Register (RX Counter) (32-bits)**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	D	Port 0 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	E	Port 1 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	F	Port 2 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	10	Port 3 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	11	Port 4 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	12	Port 5 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	13	Port 6 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	14	Port 7 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	15	Port 8 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	16	Port 9 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	17	Port 10 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	18	Port 11 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	19	Port 12 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1A	Port 13 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1B	Port 14 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1C	Port 15 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1D	Port 16 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1E	Port 17 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1F	Port 18 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	20	Port 19 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	21	Port 20 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	22	Port 21 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	23	Port 22 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	24	Port 23 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	25	Reserved				
	26	Reserved				

## 10.8.2. Port MIB Counter 2 Register (TX Counter) (32-bits)

**Table 35. Port MIB Counter 2 Register (TX Counter) (32-bits)**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	27	Port 0 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	28	Port 1 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	29	Port 2 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2A	Port 3 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2B	Port 4 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2C	Port 5 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2D	Port 6 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2E	Port 7 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2F	Port 8 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	30	Port 9 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	31	Port 10 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	32	Port 11 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	33	Port 12 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	34	Port 13 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	35	Port 14 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	36	Port 15 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	37	Port 16 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	38	Port 17 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	39	Port 18 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3A	Port 19 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3B	Port 20 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3C	Port 21 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3D	Port 22 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3E	Port 23 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3F	Reserved				
	40	Reserved				

### 10.8.3. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

**Table 36. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	41	Port 0 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	42	Port 1 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	43	Port 2 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	44	Port 3 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	45	Port 4 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	46	Port 5 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	47	Port 6 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	48	Port 7 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	49	Port 8 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4A	Port 9 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4B	Port 10 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4C	Port 11 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4D	Port 12 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4E	Port 13 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4F	Port 14 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	50	Port 15 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	51	Port 16 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	52	Port 17 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	53	Port 18 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	54	Port 19 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	55	Port 20 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	56	Port 21 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	57	Port 22 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	58	Port 23 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	59	Reserved				
	5A	Reserved				

### 10.9. System Parameter Register (Reserved)

**Table 37. System Parameter Register (Reserved)**

Register Base Address	Offset	Description	RW	Default	Pin	EE
0xFFFF	--	System Parameter Register (Reserved).	RW	0	V	V



## 11. Internal Register Settings

Register Symbols:

R: Read

LL: Latch Low until cleared

W: Write

LH: Latch High until cleared

RW: Read/Write

SC: Self Clearing

(W: EEPROM. Permit writing by EEPROM)

RC: Read to Clear

### 11.1. System Configuration Register

#### 11.1.1. 0x0000H: System Reset Control Register

**Table 38. 0x0000H: System Reset Control Register**

Bits	Name	Description	RW	Default
0	SRST	Soft Reset. A soft reset will reset the system similar to a power on reset except that the user configuration will not be cleared: 1. The MAC table and VLAN table data are kept. 2. All current user configured internal register values are kept. 3. The EEPROM download is not done again. 4. The system restarts the auto-negotiation process.  0: Normal (Default) 1: Soft reset	W/SC	0
1	HRST	Hardware Reset. Resets the system to the power on initial state: 1. Downloads configuration from strap pin and EEPROM. 2. Starts internal Memory self test. 3. Clears all the MAC, VLAN tables. 4. Resets all registers to default values. 5. Restarts auto-negotiation.  0: Normal (Default) 1: Hardware reset	W/SC	0
15:2	Reserved			



### 11.1.2. 0x0001H: Switch Parameter Register

Note: The Write operation is reserved for IC testing mode. Do NOT write this register.

**Table 39. 0x0001H: Switch Parameter Register**

Bits	Name	Description	RW	Default
1:0	MaxPktLen[1:0]	System Valid Max Packet Length. The minimum packet length is 64 bytes. The maximum packet length is controlled by MaxPktLen[1:0]: 00: 1536 bytes (Default) 01: 1552 byte 1x: Reserved.	RW	00 HW pin MaxPktLen
2	TXIPG_Comp	Transmit IPG Compensation. Used to compensate the oscillator frequency or incoming packet Inter-Packet Gap (IPG) tolerance. 0: Give +65 ppm TXIPG compensation (Default) 1: Give +90 ppm TXIPG compensation	RW	0
3	MaxPauseCnt	Max Pause Count for Congestion Control. 0: Supports a maximum of 128 Pause frames during congestion control (Default) 1: Continue Pause mode. Do not limit the Pause frame count during congestion control.	RW	0 HW pin MaxPauseCnt
4	DisBKP48One (EnBKP48One)	Disable Back pressure 48 Pass One Algorithm. When the 48One algorithm is enabled, the switch will pass one incoming packet after every 48 collisions. 0: Enable 48 Pass One algorithm (Default) 1: Disable 48 Pass One algorithm	RW	0 HW pin EnBKP48One
6:5	Reserved	Internal test bit.		
7	DisCRSBKPMode (EnCOLBKPMode)	Disable Carrier Based Back Pressure Mode. Half duplex back pressure algorithm selection. 0: Select Collision-based back pressure mode 1: Select Carrier-based back pressure mode (Default)	RW	1 HW pin EnCOLBKPMode
15:8	Reserved	Internal test bit.		

### 11.1.3. 0x0002H: EEPROM Check ID

**Table 40. 0x0002H: EEPROM Check ID**

Bits	Name	Description	RW	Default
5:0	Reserved (EEPROM Check ID)	Reserved bits. Used for EEPROM existence checking. Keep the value at 000000.		
15:6	Reserved	Internal test bit.		

### 11.1.4. 0x0004H: General Purpose User Defined I/O Data Register

**Table 41. 0x0004H: General Purpose User Defined I/O Data Register**

Bits	Name	Description	RW	Default
1:0	LED MODE	00: Scan Led 01: Single-color serial (default) 10: Bi-color serial 11: Reserved	RW	01 HW pin P9TXD P8TXD
15:2	Reserved			

### 11.1.5. 0x0005H: LED Display Configuration

**Table 42. 0x0005H: LED Display Configuration**

Bits	Name	Description	RW	Default
2:0	StatLED0_mode[2:0]	Mode Selection for State LED0. This state LED mode selection register controls the status type of the State LED0. The Status type is defined as follows: 000: Link/Act (Default) 001: 100Spd 010: Duplex/Col 011: Link/Act/100Spd 100: Duplex 101: Act 110: Link 111: Col	RW	000
5:3	StatLED1_mode[2:0]	Mode Selection for State LED1. 000: Link/Act 001: 100Spd (Default) 010: Duplex/Col 011: Link/Act/100Spd 100: Duplex 101: Act 110: Link 111: Col	RW	001
8:6	StatLED2_mode[2:0]	Mode Selection for State LED2. 000: Link/Act 001: 100Spd 010: Duplex/Col (Default) 011: Link/Act/100Spd 100: Duplex 101: Act 110: Link 111: Col	RW	010

Bits	Name	Description	RW	Default
12:9	EnLED[3:0]	State LED 0, 1, 2 and Diagnostic LED Enable/Disable Control. EnLED[3:0] controls enabling/disabling of DiagLED, StatLED2, StatLED1, StatLED0. 0: Disable 1: Enable If an LED is disabled, the corresponding serial clock will be masked.	RW	0111
14:13	Diagnostic mode		RW	00
15	Reserved			

## 11.2. System Status Register

### 11.2.1. 0x0100H: Board Trapping Status Register

**Table 43. 0x0100H: Board Trapping Status Register**

Bits	Name	Description	RW	Default
0	EEPROM_detect_status	EEPROM Existence Status. 0: Exists (Default) 1: Does not Exist	R	0
15:2	Reserved			

### 11.2.2. 0x0101H: Loop Detect Status Register (32-Bit Register)

**Table 44. 0x0101H: Loop Detect Status Register (32-Bit Register)**

Bits	Name	Description	RW	Default
23:0	LoopDetPort[23:0]	Network Loop event Detect Port Status. If the loop detect function is enabled, the corresponding bit of LoopDetPort[23:0] will be set whenever a loop event is detected on the corresponding switch port. The set bit is cleared only when the loop event has disappeared on that port.  When the loop detect function is enabled, the switch will periodically transmit one loop detect diagnostic frame. The normal interval time is approx. five minutes. When a loop event is detected, the interval time will be changed to fast mode. In fast mode the interval time is about 1 second in order to accelerate detection and diagnostic. The loop event will be reported in this Loop Detect Status Register. 0: No Loop detected on this port (Default) 1: Loop detected on this port	R	0
31:24	Reserved			

### 11.2.3. 0x0102H: System Fault Indication Register

**Table 45. 0x0102H: System Fault Indication Register**

Bits	Name	Description	RW	Default
0	Reserved			
1	TrunkFault	Trunk Fault event flag. The flag indicates that there is a trunk port member link down. The trunk will still continue to operate due to the trunk auto fault recovery algorithm. 0: No trunk fault detected (Default) 1: Trunk fault detected	R	0
2	LoopFault	Network Loop Fault Indication. When the Loop Fault indication is set, a loop detected port will be reported on the Loop Detect Port Register. 0: Network Loop not detected (Default) 1: Network Loop detected	R	0
5:3	Reserved			
11:6	FaultTkGroup[5:0]	The Fault Trunk Group Indicator. Indicates a Link Fault in the trunk group. A physical link failure of an enabled trunk group will cause the corresponding bit to be set in the FaultTkGroup[5:0]. This is a real time fault status report. Even though the Trunk Group's fault occurred and the fault bit is set, the corresponding trunk can still work properly as fault recovery will be auto applied.  FaultTkGroup[0] indicator for Trunk 1: (port 0, 1, 2, 3) FaultTkGroup[1] indicator for Trunk 2: (port 4, 5, 6, 7) FaultTkGroup[2] indicator for Trunk 3: (port 8, 9, 10, 11) FaultTkGroup[3] indicator for Trunk 4: (port 12, 13, 14, 15) FaultTkGroup[4] indicator for Trunk 5: (port 16, 17, 18, 19) FaultTkGroup[5] indicator for Trunk 6: (port 20, 21, 22, 23)  0: Trunk OK 1: Trunk Fault detected	R	000000
15:12	Reserved			

## 11.3. Management Configuration Register

### 11.3.1. 0x0200H: Realtek Protocol Control Register

**Table 46. 0x0200H: Realtek Protocol Control Register**

Bits	Name	Description	RW	Default
0	Reserved			
1	DisREcho	Disable Realtek Remote Echo Protocol. 0: Enable REcho protocol (Default) 1: Disable REcho protocol	RW	0
2	EnLoopDet	Enable Loop Detect Function. When enabled, the loop detect status will be reported in register 0x0101 (Loop Detect Status Register). 0: Disable(Default) 1: Enable	RW	0
15:3	Reserved			

### 11.3.2. 0x0203H: Switch MAC ID Register 0

**Table 47. 0x0203H: Switch MAC ID Register 0**

Bits	Name	Description	RW	Default
15:0	MACID[15:0]	Switch Physical MAC Address bit[15:0]. E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52.	R (W: EEPROM)	0

### 11.3.3. 0x0204H: Switch MAC ID Register 1

**Table 48. 0x0204H: Switch MAC ID Register 1**

Bits	Name	Description	RW	Default
15:0	MACID[31:16]	Switch Physical MAC Address bit[31:16] E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52.	R (W: EEPROM)	0

### 11.3.4. 0x0205H: Switch MAC ID Register 2

**Table 49. 0x0205H: Switch MAC ID Register 2**

Bits	Name	Description	RW	Default
15:0	MACID[47:32]	Switch Physical MAC Address bit[47:32]. E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52.	R (W: EEPROM)	0

### 11.3.5. 0x0206H: Chip Model ID

**Table 50. 0x0206H: Chip Model ID**

Bits	Name	Description	RW	Default
7:0	ChipID[7:0]	Chip ID. Identifies the chip version for programmer version control.	R (W: EEPROM)	0
15:8	Reserved			

### 11.4. 0x0207H: System Vender ID Register 0

**Table 51. 0x0207H: System Vender ID Register 0**

Bits	Name	Description	RW	Default
15:0	VenderID[15:0]	System Vender Identity Stream [15:0]. Used for the system vender to fill a code or name stream for switch device model number or vender name identification.	R (W: EEPROM)	0

### 11.5. 0x0208H: System Vender ID Register 1

**Table 52. 0x0208H: System Vender ID Register 1**

Bits	Name	Description	RW	Default
15:0	VenderID[31:16]	System Vender Identity Stream [31:16]. Used for system vender to fill a code or name stream for switch device model number or vender name identification.	R (W: EEPROM)	0

### 11.6. 0x020AH: Port 0, 1 Bandwidth Control Register

**Table 53. 0x020AH: Port 0, 1 Bandwidth Control Register**

Bits	Name	Description	RW	Default
3:0	PORXRate[3:0]	Port 0 RX Bandwidth Control. Configures the maximum output bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum RX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000

Bits	Name	Description	RW	Default
7:4	P0TXRate[3:0]	Port 0 TX Bandwidth Control. Configures the maximum input bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum TX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000
11:8	P1RXRate[3:0]	Port 1 RX Bandwidth Control. Configures the maximum output bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum RX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000
15:12	P1TXRate[3:0]	Port 1 TX Bandwidth Control. Configures the maximum input bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum TX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000

### 11.6.1. 0x020BH~0x0215H: Port 2~23 Bandwidth Control Register

Refer to Table 53, page 58, for Configuration description of n: 1 ~ 11.

**Table 54. 0x020BH~0x0215H: Port 2~23 Bandwidth Control Register**

Bits	Name	Description	RW	Default
3:0	P2nRXRate[3:0]	Port 2n RX Bandwidth Control	RW	0000
7:4	P2nTXRate[3:0]	Port 2n TX Bandwidth Control	RW	0000
11:8	P2n+1RXRate[3:0]	Port 2n+1 RX Bandwidth Control.	RW	0000
15:12	P2n+1TXRate[3:0]	Port 2n+1 TX Bandwidth Control.	RW	0000

## 11.7. 0x0217H~0x0218: EEPROM RW Control Register

### 11.7.1. 0x0217H: EEPROM RW Command Register

**Table 55. 0x0217H: EEPROM RW Command Register**

Bits	Name	Description	RW	Default
7:0	EEPROM address	Assigns EEPROM address bits.	RW	0
10:8	CHIP_SEL[2:0]	Assigns chip selection bits.	RW	0
11	Read/Write Operation	0: Write Operation 1: Read Operation	RW	0
12	Status	0: Idle 1: Busy	RW	0
13	Operation Success status	0: Operation Succeeded 1: Operation Failed (Read Clear)	RW	0
15:14	Reserved			

### 11.7.2. 0x0218H: EEPROM RW Data Register

**Table 56. 0x0218H: EEPROM RW Data Register**

Bits	Name	Description	RW	Default
7:0	WdataEE[7:0]	Data to be written to EEPROM.	RW	0
15:8	RdataEE[15:8]	Data Read from EEPROM.	R	0



## 11.8. 0x0219H~0x021EH: Port Mirror Control Register

### 11.8.1. 0x0219H: Port Mirror Control Register 0 for P15-P0

**Table 57. Port Mirror Control Register for P15-P0**

Bits	Name	Description	RW	Default
15:0	EnPortMirror(0)[15:0]	Enables the port-based mirror function. Bit n corresponds to port n. Write '1' to enable a port's mirror function.	RW	0

### 11.8.2. 0x021AH: Port Mirror Control Register 1 for P23-P16

**Table 58. Port Mirror Control Register for P23-P16**

Bits	Name	Description	RW	Default
7:0	EnPortMirror(1)[7:0]	Enables the port-based mirror function. Used for MD_24FX Bit n corresponds to port n. Write '1' to enable a port's mirror function	RW	0
15:8	Reserved			

### 11.8.3. 0x021BH: RX Mirror Port Register 0 for P15-P0

**Table 59. RX Mirror Port Register 0 for P15-P0**

Bits	Name	Description	RW	Default
15:0	Mirror_RX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n RX data to mirrored port.	RW	0

### 11.8.4. 0x021CH: RX Mirror Port Register 1 for P23-P16

**Table 60. RX Mirror Port Register 1 for P23-P16**

Bits	Name	Description	RW	Default
7:0	Mirror_RX(1)[7:0]	Used for MD_24FX. Bit n corresponds to port (16+n). Write '1' to duplicate port n RX data to mirrored port.	RW	0
15:8	Reserved			

### 11.8.5. 0x021DH: TX Mirror Port Register 0 for P15-P0

**Table 61. TX Mirror Port Register 0 for P15-P0**

Bits	Name	Description	RW	Default
15:0	Mirror_TX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n TX data to mirrored port.	RW	0

### 11.8.6. 0x021EH: TX Mirror Port Register 1 for P23-P16

**Table 62. RX Mirror Port Register 1 for P23-P16**

Bits	Name	Description	RW	Default
7:0	Mirror_TX(1)[7:0]	Used for MD_24FX Bit n corresponds to port (16+n). Write '1' to duplicate port n TX data to mirrored port.	RW	0
15:8	Reserved			

## 11.9. Address Lookup Table (ALT) Control Register

### 11.9.1. 0x0300H: ALT Configuration Register

**Table 63. 0x0300H: ALT Configuration Register**

Bits	Name	Description	RW	Default
0	DisMacAging	Global Disable Mac Table Aging Function. 0: Enable Aging function (Default) 1: Disable Aging function	RW	0
1	EnFastAgeTime	Enable Fast Aging Time Mode. 0: Disable Fast Aging time; Aging set to 200~300 seconds (Default) 1: Enable Fast Aging time; Aging set to 12 seconds	RW	0
2	EnCtrlFilter	Global Enable 802.1D Specified Reserved Control Frame Filtering. When network control packets are received with a destination MAC address as the group MAC address: (01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F), the switch will drop the packets if the bit EnCtrlFilter=1. Otherwise (EnCtrlFilter=0) they will be flooded. 1: Enable Filtering (Default) 0: Disable Filtering	RW	1 HW pin. EnCtrlFilter
3	EnDropUknDA	Internal test bit.	RW	0
15:4	Reserved			

### 11.9.2. 0x0301H: Address Learning Control Register 0

**Table 64. 0x0301H: Address Learning Control Register 0**

Bits	Name	Description	RW	Default
15:0	DisMacLearn[15:0]	Per-Port Disable Mac Address Learning Function (Ports 0~15). DisMacLearn[15:0] control port[15:0]. The Layer 2 MAC address learning function can be per-port disabled for security management purposes. Generally this register is used with the ALT Configuration Register (0x0300) bits 'DisMacAging'. 0: Enable learning (Default) 1: Disable learning	RW	0

### 11.9.3. 0x0302H: Address Learning Control Register 1

**Table 65. 0x0302H: Address Learning Control Register 1**

Bits	Name	Description	RW	Default
7:0	DisMacLearn[23:16]	Per-Port Disable Mac Address Learning Function (port 16~25). DisMacLearn[23:16] control port[23:16]. The Layer 2 MAC address learning function can be per-port disabled for security management purposes. Generally this register is used with the ALT Configuration Register (0x0300H) bits 'DisMacAging' &. 0: Enable learning (Default) 1: Disable learning	RW	0
15:8	Reserved			

### 11.9.4. 0x0307H: Port Trunking Configuration Register

**Table 66. 0x0307H: Port Trunking Configuration Register**

Bits	Name	Description	RW	Default
0	Reserved			
6:1	EnTrunk[5:0]	Trunk Group Enable/Disable Control. Enables trunk groups.  EnTrunk[0] control for Trunk 1: (port 0, 1, 2, 3). EnTrunk[1] control for Trunk 2: (port 4, 5, 6, 7). EnTrunk[2] control for Trunk 3: (port 8, 9, 10, 11). EnTrunk[3] control for Trunk 4: (port 12, 13, 14, 15). EnTrunk[4] control for Trunk 5: (port 16, 17, 18, 19). EnTrunk[5] control for Trunk 6: (port 20, 21, 22, 23).  0: Disable Trunking (Default) 1: Enable Trunking	RW	0x00
15:7	Reserved			

### 11.9.5. 0x0308H: IGMP Snooping Control Register

**Table 67. 0x0308H: IGMP Snooping Control Register**

Bits	Name	Description	RW	Default
0	EnIGMPsnooping	Enable IGMP Snooping. The switch controller features an ASIC-based auto IGMP v1 snooping function. No software support is required. When enabled, the switch can automatically snoop IGMP packets and build up an IP multicast address table. The discovered IP multicast Router port will be indicated in the 'IP Multicast Router Port Discovery Register'. 0: Disable IGMP snooping (Default) 1: Enable IGMP snooping	RW	0
15:1	Reserved			

### 11.9.6. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)

**Table 68. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)**

Bits	Name	Description	RW	Default
23:0	IPMRouterDISC[23:0]	IP Multicast Router Ports Discovery Result. This is a bit map that indicates which port is an IP Multicast Router port. IPMRouterDISC[23:0] maps to port 23 ~ 0 0: Normal port (Default) 1: IP multicast Router port	R	0
31:24	Reserved			

### 11.9.7. 0x030BH: VLAN Control Register

**Table 69. 0x030BH: VLAN Control Register**

Bits	Name	Description	RW	Default
0	EnHomeVlan	Enable VLAN Function. When the VLAN function is enabled, the power on default VLAN topology is 24 Home VLANs for non-EEPROM environments. The VLAN topology can be configured by Port VLAN Configuration Registers. 0: Disable VLAN (Default) 1: Enable VLAN	RW	0 HW pin. EnHomeVLAN
1	EnUCleaky	Unicast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for unicast forwarding packets. Normally, inter-VLAN packet switching is not valid. The RTL8324 supports a control bit to enable inter-VLAN communication in the switch without an external router. 0: Disable (Default) 1: Enable	RW	0

Bits	Name	Description	RW	Default
2	EnARPlucky	ARP broadcast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for ARP broadcast packet forwarding. 0: Disable (Default) 1: Enable	RW	0
3	EnIPMleaky	IP Multicast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for ARP broadcast packet forwarding. 0: Disable (Default) 1: Enable	RW	0
4	En8021Qaware	Enable 802.1Q VLAN tag aware. If 802.1Q VLAN aware, the switch supports the ability to identify the VLAN ID from the VLAN tag. Reset to force the switch to ignore the VLAN tag header and classify the VLAN only by the PVID. 0: Disable 802.1Q VLAN aware (Default) 1: Enable 802.1Q VLAN aware	RW	0
5	EnIR_TagAdmit	Ingress Rule for Acceptable frame types control. If this parameter is set to 'Admit only VLAN-Tagged Frames', any frames received on that port that carry no VID (i.e., Untagged Frames or Priority-Tagged Frames) are discarded. If this parameter is set to 'Admit all Frames', all incoming Priority-Tagged and Untagged Frames are associated with a VLAN by the ingress rule on the receiving port. 0: Admit all Frames (Default) 1: Admit only VLAN-Tagged Frames	RW	0
6	EnIR_MembSet	Ingress Rule for Ingress Filtering control. If the Enable Ingress Filtering parameter 'EnIR_MembSet' is set, then all frames received on a port whose VLAN classification does not include that port in its member set shall be discarded. 0: Disable ingress member set Filtering (Default) 1: Enable ingress member set filtering	RW	0
15:7	Reserved			

## 11.9.8. 0x030C~0x0317H: Port VLAN ID Assignment Index Register 0~11

For Port(2n), and Port(2n+1) the register is defined as follows: where n=0, 1, 2, ... 10, 11 (Addr: 0x030CH + n).

**Table 70. 0x030C~0x0317H: Port VLAN ID Assignment Index Register 0~11**

Bits	Name	Description	RW	Default
7:0	P(2n)_VIDIndex[7:0]	Port(2n) VID assignment Index. Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID. Bit[7:5]: Reserved	RW	n
15:8	P(2n+1)_VIDIndex[7:0]	Port(2n+1) VID assignment Index. Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID. Bit[7:5]: Reserved	RW	2n+1

## 11.9.9. 0x0319~0x031BH: VLAN Output Port Priority-Tagging Control Register 0, 1, 2

For Port(8n), Port(8n+1), .... ~ Port(8n+7) the register is defined as follows: n=0, 1, 2

**Table 71. 0x0319~0x031BH: VLAN Output Port Priority-Tagging Control Register 0, 1, 2**

Bits	Name	Description	RW	Default
1:0	P(8n)_PriTagCtl[1:0]	Port(8n) VLAN Output priority Tag/Untag Control. 00: Remove the VLAN tag from a tagged frame 01: Insert priority tag into an untagged high-priority frame (set priority field: 7, VID field: 0 for high priority frame) 10: Insert priority tag into all untagged frames. (set priority field: 7, VID field: 0 for high priority frame; set priority field: 0, VID field: 0 for low priority frame) 11: Don't touch (Don't modify the packet) (Default)	RW	11
3:2	P(8n+1)_PriTagCtl[1:0]	Port(8n+1) VLAN Output priority Tag/Untag Control.	RW	11
5:4	P(8n+2)_PriTagCtl[1:0]	Port(8n+2) VLAN Output priority Tag/Untag Control.	RW	11
7:6	P(8n+3)_PriTagCtl[1:0]	Port(8n+3) VLAN Output priority Tag/Untag Control.	RW	11
9:8	P(8n+4)_PriTagCtl[1:0]	Port(8n+4) VLAN Output priority Tag/Untag Control.	RW	11
11:10	P(8n+5)_PriTagCtl[1:0]	Port(8n+5) VLAN Output priority Tag/Untag Control.	RW	11
13:12	P(8n+6)_PriTagCtl[1:0]	Port(8n+6) VLAN Output priority Tag/Untag Control.	RW	11
15:14	P(8n+7)_PriTagCtl[1:0]	Port(8n+7) VLAN Output priority Tag/Untag Control.	RW	11

## 11.10. 0x031D~0x037CH: VLAN Table Configuration Register

Each VLAN configuration entry requires three 16-bit registers. There are 32 VLAN configuration entries in the VLAN table. The VLAN configuration entry is combined with three registers: VLAN\_Entry\_Configuration\_0, 1, 2. For VLAN m, its format is defined as follows: m=0, 1, 2, .... 31.

### 11.10.1. Register VLAN(m)\_Entry\_Configuration\_0 (Addr: (0x031DH+3m))

**Table 72. Register VLAN(m)\_Entry\_Configuration\_0 (Addr: (0x031DH+3m))**

Bits	Name	Description	RW	Default
15:0	VLAN(m)_PM[15:0]	VLAN (entry m) Port Member, 24-bit map (bit 0~15). Bit value 0: Port is not a member of the VLAN Bit value 1: Port is a member of the VLAN	RW	-

### 11.10.2. Register VLAN(m)\_Entry\_Configuration\_1 (Addr: (0x031DH+3m+1))

**Table 73. Register VLAN(m)\_Entry\_Configuration\_1 (Addr: (0x031DH+3m+1))**

Bits	Name	Description	RW	Default
7:0	VLAN(m)_PM[23:16]	VLAN(m) Port Member 24-bit map (bit 16~23). Bit value 0: Port is not a member of the VLAN Bit value 1: Port is a member of the VLAN	RW	-
15:8	Reserved			

### 11.10.3. Register VLAN(m)\_Entry\_Configuration\_2 (Addr: (0x031DH+3m+2))

**Table 74. Register VLAN(m)\_Entry\_Configuration\_2 (Addr: (0x031DH+3m+2))**

Bits	Name	Description	RW	Default
11:0	VLAN(m)_VID[11:0]	VLAN(m) VID[11:0] bit 11~0. Each VLAN must be assigned a 12-bit VID.	RW	0
15:12	Reserved			

## 11.11. 0x037D~0x037EH: Insert Per-Port VID (PVID) Enabling Register

### 11.11.1. 0x037D: Insert Per-Port VID (PVID) Enabling Register 0 (P15~P0)

**Table 75. Insert Per-Port VID (PVID) Enabling Register 0**

Bits	Name	Description	RW	Default
15:0	InsPVID_0[15:0]	To enable per-port insert PVID function (P15-P0). 0: Disable (default) 1: Enable	RW	0

### 11.11.2. 0x037E: Insert Per-Port VID (PVID) Enabling Register 1 (P23~P16)

**Table 76. Insert Per-Port VID (PVID) Enabling Register 1**

Bits	Name	Description	RW	Default
7:0	InsPVID_1[7:0]	To enable per-port insert PVID function. (P23-P16) 0: Disable (default) 1: Enable	RW	0
15:8	Reserved			



## 11.12. QoS Configuration Register

### 11.12.1. 0x0400H: QoS Control Register

**Table 77. 0x0400H: QoS Control Register**

Bits	Name	Description	RW	Default
0	EnDSPri	Enable TCP/IP TOS/DS (DiffServ) based Priority QoS. 0: Disabled (Default) 1: Enabled When enabled, the priority definition is defined as follows: High Priority: If TOS/DS[0:5]: (EF) ‘101110’; (AF) ‘001010’, ‘010010’, ‘011010’, ‘100010’; (Network Control) ‘11x000’ Low Priority: TOS/DS = Other codepoint values <i>Note 1: The DS[0:5] bit location is equal to the mapping of TOS[0:5] = {precedence[2:0], Delay, Throughput, Reliability}.</i> <i>Note 2: DS=Differentiated Services, EF= Expected Forwarding, AF= Assured Forwarding.</i>	RW	0
1	En8021pPri	Enable 802.1p VLAN Tag Based Priority QoS Function. 0: Disable (Default) 1: Enable	RW	0
2	EnFCAutoOff	Enable Flow Control Ability Auto Turn Off for QoS. Enabled: Enables auto turn off of a port’s queue flow control ability for 1~2 seconds whenever the port receives a high priority frame. The flow control ability of this port is re-enabled when no high priority frames are received at this port during a 1~2 second period. Disabled: When EnFCAutoOff is disabled, the flow control ability of this port for any packet will be enabled as it was set. 0: Disabled (Default) 1: Enabled	RW	0
4:3	QWEIGHT[1:0]	Weighted round robin ratio setting of priority queue. The frame service rate of High-pri queue to Low-pri queue is: 00: 4:1 (Default) 01: 8:1 10: 16:1 11: High priority queue first always	RW	00
15:5	Reserved			

### 11.12.2. 0x0401: Port Priority Configuration Register 0

**Table 78. 0x0401: Port Priority Configuration Register 0**

Bits	Name	Description	RW	Default
15:0	PortPriCfg[15:0]	Port-based Priority setting (Port0 ~ Port15). Sets the priority QoS based on the physical port. If a port is set as a high priority port, all packets received from that port will be treated as high priority packets. Bit value 1: Sets that port as a high priority port Bit value 0: Sets that port as a low priority port <i>Note: Ports 0~15 map to bits 0~15.</i>	RW	0

### 11.12.3. 0x0402: Port Priority Configuration Register 1

**Table 79. 0x0402: Port Priority Configuration Register 1**

Bits	Name	Description	RW	Default
7:0	PortPriCfg[23:16]	Port based Priority setting (Port16 ~ Port23). Sets the priority QoS based on the physical port. If a port is set as a high priority port, all packets received from that port will be treated as high priority packets. Bit value 1: Sets that port as a high priority port Bit value 0: Sets that port as a low priority port <i>Note: Ports 16~23 map to bits 0~7.</i>	RW	0
15:8	Reserved			

## 11.13. PHY Access Control Register

### 11.13.1. 0x0500H: PHY Access Control Register

**Table 80. 0x0500H: PHY Access Control Register**

Bits	Name	Description	RW	Default
4:0	REG_addr	PHY Register address setting for the PHY Access command.	RW	0
9:5	PHY_ID[4:0]	PHY ID (PHY address) setting for the PHY Access command. RTL8324 connected PHY ID is fixed as: Fast Ethernet Port0 ~ 15. PHY ID: 16,17, ..., 30, 31. Fast Ethernet Port16 ~ 23. PHY ID: 8,9, ..., 14, 15.	RW	0
13:10	Reserved			0
14	PHY_RW	PHY Access Command. 0: PHY Access Read command (Default) 1: PHY Access Write command	RW	0
15	PHYCmdExeSta	PHY Access Command Execution Status. 0: Idle (Default) 1: Busy	R	0

### 11.13.2. 0x0501H: PHY Access Write Data Register

**Table 81. 0x0501H: PHY Access Write Data Register**

Bits	Name	Description	RW	Default
15:0	PHY_WD[15:0]	PHY Access Write Out Data (16 bits).	RW	0

### 11.13.3. 0x0502H: PHY Access Read Data Register

**Table 82. 0x0502H: PHY Access Read Data Register**

Bits	Name	Description	RW	Default
15:0	PHY_RD[15:0]	PHY Access Read In Data (16 bits).	R	0

## 11.14. Port Control Register

### 11.14.1. 0x0607H: Global Port Control Register

**Table 83. 0x0607H: Global Port Control Register**

Bits	Name	Description	RW	Default
0	DisFDFC  ( $\overline{\text{EnFDFC}}$ )	Disable Full Duplex Flow Control (802.3x PAUSE ability). This control bit will be applied to the switch only when a software reset is sent to the switch. This function can also be directly controlled by PHY register access through the PHY Access Control Register 0: Enable 802.3x Pause ability (Default) 1: Disable 802.3x Pause ability	RW	0 HW pin: EnFDFC
1	DisBKP  ( $\overline{\text{EnBKP}}$ )	Globally Disable Half Duplex Back Pressure Flow Control Ability. Set to globally disable the back pressure flow control ability of all ports. 0: Enable back pressure flow control ability (Default) 1: Disable back pressure flow control ability	RW	0 HW pin. EnBKP
2	DisBCSFC	Disable Broadcast Packet Strict Flood Control. This control function is used under 802.3x flow control mode. Strict flood mode will drop broadcast packets (DA: FF-FF-FF-FF-FF-FF) if any destination port member is congested. Loose flood mode allows broadcast packets to be flooded to all non-congested ports. 0: Enable Broadcast Packet Strict Flood (Strict flood mode) (default) 1: Disable Broadcast Packet Strict Flood (Loose flood mode)	RW	0 HW pin. DisBCSFC

Bits	Name	Description	RW	Default
3	DisIPMCFC	Disable IP Multicast Packet Strict Flood Control. This control function is used under 802.3x flow control mode. Strict flood mode will drop IP Multicast packets (DA: 01-00-5E-XX-XX-XX) if any destination port member is congested. Loose flood mode allows IP multicast packets to be flooded to all non-congested ports. 0: Enable IP Multicast Packet Strict Flood (Loose flood mode) (default) 1: Disable IP Multicast Packet Strict Flood (Strict flood mode)	RW	0
4	DisBRDCTRL ( $\overline{\text{EnBRDCTRL}}$ )	Disable Broadcast Storm Filtering Control. Set to disable the broadcast storm filtering control function. 1: Disable Broadcast storm filtering control (Default) 0: Enable Broadcast storm filtering control	RW	1 HW pin: EnBRDCTRL
15:5	Reserved			

### 11.14.2. 0x0608H: Port Disable Control Register 0

**Table 84. 0x0608H: Port Disable Control Register 0**

Bits	Name	Description	RW	Default
15:0	PortDisable[15:0]	Port Enable/Disable Control for ports 0~15. Bit value 0: Port enable Bit value 1: Port disable When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets. <i>Note: Ports 0~15 map to bits 0~15.</i>	RW	0

### 11.14.3. 0x0609H: Port Disable Control Register 1

**Table 85. 0x0609H: Port Disable Control Register 1**

Bits	Name	Description	RW	Default
7:0	PortDisable[23:16]	Port Enable/Disable Control for ports 16~23. Bit value 0: Port enable Bit value 1: Port disable When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets. <i>Note: Ports 16~23 map to bits 0~7.</i>	RW	0
15:8	Reserved			

### 11.14.4. 0x060AH~0x0615. Port Property Configuration Register 0 ~ 11

For Port(2n) and Port(2n+1) the Port Property is defined as follows: n = 0, 1, 2, . . . , 11 (Addr: 0x060AH +n); where n=0~11 for Fast Ethernet ports.

**Table 86. 0x060AH~0x0615. Port Property Configuration Register 0 ~ 11**

Bits	Name	Description	RW	Default
7:0	P(2n)_Property[7:0]	Port(2n) Port Property configuration. Bit [3:0]: Media Capability[3:0]= (100F, 100H, 10F, 10H). Bit [5]: Pause ability (1: Enable). Bit [6]: AsyPause ability (Asynchronous Pause) (1. enable) Bit [7]: Enable Auto Negotiation (1: Enable).	RW	100M. 0xAF
15:8	P(2n+1)_Property[7:0]	Port(2n+1) Port property configuration. Bit [3:0]: Media Capability[3:0]= {100F, 100H, 10F, 10H}. Bit [5]: Pause ability (1: Enable). Bit [6]: AsyPause ability ( Asynchronous Pause) (1: Enable). Bit [7]: Enable Auto Negotiation (1: Enable).	RW	100M. 0xAF

*Note: A configuration update of these registers requires a software reset (via write Reg. 0x0000 bit 0 =1) to force the configuration to be written to the PHY register and restart the auto-negotiation process.*

### 11.14.5. 0x0619H~0x0624. Port Link Status Register 0 ~ 11

For Port(2n) and Port(2n+1) the Port Properties are defined as follows:  
(n: 0,1,2,.. ..., 11) (Addr: 0x0619H +n).

**Table 87. 0x0619H~0x0625. Port Link Status Register 0 ~ 11**

Bits	Name	Description	RW	Default
7:0	P(2n)_LinkStatus[7:0]	<p>Port (2n) Port Link Status.</p> <p>Bit [1:0]: Link speed[1:0]: 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: NA.</p> <p>Bit [2]: Full duplex: 0: Half duplex 1: Full duplex Bit[3]: Reserved.</p> <p>Bit [4]: Link up: 0: Link down 1: Link up</p> <p>Bit [5]: Flow control (back pressure or 802.3x): For ports 0~23 (Fast Ethernet ports). Defined as Pause ability. In half duplex mode. Defined as back pressure ability. 0: Flow control disabled 1: Flow control enabled</p> <p>Bit [6]: AsyPause ability (Asymmetric Pause): For ports 0~23 (Fast Ethernet ports) Don't Care. In half duplex mode. Don't Care. 0: Flow control disabled 1: Flow control enabled</p> <p>Bit [7]: Enable Auto Negotiation (AN): 0: Disable AN 1: Enable AN</p>	R	0

Bits	Name	Description	RW	Default
15:8	P(2n+1)_LinkStatus[7:0]	<p>Port(2n+1) Port Link Status.</p> <p>Bit [1:0]: Link speed[1:0]:            00: 10Mbps            01: 100Mbps            10: 1000Mbps            11: NA.</p> <p>Bit [2]: Full duplex:            0: Half duplex            1: Full duplex</p> <p>Bit[3]: Reserved.</p> <p>Bit [4]: Link up:            0: Link down            1: Link up</p> <p>Bit [5]: Flow Control (back pressure or 802.3x):            For ports 0~23 (Fast Ethernet ports). Defined as Pause ability.            In half duplex mode. Defined as back pressure ability.            0: Flow control disabled            1: Flow control enabled</p> <p>Bit [6]: AsyPause ability (Asymmetric Pause):            For ports 0~23 (Fast Ethernet ports) Don't Care.            In half duplex mode. Don't Care.            0: Flow control disabled            1: Flow control enabled</p> <p>Bit [7]: Enable Auto Negotiation (AN):            0: Disable AN            1: Enable AN</p>	R	0

## 12. MIB Counter Register

### 12.1. *0x0700H~0x070BH: Port MIB Counter Object Selection Register 0~11*

For Port(2n), Port(2n+1), the Port MIB Counter Object Selection Register is defined as follows:  
n = 0, 1, 2, ..., 11) (Addr=0x0700H +n).

**Table 88. 0x0700H~0x070BH: Port MIB Counter Object Selection Register 0~11**

Bits	Name	Description	RW	Default
1:0	P(2n)CNT1_MIBS [1:0]	Port(2n) Counter_1 MIB Object Selection. P(2n)CNT_1_MIBS [1:0] 00: MIB object: RX byte count 01: MIB object: RX packet count (Default) 10: MIB object: CRC error packet count 11: MIB object: Collision packet count  RX byte count. This counter is incremented once for every data byte of a received and forwarded packet (includes both good and bad packets). RX packet count. This counter is incremented once for every received and forwarded packet (includes both good and bad packets).	RW	01
3:2	P(2n)CNT2_MIBS [1:0]	Port(2n) Counter_2 MIB Object Selection. P(2n)CNT_2_MIBS [1:0] 00: MIB object: TX byte count 01: MIB object: TX packet count (Default) 10: MIB object: CRC error packet count 11: MIB object: Collision packet count  TX byte count. This counter is incremented once for every data byte of a transmitted packet (includes both good and bad packets). TX packet count. This counter is incremented once for every transmitted packet (includes both good and bad packets).	RW	01



Bits	Name	Description	RW	Default
5:4	P(2n)CNT3_MIBS [1:0]	Port(2n) Counter_3 MIB Object Selection P(2n)CNT_3_MIBS [1:0] 00: MIB object: Drop byte count 01: MIB object: Drop packet count (Default) 10: MIB object: CRC error packet count 11: MIB object: Collision packet count  Drop packet count. This counter is incremented once for every drop of a received packet. Packet drop events could be due to undersize, oversize, CRC error, lack of resources, local packet, point-to-point control packet (ex. Pause packet, LACP packet). CRC error packet count. This counter is incremented once for every received packet with a valid length but with a CRC error. Collision packet counter. This counter is incremented once for every collision event detected.	RW	01
7:6	P(2n+1)CNT1_MIBS [1:0]	Port(2n+1) Counter_1 MIB Object Selection.	RW	01
9:8	P(2n+1)CNT2_MIBS [1:0]	Port(2n+1) Counter_2 MIB Object Selection.	RW	01
11:10	P(2n+1)CNT3_MIBS [1:0]	Port(2n+1) Counter_3 MIB Object Selection.	RW	01

## 12.2. *0x070DH ~0724H: Port MIB Counter 1 Register (RX Counter) (32 bits)*

The MIB counters are 32-bit counters. After power on reset, the counters are all reset to 0. A read access of the MIB counter will NOT reset the counter to 0. When a MIB counter MIB object is changed, then the counter will be reset to 0 and the count will restart.

The time before the next read of the same counter should not be longer than the counter's timeout. The timeout of the 32-bit MIB counter depends on the object type and the port speed, and is calculated as follows:

Packet counter timeout is calculated based on 64-byte packets and byte counter timeout is calculated based on 1518 byte packets).

**Table 89. MIB Counter Timeout**

Port Speed	MIB Object Type	MIB Counter Timeout (Sec.)
100Mbps	Packet count	28862
	Byte count	348
10Mbps	Packet count	288621
	Byte count	3481

### 12.2.1. For Port(n) MIB Counter 1 Register (32-bit). n=0, 1, 2, ... 23 (Addr: 0x070DH+n)

**Table 90. 0x070DH ~0724H: Port MIB Counter 1 Register (RX Counter) (32 bits)**

Bits	Name	Description	RW	Default
31:0	Port(n)_MIB_CNT_1[31:0]	Port(n) MIB Counter_1[31:0]	R	0

### 12.2.2. 0x0727~073EH: Port MIB Counter 2 Register (TX Counter) (32-bits)

For Port(n) MIB Counter 2 Register (32-bit): n = 0, 1, 2, ... 23 (Addr: 0x0727H+n).

**Table 91. 0x0727~073EH: Port MIB Counter 2 Register (TX Counter) (32 bits)**

Bits	Name	Description	RW	Default
31:0	Port(n)_MIB_CNT_2[31:0]	Port(n) MIB Counter_2[31:0]	R	0

### 12.2.3. 0x0741~0758H: Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

For Port(n) MIB Counter 3 Register (32-bit): n = 0, 1, 2, ... 23 (Addr: 0x0741H+n).

**Table 92. 0x0741~0758H: Port MIB Counter 3 Register (Diagnostic Counter) (32 bits)**

Bits	Name	Description	RW	Default
31:0	Port(n)_MIB_CNT_3[31:0]	Port(n) MIB Counter_3[31:0]	R	0

## 13. Characteristics

### 13.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device or which may affect device reliability. All voltages are specified reference to GND unless otherwise specified.

**Table 93. Absolute Maximum Ratings**

Parameter	Min	Max	Units
Storage Temperature	-10	+125	°C
DVDD, RVDD, AVDD Supply Referenced to GND	GND-0.3	+3.63	V
VDD Supply Reference to GND	GND-0.3	+1.98	V
Digital Input Voltage	GND-0.3	DVDD+0.3	V

### 13.2. Operating Range

**Table 94. Operating Range**

Parameter	Min	Max	Units
Ambient Operating Temperature	0	70	°C
3.3V Vcc Supply Voltage Range (RVDD, DVDD)	3.15	3.45	V
1.8V Vcc Supply Voltage Range (VDD)	1.71	1.89	V

### 13.3. DC Characteristics

Supply Voltage VDD: 3.3V ± 5%.

**Table 95. DC Characteristics**

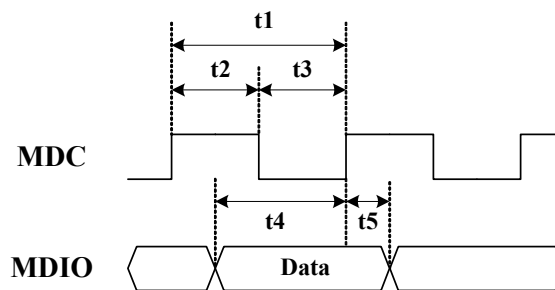
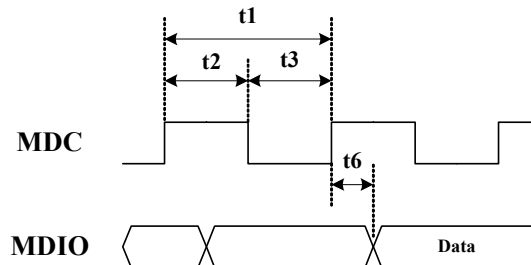
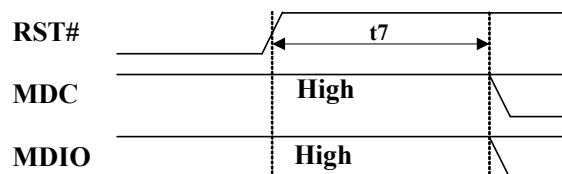
Parameter	Pin Name	Condition	Min	Typical	Max	Units
Power Supply Current	I <sub>cc</sub>	24FE, wire-speed traffic load			280	mA
		24FE all idle			170	
Total Power Consumption	PS	24FE, wire-speed traffic load			924	mW
		24FE all idle			561	
TTL Input High Voltage	V <sub>ih</sub>		2.0			V
TTL Input Low Voltage	V <sub>il</sub>				0.8	V
TTL Input Current	I <sub>in</sub>		-10		10	μA
TTL Input Capacitance	C <sub>in</sub>			2.9		pF
Output High Voltage	V <sub>oh</sub>		2.6		3.6	V
Output Low voltage	V <sub>ol</sub>		0		0.4	V

## 13.4. AC Characteristics

### 13.4.1. PHY Management (SMI) Timing

**Table 96. PHY Management (SMI) Timing**

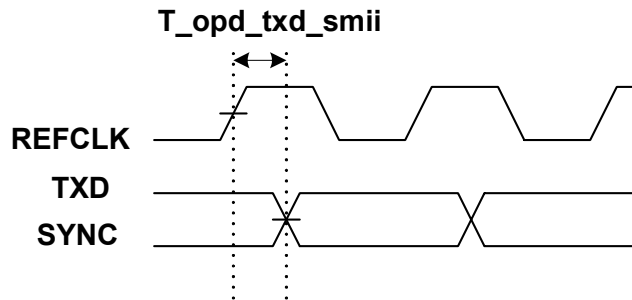
Pin Name	Description	Minimum	Typical	Maximum	Units
t1	MDC clock period	-	1360	-	ns
t2	MDC high level width	-	680	-	ns
t3	MDC low level width	-	680	-	ns
t4	MDIO to MDC rising setup time (Write Bits)		680	-	ns
t5	MDIO to MDC rising hold time (Write Bits)		680	-	ns
t6	MDC to MDIO delay (Read Bits)	20	-	-	ns
t7	MDC/MDIO activates from RST# deasserted	-	45	-	ms


**Figure 14. MDC/MDIO Write Timing**

**Figure 15. MDC/MDIO Read Timing**

**Figure 16. MDC/MDIO Reset Timing**

### 13.4.2. SMII Transmit Timing

**Table 97. PHY Management (SMI) Timing**

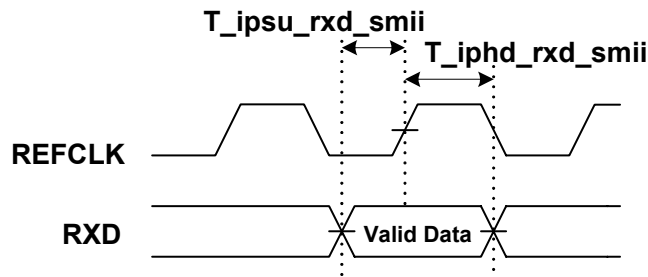
Pin Name	Description	Minimum	Typical	Maximum	Units
T_opd_txd_smii	REFCLK rising edge to TXD (SYNC) delay.	2	4	5	ns


**Figure 17. SMII Transmit Timing**

### 13.4.3. SMII Receive Timing

**Table 98. SMII Receive Timing**

Pin Name	Description	Minimum	Typical	Maximum	Units
T_ipsu_rxd_smii	RXD setup time to REFCLK.	2			ns
T_iphd_rxd_smii	RXD hold time from REFCLK.	1.5			ns


**Figure 18. SMII Receive Timing**

## 14. Thermal Data

### Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip ( $T_j$ , junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment ( $T_a$ , ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible  $T_a$  is outlined below.

Thermal parameters are defined according to JEDEC standard JESD 51-2, 51-6:

$\theta_{JA}$  (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower  $\theta_{JA}$  means better thermal performance.

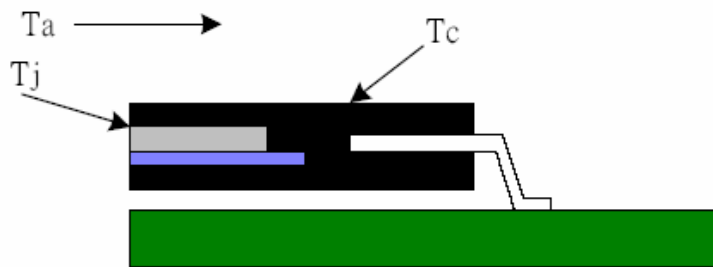
$\theta_{JA} = (T_j - T_a) / P_h$ , where  $T_j$  is the junction temperature

$T_a$  is the ambient temperature

$P_h$  is the power dissipation

$\theta_{JC}$  (Thermal resistance from junction to case), represents resistance to heat flow from the chip to the package top case.  $\theta_{JC}$  is important when an external heat sink is attached on the package top.

$\theta_{JC} = (T_j - T_c) / P_h$ , where  $T_j$  is the junction temperature.



**Figure 19. Cross-section of 128-Pin PQFP**

## Thermal Operating Range

**Table 99. Thermal Operating Range**

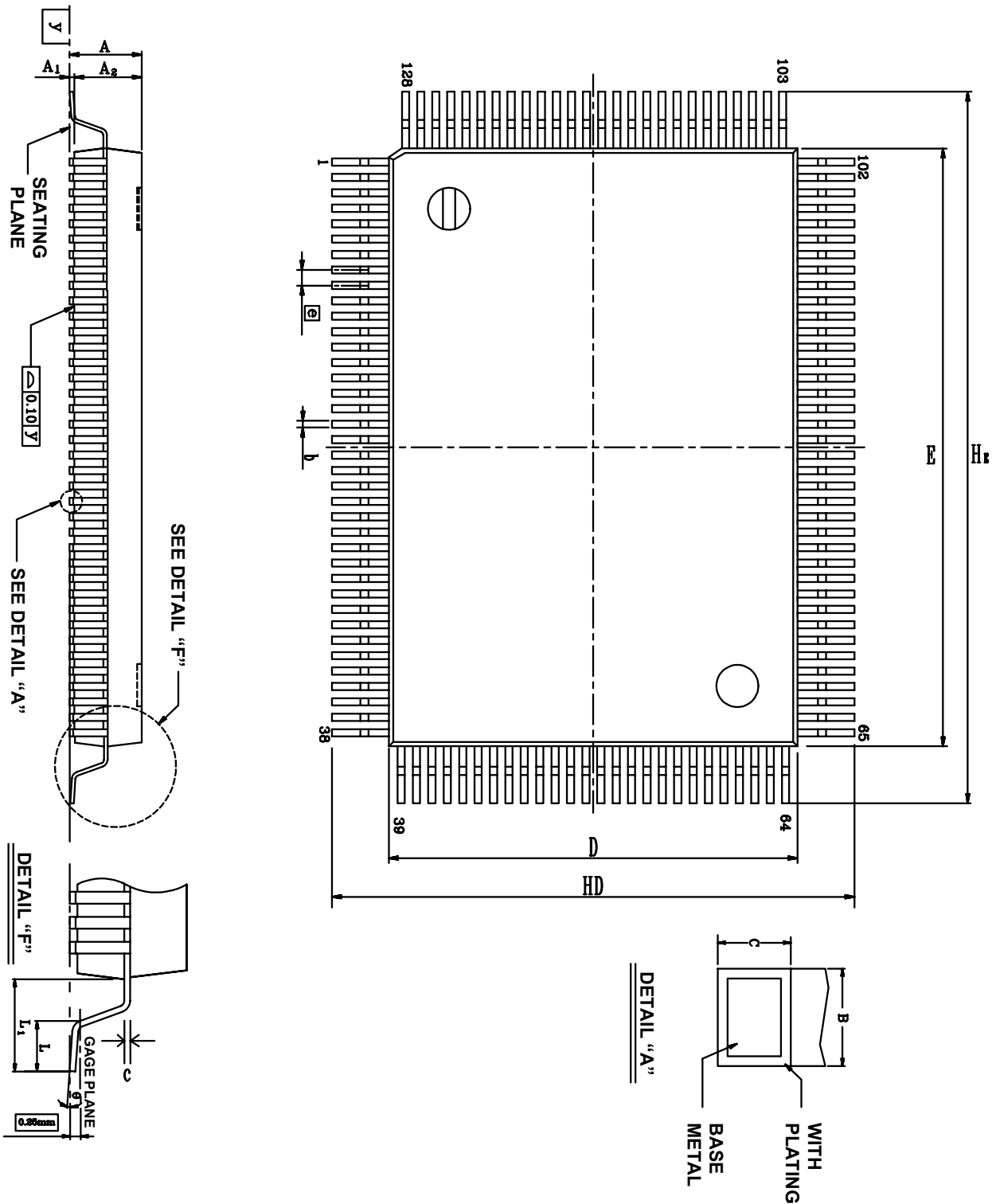
Parameter	SYM	Min	Typical	Max	Units
Junction operating temperature	T <sub>j</sub>		25	125	°C
Junction operating temperature	T <sub>a</sub>		25	70	°C

## Thermal Resistance

**Table 100. Thermal Resistance**

Parameter	SYM	Conditions	Min	Typical	Max	Units
Thermal resistance: junction to ambient	$\theta_{JA}$	2 layer PCB, 0 ft/s airflow		48.5		°C/W
Thermal resistance: junction to case	$\theta_{JC}$	2 layer PCB, 0 ft/s airflow		16.4		°C/W

## 15. Mechanical Information



See the Mechanical Dimensions notes on the next page.



## 15.1. Mechanical Dimensions Notes

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
<b>A</b>	-	-	0.134	-	-	3.40
<b>A1</b>	0.004	0.010	0.036	0.10	<b>0.25</b>	0.91
<b>A2</b>	0.102	0.112	0.122	2.60	<b>2.85</b>	3.10
<b>b</b>	0.005	0.009	0.013	0.12	<b>0.22</b>	0.32
<b>c</b>	0.002	0.006	0.010	0.05	<b>0.15</b>	0.25
<b>D</b>	0.541	0.551	0.561	13.75	<b>14.00</b>	14.25
<b>E</b>	0.778	0.787	0.797	19.75	<b>20.00</b>	20.25
<b>e</b>	0.010	0.020	0.030	0.25	<b>0.5</b>	0.75
<b>HD</b>	0.665	0.677	0.689	16.90	<b>17.20</b>	17.50
<b>HE</b>	0.902	0.913	0.925	22.90	<b>23.20</b>	23.50
<b>L</b>	0.027	0.035	0.043	0.68	<b>0.88</b>	1.08
<b>L1</b>	0.053	0.063	0.073	1.35	<b>1.60</b>	1.85
<b>y</b>	-	-	0.004	-	-	0.10
<b>θ</b>	0°	-	12°	0°	-	12°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

TITLE: -CU L/F, PQFP FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1.2
		PAGE	
CHECK		DWG NO.	Q128 - 1
		DATE	
REALTEK SEMICONDUCTOR CORP.			

## 16. Ordering Information

**Table 101. Ordering Information**

Part Number	Package	Status
RTL8324	PQFP-128	Available Now
RTL8324-LF	RTL8324 with Lead (Pb)-Free package	Available Now

Note: See page 5 for lead (Pb)-free package identification.

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