

## DM74AS174 Hex D Flip-Flop with Clear

### General Description

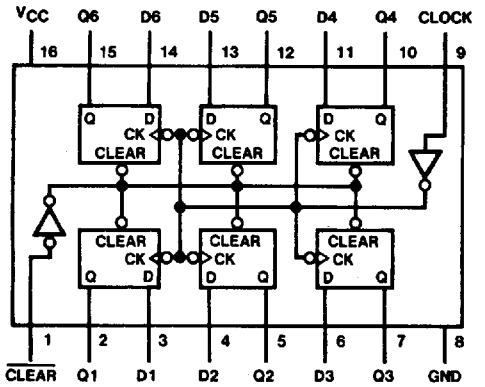
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. This device has an asynchronous clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either a high or low level, the D input signal has no effect at the output.

### Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Pin and functional compatible with LS and Schottky family counterpart
- Switching performance guaranteed over full temperature and  $V_{CC}$  supply range

### Connection Diagram



TL/F/8655-1

Order Number DM74AS174N  
See NS Package Number N16A\*

### Function Table

Inputs			Output
CLEAR	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

H = High Logic State

L = Low Logic State

X = Either Low or High Logic State

$Q_0$  = The level of Q before the indicated steady-state input conditions were established.

↑ = Transition from Low Logic Level to High Logic Level

\*Contact your local NSC representative about surface mount (M) package availability.

## Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical $\theta_{JA}$ N Package	66.3°C/W

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
V <sub>IH</sub>	High Level Input Voltage	2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8	V
I <sub>OH</sub>	High Level Output Current			-2	mA
I <sub>OL</sub>	Low Level Output Current			20	mA
f <sub>CLOCK</sub>	Clock Frequency	0		100	MHz
t <sub>w</sub>	Pulse Width	Clock High	4		ns
		Clock Low	6		
		CLEAR	5		
t <sub>Setup</sub>	Setup Time	Data	4		ns
		CLEAR Inactive	6		
t <sub>HOLD</sub>	Data Input Hold Time	1			ns
T <sub>A</sub>	Operating Free Air Temperature Range	0		70	°C

## Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>IK</sub>	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High Level Output Voltage	I <sub>OH</sub> = Max, V <sub>CC</sub> = 4.5 to 5.5V	V <sub>CC</sub> - 2			V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = 4.5V, I <sub>OL</sub> = Max, V <sub>IH</sub> = 2V		0.35	0.5	V
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 7V			100	μA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 0.4V			-500	μA
I <sub>O</sub>	Output Drive Current	V <sub>CC</sub> = 5.5V, V <sub>O</sub> = 2.25V	-30		-112	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 5.5V (Note 2)		30	45	mA

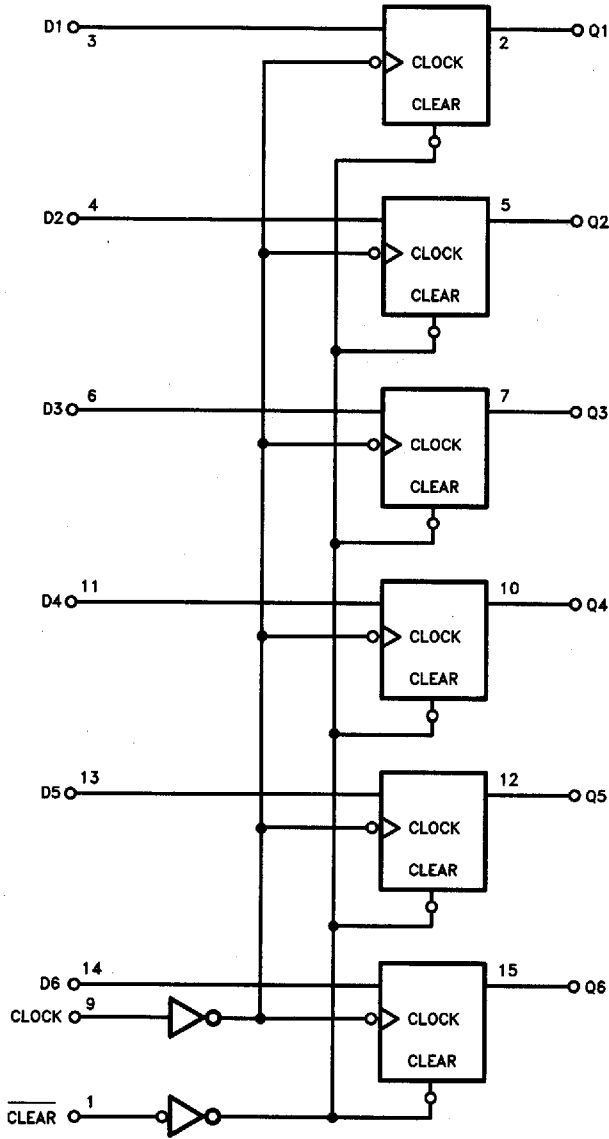
Note 2: I<sub>CC</sub> is measured with D inputs and CLR grounded and CLK at 4.5V.

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	Units
f <sub>MAX</sub>	Maximum Clock Frequency			V <sub>CC</sub> = 4.5V to 5.5V, C <sub>L</sub> = 50 pF, T <sub>A</sub> = Min to Max, R <sub>L</sub> = 500Ω	100		MHz
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	CLEAR	Q		5	14	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	Clock	Q		3.5	8	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	Clock	Q		4.5	10	ns

Note 1: See Section 5 for test waveforms and output load.

# Logic Diagram



TL/F/8655-2