ModelSim

ModelSim is a multi-language HDL simulation environment by Mentor Graphics,[1] for simulation of hardware description languages such as VHDL, Verilog and SystemC, and includes a built-in C debugger.[2][1] ModelSim can be used independently, or in conjunction with Intel Quartus Prime, Xilinx ISE or Xilinx Vivado.[3] Simulation is performed using the graphical user interface (GUI), or automatically using scripts. [4]

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LeonardoSpectrum is a multi-tiered product family that consists of three levels - Level 1, Level 2, and Level 3. Each level contains a bundle of features that provides users with a simple, fully integrated HDL synthesis environment. Users at any level of design complexity can find a LeonardoSpectrum level that provides logic synthesis results for their FPGA, CPLD, and ASIC designs.

All three levels are centered on a powerful logic synthesis engine. These levels offer best-inclass synthesis and optimization, and differ only in options.

Note: For more information on the LeonardoSpectrum standard features, options, and salient highlights refer to Chapter 1 in the LeonardoSpectrum User's Manual

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FPGA Compiler II is a powerful synthesis tool for leading FPGA architectures. With the tool, you can create optimized netlists from VHDL code, Verilog HDL code, and existing, unoptimized EDIF or Xilinx Netlist Format (XNF) netlists.

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Logic Synthesis for FPGA Design. *Synplify* Pro® FPGA synthesis software is the industry standard for producing high-performance and cost-effective FPGA designs. *Synplify* software supports the latest VHDL and Verilog language constructs including SystemVerilog and VHDL-2008.