NEC ELECTRONICS INC.

MOS INTEGRATED CIRCUIT
μPD7004C

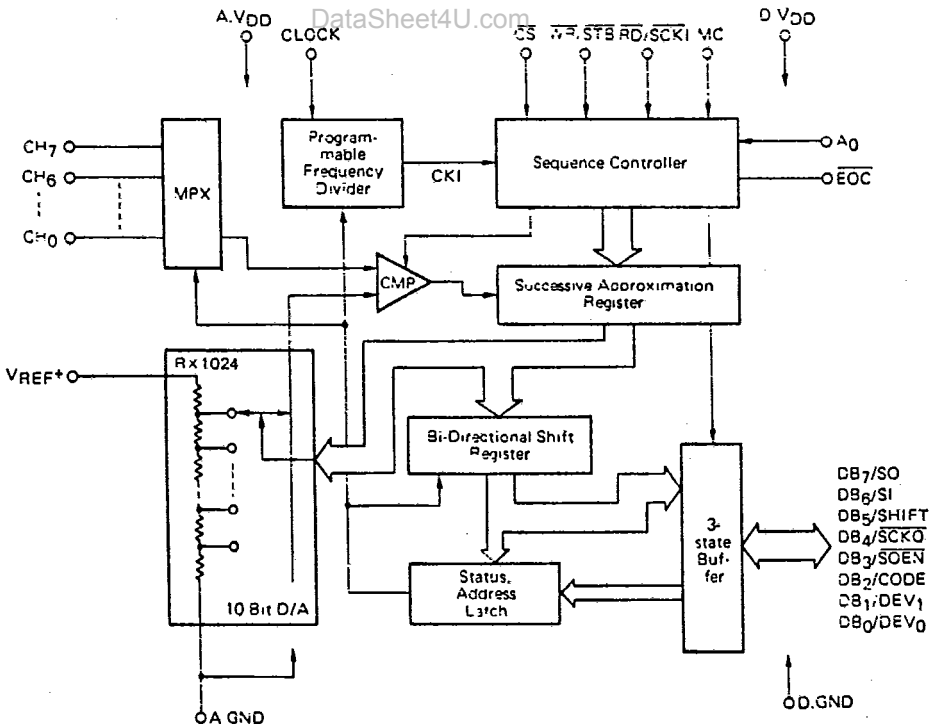
10-BIT CMOS SUCCESSIVE APPROXIMATION A/D CONVERTER

The μPD7004 is a 10-bit monolithic CMOS analog-to-digital converter using the Successive Approximation Register (SAR) technique. The μPD7004 incorporates an 8-channel multiplexed analog input and full microprocessor interface to achieve a high degree of versatility. The designer has a choice of either serial or parallel output and interface to 8080 type microprocessors or advanced signal processors like the μPD7720.

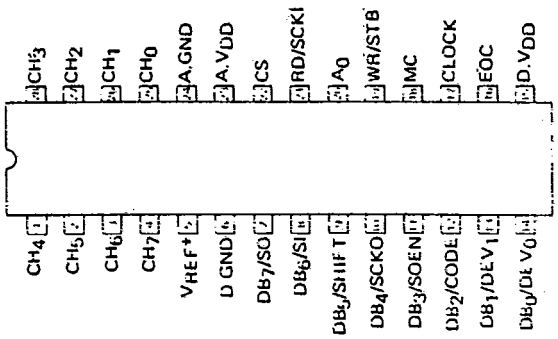
FEATURES

- 8-channel multiplexed analog input
- Serial or parallel interface
- 10-bit resolution
- Linearity: 1 LSB MAX. (T_a = 25 °C)
- Conversion time: 10 μs (f_{CLK} = 1 MHz)
- Input voltage range 0 to V_{REF}
- Temperature range from -40 to +85 °C
- Operates from single +5 volt supply (5 V ±10 %)

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



PIN IDENTIFICATION

Pin No.	Sumbol	Parallel mode		Serial mode	
		I/O	Function	I/O	Function
1	CH_4	Analog input CH_4			
2	CH_5	Analog input CH_5			
3	CH_6	Analog input CH_6			
4	CH_7	Analog input CH_7			
5	V_{REF}^+	Positive reference voltage input			
6	D.GND	Digital Ground Note			
7	DB_7/SO	Output	Data bus (MSB)	Output	Serial output
8	DB_6/SI	Output	Data bus (2nd)	Input	Serial input
9	DB_5/SHIFT	Output	Data bus (3rd)	Input	First-bit select (LSB/MSB)
10	$DB_4/\overline{SCKO}$	Output	Data bus (4th)	I/O	Serial clock output
11	$DB_3/\overline{SOEN}$	Output	Data bus (5th)	I/O	Serial-out enable
12	DB_2/CODE	I/O	Data bus (6th)	Input	Code select
13	DB_1/DEV_1	I/O	Data bus (7th)	Input	Division ratio set
14	DB_0/DEV_0	I/O	Data bus (LSB)	Input	Division ratio set
15	$D.V_{DD}$	Digital Power Supply Note			
16	$\overline{EOC}$	Output	End-of-conversion signal (Active low)		
17	CLOCK	Input	Clock signal input terminal		
18	MC	Input	Mode select (H=Parallel, L=Serial)		
19	$\overline{WR}/\overline{STB}$	Input	Write signal input	Input	Address-write strobe signal
20	A_0	Input	Control address input	Input	Internal/external serial clock select
21	$\overline{RD}/\overline{SCKI}$	Input	Read signal input	Input	Serial clock input
22	$\overline{CS}$	Input	Chip select signal		
23	$A.V_{DD}$	Analog Power Supply Note			
24	A.GND	Analog Ground Note			
25	CH_0	Analog input CH_0			
26	CH_1	Analog input CH_1			
27	CH_2	Analog input CH_2			
28	CH_3	Analog input CH_3			

Note: Connect to Digital Ground (D.GND) with Analog Ground (A.GND) externally.
Connect to Digital Power Supply ($D.V_{DD}$) with Analog Power Supply ($A.V_{DD}$) externally.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.3	V
Reference Voltage	V_{REF}	-0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -40 to +85 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	4.0		V_{DD}	V	
Analogue Input Voltage	V_I	0.0		V_{REF}	V	
High-level Input Voltage	V_{IH}	2.4			V	
Low-level Input Voltage	V_{IL}			0.8	V	
Clock Frequency	f_{CK}	0.4		8.8	MHz	
Internal Clock Frequency	f_{CKI}	0.4	1.0	1.1	MHz	$f_{CKI} = f_{CK}$ × Division ratio
Parallel Mode (MC = High)						
Address Setup Time	t_{AW}	20			ns	$\overline{CS}$ ↓, A_0 → $\overline{WR}$ ↓
	t_{AR}	20			ns	$\overline{CS}$ ↓, A_0 → $\overline{RD}$ ↓
Address Hold Time	t_{WA}	10			ns	$\overline{WR}$ ↑ → $\overline{CS}$ ↑, A_0
	t_{RA}	10			ns	$\overline{RD}$ ↑ → $\overline{CS}$ ↑, A_0
$\overline{WR}$ Signal Pulse Width	t_{WW}	200			ns	
$\overline{RD}$ Signal Pulse Width	t_{RR}	200			ns	
Data Setup Time	t_{DW}	100			ns	DB → $\overline{WR}$ ↑
Data Hold Time	t_{WD}	20			ns	$\overline{WR}$ ↑ → DB
Serial Mode 1 (MC = Low, A_0 = Low; External Serial Clock)						
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}$ ↓ → $\overline{CS}$ ↓
$\overline{CS}$ Setup Time	t_{SCSK}	1			μs	$\overline{CS}$ ↓ → $\overline{SCKI}$ ↓ (*)
Serial Input Setup Time	t_{SIK}	150			ns	SI → $\overline{SCKI}$ ↑
Serial Input Hold Time	t_{HKI}	100			ns	$\overline{SCKI}$ ↑ → SI
Low-level Serial Clock Pulse Width	t_{WLK}	400			ns	
High-level Serial Clock Pulse Width	t_{WHK}	400			ns	
Strobe Pulse Width	t_{WLST}	200			ns	
Strobe Hold Time	t_{HKST}	200			ns	$\overline{SCKI}$ ↑ → $\overline{STB}$ ↑
Chip Select Hold Time	t_{HKCS}	100			ns	$\overline{SCKI}$ ↑ → $\overline{CS}$ ↑

* f_{CKI} = 1 MHz

↑ ... Rising edge
↓ ... Falling edge

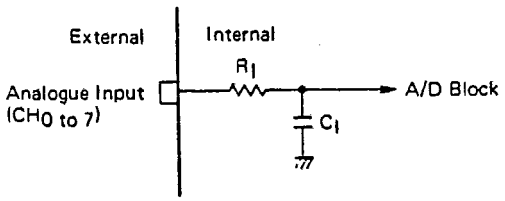
CONVERSION CHARACTERISTICS (T_a = 25 °C, V_{DD} = V_{REF} = 5.0 ±0.5 V, f_{CKI} = 1 MHz)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Resolution		10	10	10	Bit	T_a = −40 to +85 °C
Total Unajusted Error	NL			±1.0	LSB	
Total Unajusted Error				±2.0	LSB	T_a = −40 to +85 °C
Zero Scale Error				±0.5	LSB	
Zero Scale Temperature Coefficient			2		ppm/°C	T_a = −40 to +85 °C
Full Scale Error				±0.5	LSB	
Full Scale Temperature Coefficient			2		ppm/°C	T_a = −40 to +85 °C
Conversion Time	T_{CONV}	96		104	μs	Parallel Mode, Serial Mode 1
Conversion Time	T_{CONV}	104	104	104	μs	Serial Mode 2

DC CHARACTERISTICS (V_{DD} = V_{REF} = 5.0 ±0.5 V, T_a = −40 to +85 °C, f_{CKI} = 1 MHz)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
High-level Output Voltage	V_{OH}	3.5			V	I_O = −1.6 mA
Low-level Output Voltage	V_{OL}			0.4	V	I_O = 1.6 mA
Digital Input Leakage Current	I_{ID}			±10	μA	V_I = 0 to V_{DD}
Floating Output Leakage Current	I_{FO}			±10	μA	V_O = 0 to V_{DD}
Analog Input Resistance (DC)	R_I (DC)		2		MΩ	V_I = 0 to V_{DD}
Equivalent Analog Input Impedance (*)	RI		10		kΩ	The analogue input impedance is equivalent to the series circuit between RI and CI.
	CI		100		pF	
Reference Input Resistance	R_{REF}	5		50	kΩ	
Power Consumption	P_d		5	15	mW	

* Equivalent Circuit



Charge or discharge current flows at the internal multiplexer switching timing. Therefore, connect a capacitor (>0.01 μF) to the analog input terminal in case the external is high.

AC CHARACTERISTICS (V_{DD} = V_{REF} = 5 ±0.5 V, T_a = -40 to +85 °C, f_{CKI} = 1 MHz)

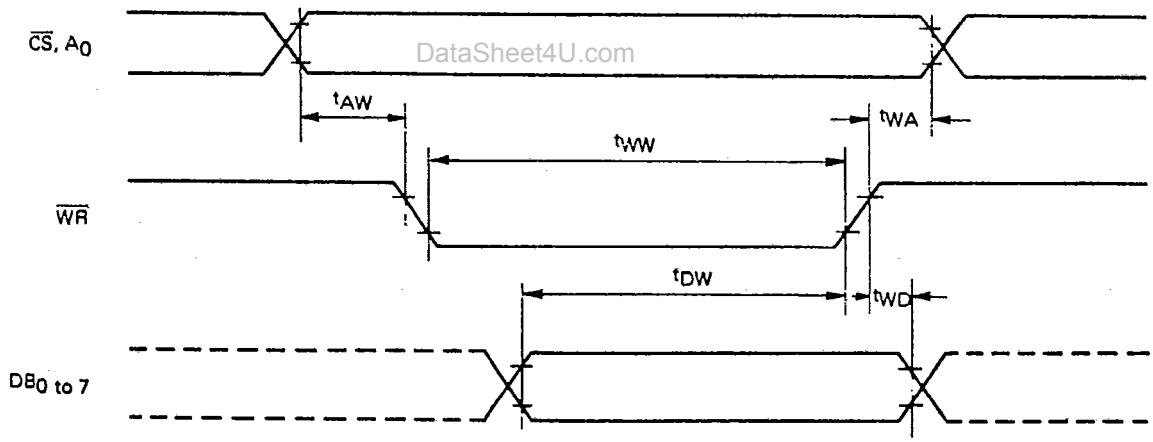
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Output Delay Time	t_{RD}			150	ns	$\overline{RD}$ ↓ → DB (Parallel Mode)
	t_{DKO}			250	ns	$\overline{SCKI}$ ↓, $\overline{SCKO}$ ↓ → SO (Serial Mode 1, 2)
Output Floating Delay Time	t_{DF}			100	ns	$\overline{RD}$ ↑ → DB Floating (Parallel Mode)
	t_{FCSO}			150	ns	$\overline{CS}$ ↑ → SO Floating (Serial Mode 1)
Serial-out Enable Delay Time	t_{SKS}	40		200	ns	$\overline{SCKO}$ ↑ → $\overline{SOEN}$ ↓ (Serial Mode 2)
Serial-out Enable Delay Time	t_{HKS}	0		200	ns	$\overline{SCKO}$ ↓ → $\overline{SOEN}$ ↑ (Serial Mode 2)
Serial Clock Output Cycle	t_{CYK}		$1/f_{CKI}$		ns	(Serial Mode 2)
High-level Serial Clock Pulse Width	t_{WHK}	400			ns	(Serial Mode 2)
Low-level Serial Clock Pulse Width	t_{WLK}	400			ns	(Serial Mode 2)
Serial Clock Rise Time	t_{rsc}		20		ns	(Serial Mode 2)
Serial Clock Fall Time	t_{fsc}		20		ns	(Serial Mode 2)

↑ ... Rising edge
↓ ... Falling edge

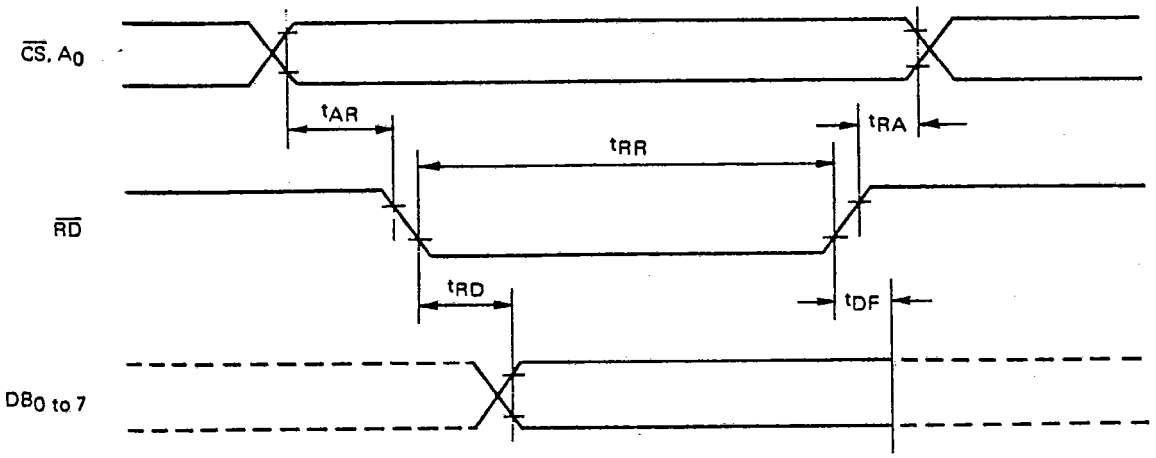
TIMING CHART

1. Parallel Mode

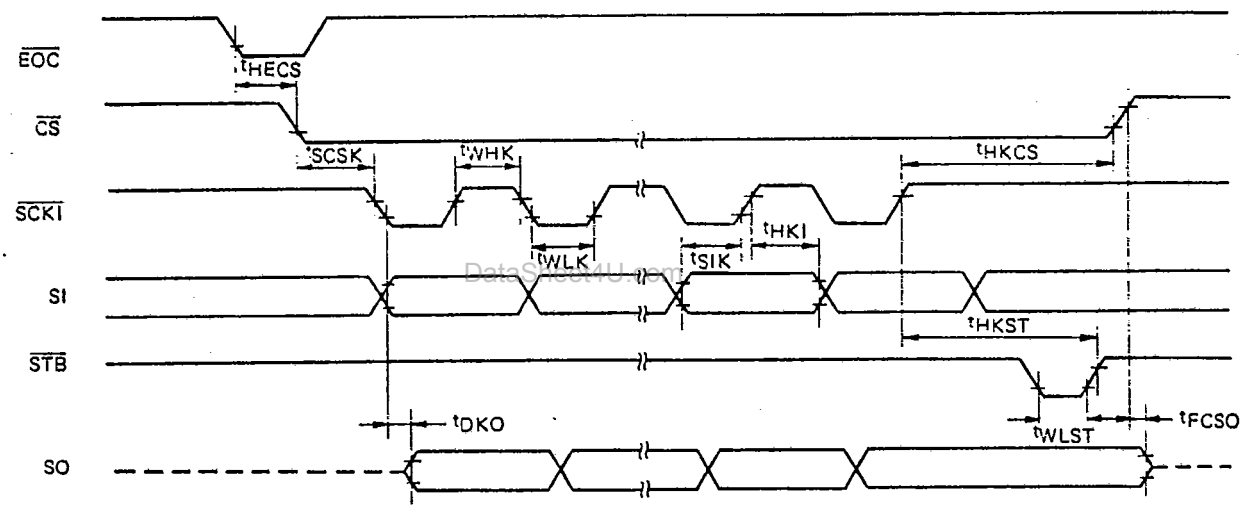
(1) Write Mode



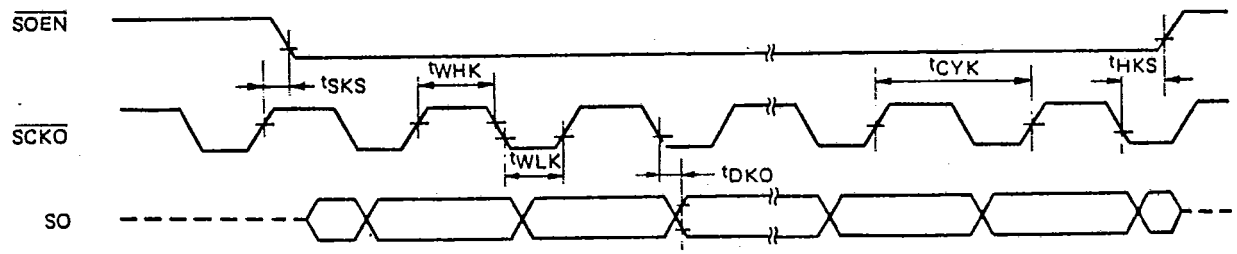
(2) Read Mode



2. Serial Mode 1



3. Serial Mode 2



INTERNAL BLOCK OPERATION

1. Sequence Controller

The sequence controller controls the operation of the comparator, internal sequence of the successive approximation register, and the 3-state buffers.

The A/D conversion starts in the parallel mode when the MPX address is written, and in the serial mode when the $\overline{CS}$ signal changes to the high level.

When the A/D conversion is terminated, the sequence controller issues an end-of-conversion signal ($\overline{EOC}$) to notify this to the external environment.

2. Successive Approximation Register

The successive approximation register sends signals to the decoder of the 10-bit D/A according to the control signals from the sequence controller and then decides to set or reset the signals for the decoder, starting with the MSB, with the help of the results from the comparator.

3. Bi Directional Shift Resister

This is the register into which the contents of the successive approximation register are entered. It outputs the converted data via 3-state buffers when in the parallel mode.

In serial mode 1, it outputs the converted data from the SO terminal when the $\overline{SIKI}$ signal falls and the $\overline{CS}$ signal is low, and fetches serial data (MPX address selector data) from the SI terminal when the $\overline{SCKI}$ signal rises.

In serial mode 2, 10-bit converted data accompanied by 6-bit high data is output from the SO terminal synchronously from the falling edge of the $\overline{SCKO}$ signal.

4. Status, Address Latch

The status and address latch are 3-bit registers to latch the clock division selector ratio data, code selector data of the conversion data, and selector data for the MPX address.

It reads the data entered from the data buses ($DB_{0\ to\ 7}$) in the parallel mode. In serial mode, it latches the division ratio selector data and code selector data specified by the multi-function terminals (DB_0/DEV_0, DB_1/DEV_1, DB_2/CODE) and also the MPX address selector data entered through the SI terminal.

However, that the MPX address is fixed at CH_7 and cannot be selected in serial mode 2.

5. Programmable Frequency Divider

The programmable frequency divider designates clock signals entered from the external circuit to one of the ratios 1/1, 1/2, 1/4, and 1/8.

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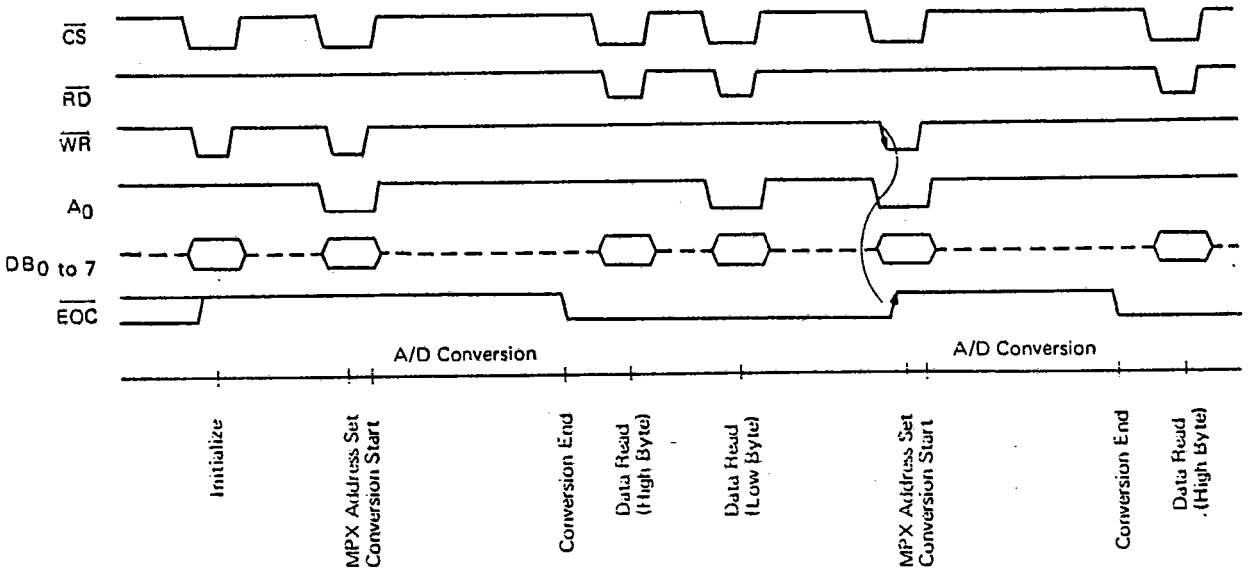
OPERATING MODE

The μPD7004, serving as an interface circuit with the microcomputer, supports two kinds of serial modes and a parallel mode.

1. Parallel Mode

The parallel mode allows a direct connection to the microprocessor data buses. Shown below is an example of the basic sequence;



The initialization designates the clock signal division ratio for the clock signal entered from the external environment and the conversion data code (2' s complement/binary). Normally, initialization is performed to initialize the peripheral circuits of the microcomputer. After initialization, the data entered is held until the next initialization. Writing the MPX address into the μPD7004 ($\overline{WR}$ signal) after the initialization makes the A/D conversion start from the rising edge of $\overline{WR}$ signal.

The A/D conversion requires f_{CKI} (internal clock: f_{CK} X division ratio) to be 96 to 104 cycles. The $\overline{EOC}$ signal changes to the low level when the A/D conversion is complete to notify this to the external environment. The 10-bit converted data is read out from the μPD7004 eight bits at a time. The low byte has valid data in its two high-order bits, followed by six "0"s in the rest (DB_5 to DB_0).

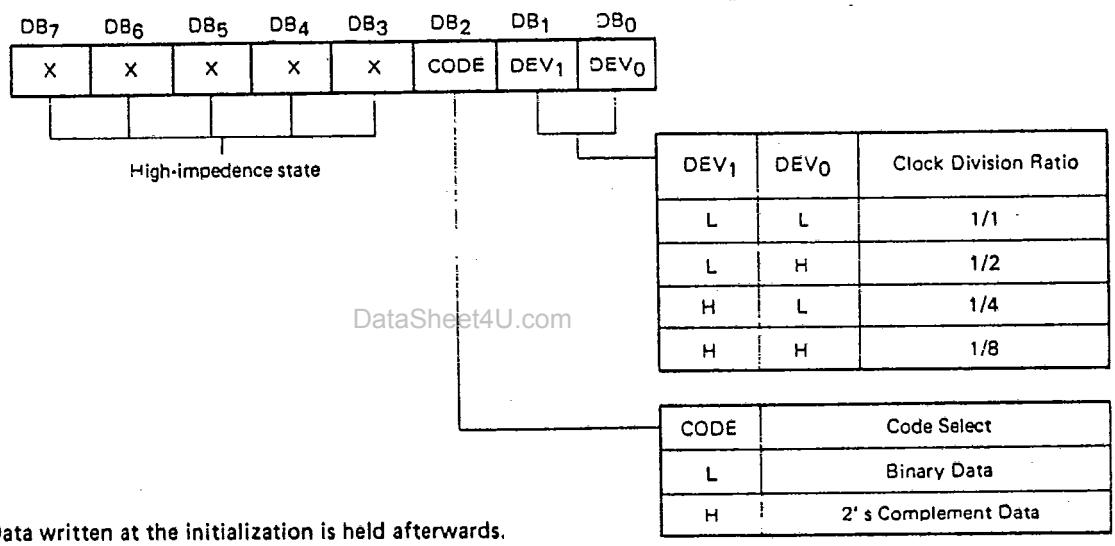
Resetting the MPX address starts the next A/D conversion, changing the $\overline{EOC}$ signal to the high level at the falling edge of $\overline{WR}$ signal.

Data Bus I/O Operation (parallel mode MC = H)

Control terminal				Operation	Serves as a data bus terminal
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0		
H	X	X	X	No Operation	High-impedance State
L	H	H	X		
L	L	H	H	Initialize	Code Select, Clock Division Ratio Input
L	L	H	L	Address Set	Analogue Channel Select Data Input
L	H	L	H	High-byte Read	High-byte Data Output
L	H	L	L	Low-byte Read	Low-byte Data Output
L	L	L	X	Inhibit	–

(1) Initialize

In the parallel mode, the initialization data for the clock division ratio and the A/D conversion data code are written into the μPD7004 through data buses.



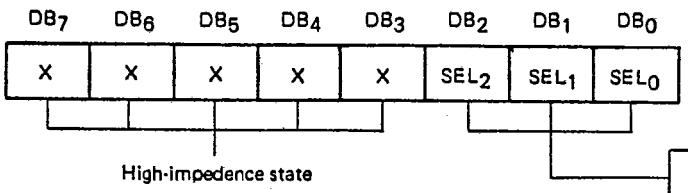
DEV_1	DEV_0	Clock Division Ratio
L	L	1/1
L	H	1/2
H	L	1/4
H	H	1/8

CODE	Code Select
L	Binary Data
H	2's Complement Data

Data written at the initialization is held afterwards.

(2) Address set

The selector data for the analog channel is written into the μPD7004.



SEL_2	SEL_1	SEL_0	MPX Channel
L	L	L	CH_0
L	L	H	CH_1
L	H	L	CH_2
L	H	H	CH_3
H	L	L	CH_4
H	L	H	CH_5
H	H	L	CH_6
H	H	H	CH_7

(3) High-byte/low-byte read

The A/D conversion data is read from the μPD7004.

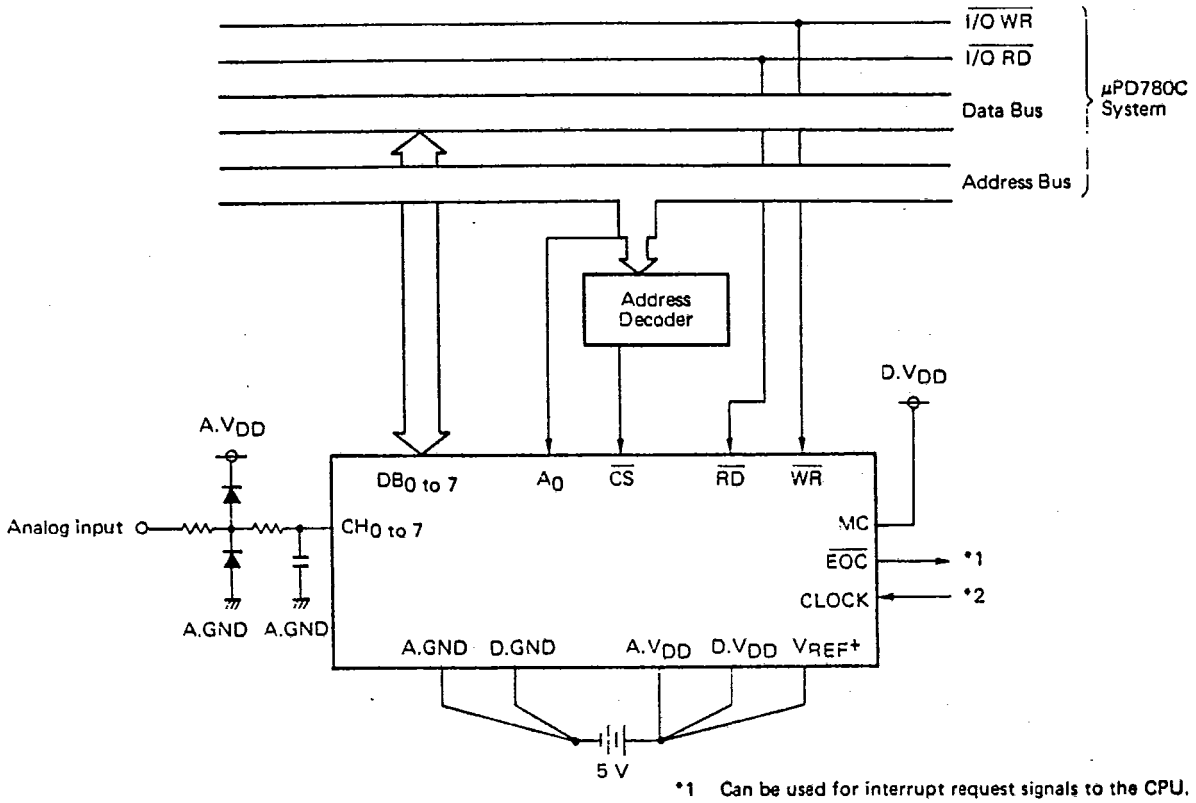
	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
High-byte	MSB	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Low-byte	9TH	LSB	L	L	L	L	L	L

EXAMPLE OF THE PARALLEL MODE INTERFACE

Fig. 1 shows an example of connecting the μPD7004C to the μPD780C system. As shown in the example, the parallel mode can handle connections using such basic interface circuits as microcomputer peripheral LSIs.

In this example, the μPD780C is employed as a CPU. It is also possible to have other 8-bit CPUs connected in the same logic design, with some timing management by the wait cycle.

Fig. 1 μPD780C/μPD7004C connection



*1 Can be used for interrupt request signals to the CPU.

*2 Can apply a clock to the CPU. (up to 8 MHz)

2. Serial Mode

The serial mode includes serial mode 1 and serial mode 2. Described below are the functions of terminals operating in each mode.

SERIAL I/O OPERATION (Serial Mode 1, 2, MC = L)

Symbol	Pin No.	Serial Mode 1 (External Serial Clock, A_0 = L)		Serial Mode 2 (Signal Processor Mode, A_0 = H)	
		I/O	Function	I/O	Function
SO	7	Output	Serial output (three state). Data are output at the falling edge of $\overline{SCKI}$ or $\overline{SCKO}$.		
SI	8	Input	Serial Input. Data read at the rising edge of $\overline{SCKI}$ or $\overline{SCKO}$.	Input	Connect to V_{DD}
SHIFT	9	Input	Shift Select (H: LSB first, L: MSB first)		
$\overline{SCKO}$	10	–	Connect to GND	Output	Serial Clock Output (= Internal Clock)
$\overline{SOEN}$	11	–	Connect to GND	Output	Serial Output Enable (= Active Low)
CODE	12	Input	Code Select (H = 2's complement, L = Binary)		
DEV 1	13	Input	Division Ratio Setting	DEV_1	L L H H
DEV 0	14	Input		DEV_0	L H L H
				Division Ratio	1/1 1/2 1/4 1/8
$\overline{STB}$	19	Input	Address strobe Input MPX addresses are latched at the rising edge of $\overline{STB}$ Input.	Input	Connect to GND
$\overline{SCKI}$	21	Input	$\overline{SCKI}$ controls the shift operation of I/O interface shift register. Data are output at the falling edge, and input at the rising edge.	–	Connect to V_{DD}
$\overline{CS}$	22	Input	Chip select signal input. Low level of $\overline{CS}$ resets the internal sequence, and I/O interface is enabled.	Input	Internal sequence reset signal input. Sequence controller are reset at the low level of $\overline{CS}$, and A/D conversion starts at the rising edge of $\overline{CS}$.

Notes: 1. In serial mode 1, the following signals are strobed by the $\overline{CS}$ signal. Therefore, the input signals are ignored and the output terminals become high impedance when $\overline{CS}$ = HIGH.
Input Terminal: SI, $\overline{STB}$, $\overline{SCKI}$
Output Terminal: SO

2. In serial mode 2, the internal sequence reset signal ($\overline{CS}$) specifies CH_7.

2.1 Serial Mode 1

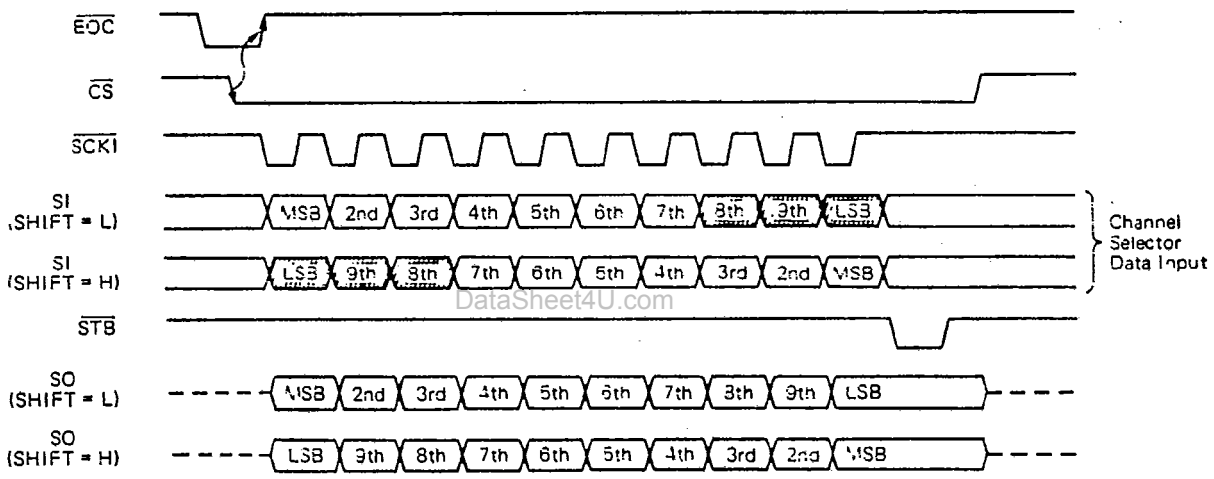
Serial mode 1 supports the serial data I/O when the $\overline{CS}$ signal is at the low level, outputs the serial data from the falling edge of the serial clock signal ($\overline{SCKI}$) entered from the external circuit, and fetches the serial input data at the rising edge of the $\overline{SCKI}$ signal.

If the MSB-first data is specified (SHIFT = L), the last three bits of the 10-bit serial input data for the MPX address selection contain valid data. If the LSB-first data is specified (SHIFT = H), the first three bits of the 10-bit data for the MPX address selection contain valid data. This MPX address data latch in the μPD7004C is implemented when at the rising edge of the $\overline{STB}$ signal. The latch can also be achieved at the rising edge the $\overline{CS}$ signal, if the $\overline{STB}$ signal is fixed at the low level.

The A/D conversion starts from the rising edge of $\overline{CS}$ signal. The $\overline{EOC}$ signal changes to the low level at the end of the conversion to notify this to the external environment. The time required for the A/D conversion is the same as that required in the parallel mode. The $\overline{EOC}$ signal changes to the high level from the falling edge of $\overline{CS}$ signal.

The A/D conversion is repeatedly operated when the $\overline{CS}$ signal stays in the high-level and the $\overline{EOC}$ signal remains in the low-level.

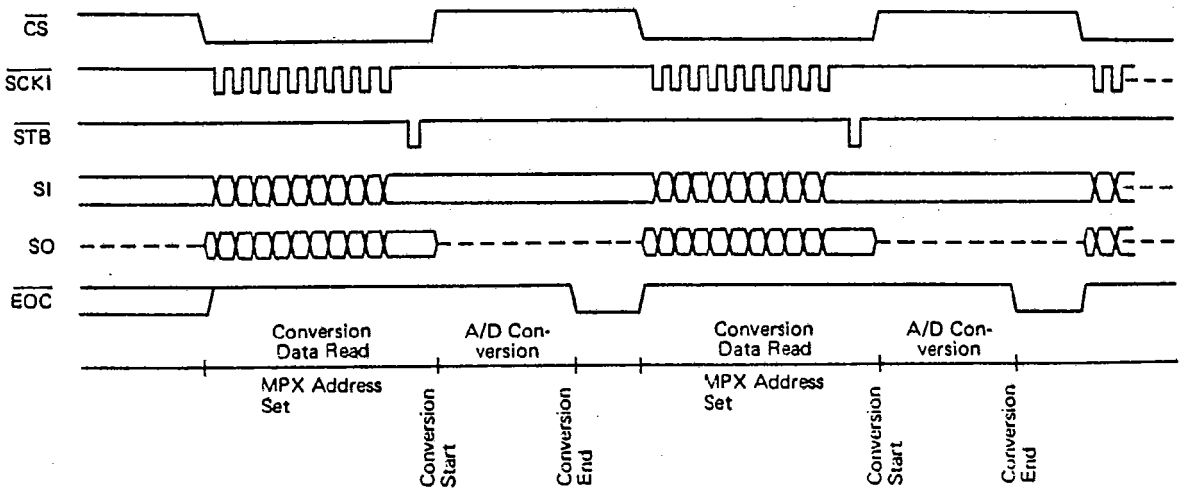
Serial Mode 1 Timing Chart



The 3 low-order bits of the serial input data serve as channel selection data.

8th	L	L	L	L	H	H	H	H
9th	L	L	H	H	L	L	H	H
LSB	L	H	L	H	L	H	L	H
Channel	CH_0	CH_1	CH_2	CH_3	CH_4	CH_5	CH_6	CH_7

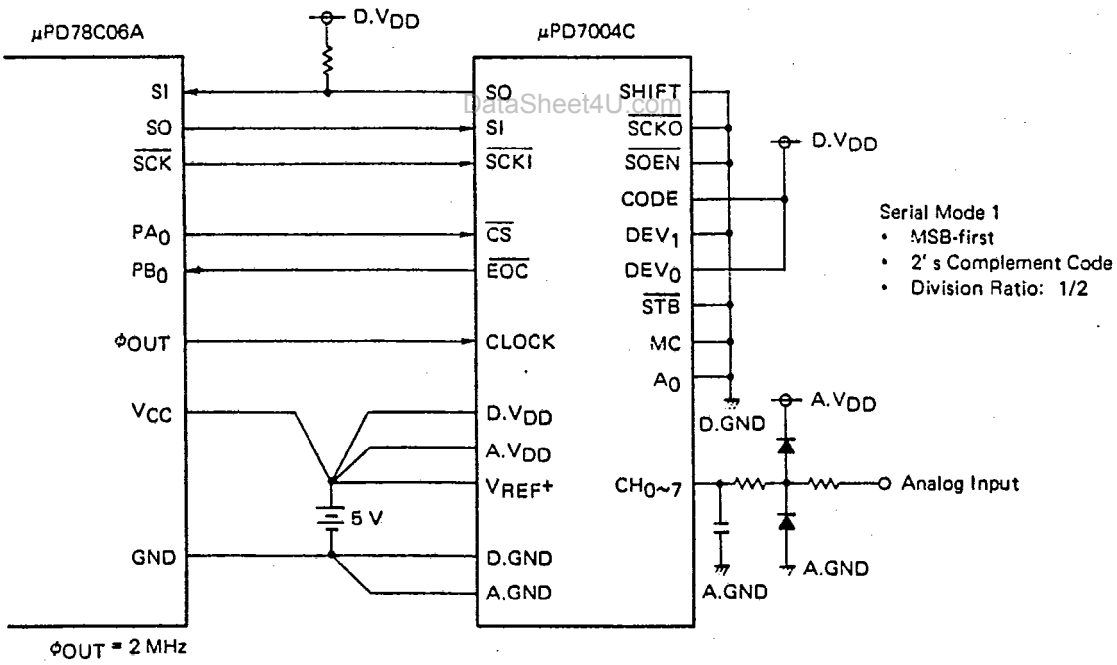
Serial Mode 1 Sequence Timing Chart



Example of the Interface with the μPD78C06A

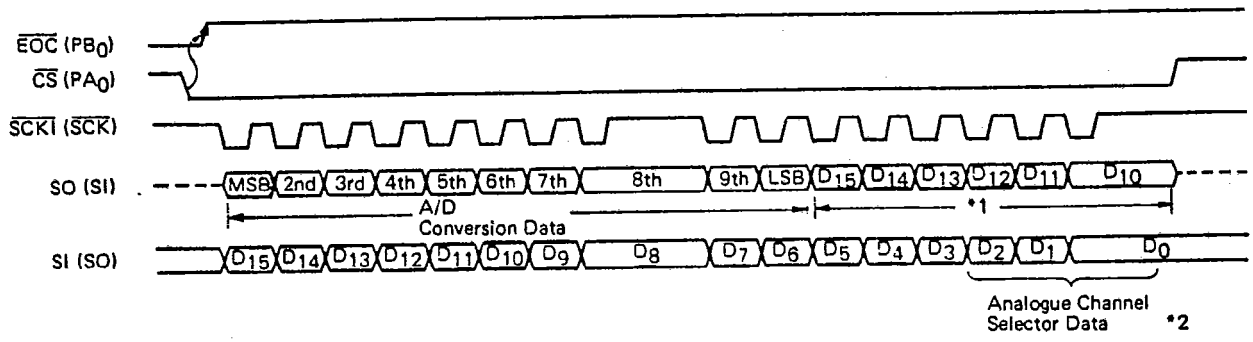
Fig. 2 shows an example of the interface with the μPD78C06A

Fig. 2 μPD7004C/μPD78C06A connection



μPD78C06A contains a serial interface circuit and handles 8-bit data transfer. Therefore, the μPD78C06A operates 8-bit data transfer twice to handle the μPD7004C's 10-bit serial data transfer. The timing of the data transfer is shown in Fig. 3.

Fig. 3 Timing in serial mode 1 (connection with μPD78C06A)



*1 The data entered through the SI terminal is output from SO.

*2 Channel selector data is latched at the rising edge of the CS signal when the STB signal is fixed at the low level.

Channel selector data

D_2	L	L	L	L	H	H	H	H
D_1	L	L	H	H	L	L	H	H
D_0	L	H	L	H	L	H	L	H
Channel	CH_0	CH_1	CH_2	CH_3	CH_4	CH_5	CH_6	CH_7

2.2 Serial Mode 2

Serial mode 2 allows direct connection to the serial interface of the signal processor μPD7720AC.

Shown on the right is an example of connecting principal terminals between the μPD7004C and μPD7720AC. Serial mode 2 differs from the other two modes. This mode cannot specify the MPX address to the μPD7004C since the address is fixed at CH_7.

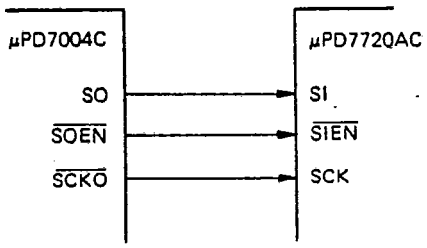
Although the data through the A/D conversion consists of 10 bits, it is followed by six bits of high data when it is output as serial data.

These six bits of high data always follow the converted data for MSB-first or LSB-first. (Refer to the Serial Mode 2 Timing Chart.)

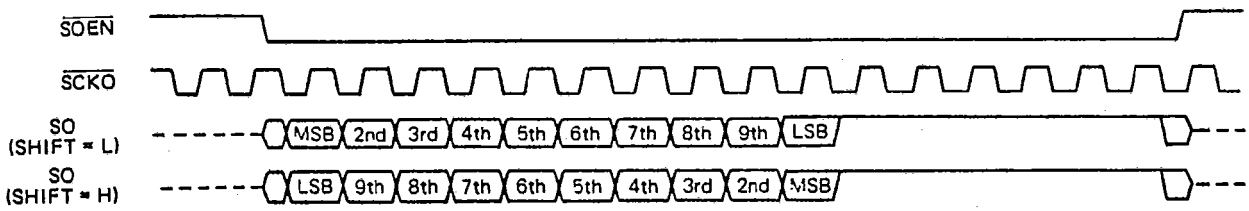
The A/D conversion sequence starts upon the initialization. The initialization is operated by holding the $\overline{CS}$ signal at the low level for more than eight clock cycles. The A/D conversion starts when the $\overline{CS}$ signal changes to the high-level. The A/D conversion requires 104 clock pulses (f_{CKI}).

The $\overline{EOC}$ signal, as in the other modes, changes to the low level to notify the end of the conversion to the external environment. The $\overline{EOC}$ signal remains at the low level until the initialization is implemented.

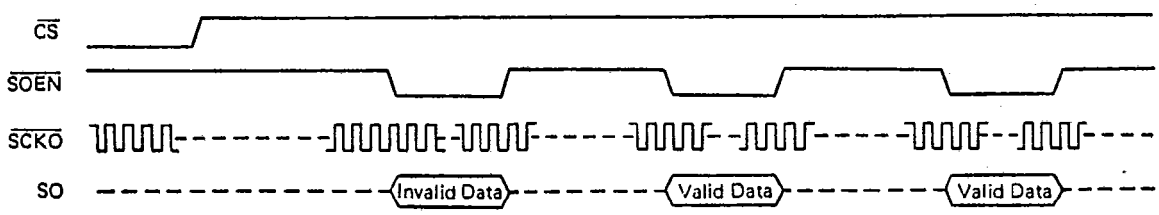
The data converted and output immediately after the initialization is invalid. Valid data is available from the second output. This is because the MPX address is fixed at CH_7 for theconverted data output after the initialization. The A/D conversion and the converted data output are repeatedly operated while the $\overline{CS}$ signal is in the high level. (Refer to the Serial Mode 2 Sequence Timing Chart.)



Serial Mode 2 Timing Chart



Serial Mode 2 Sequence Timing Chart

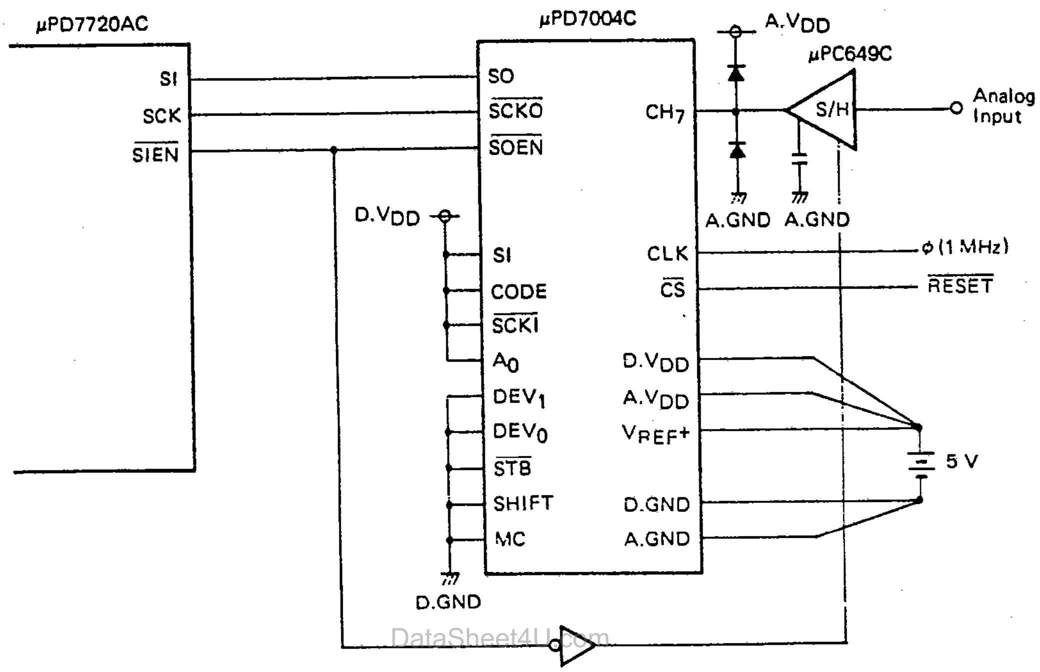


INTERFACE IN SERIAL MODE 2

In serial mode 2 direct connection can be made to the digital signal processor (μPD7720AC) and A/D conversion, unlike the parallel mode and serial mode 1, is operated in a periodic cycle.

Signals in the interface, unlike with serial mode 1, are controlled by the μPD7004C. Fig. 4 shows an example of connecting the μPD7004C to the μPD7720AC.

Fig. 4 μPD7004C/μPD7720AC connection



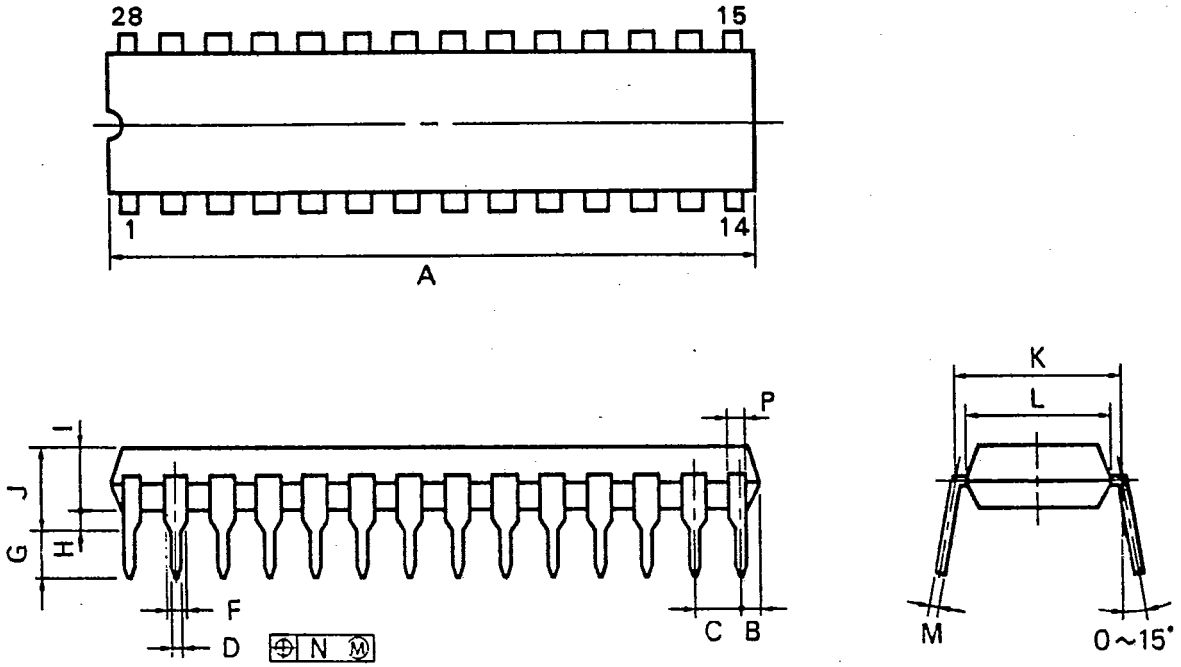
As shown in Fig. 4, it is possible to interface with only three kinds of signal connection lines in serial mode 2. A/D conversion is operated every 104 μs cycle (where clock = 1 MHz). The converted data is output synchronously with the $\overline{SOEN}$ signal.

The μPD7720AC's serial interface operates 16-bit data transfer, while the converted data consists of 10 bits. Therefore, 6 bits of high data automatically follow the 10 bits of converted data.

In the example above, the external sample & hold circuit (μPC649C) is used and the whole operation is operated as a kind of pipe-line processing. The $\overline{SOEN}$ signal supplies valid data three cycles after the reset cancellation, and then supplies converted data every 104 μs after this.

PACKAGE DIMENSIONS

28PIN PLASTIC DIP (400 mil)



P28C-100-400

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.