

**MOTOROLA
SEMICONDUCTOR**
 TECHNICAL DATA

**MC1458,C
MC1558**

2

(Dual MC1741)

**Internally Compensated, High
Performance Dual Operational
Amplifiers**

The MC1458/1558 was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

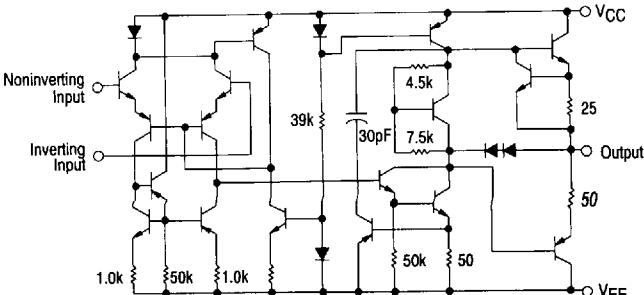
- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Input Differential Voltage	V_{ID}		± 30	V
Input Common Mode Voltage (Note 1)	V_{ICM}		± 15	V
Output Short Circuit Duration (Note 2)	t_{SC}		Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	$^\circ\text{C}$
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}		-65 to +150 -55 to +125	$^\circ\text{C}$
Junction Temperature Ceramic Package Plastic Package	T_J		175 150	$^\circ\text{C}$

NOTES: 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

2. Supply voltage equal to or less than 15 V.

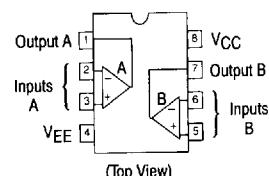
EQUIVALENT CIRCUIT SCHEMATIC

**MC1458,C
MC1558**

(DUAL MC1741)
**DUAL
OPERATIONAL AMPLIFIERS**
 SILICON MONOLITHIC
 INTEGRATED CIRCUIT

P1 SUFFIX
 PLASTIC PACKAGE
 CASE 626

U SUFFIX
 CERAMIC PACKAGE
 CASE 693

D SUFFIX
 PLASTIC PACKAGE
 CASE 751
 (SO-8)

PIN CONNECTIONS

ORDERING INFORMATION

Device	Temperature Range	Package
MC1458CD,D	$0^\circ \text{ to } +70^\circ\text{C}$	SO-8
MC1458CP1,P1		Plastic DIP
MC1458CU,U		Ceramic DIP
MC1558U	$-55^\circ \text{ to } +125^\circ\text{C}$	Ceramic DIP

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ELECTRICAL CHARACTERISTICS — Note 1. ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	—	1.0	5.0	—	2.0	6.0	—	2.0	1.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	—	20	300	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	—	80	700	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	—	2.0	—	MΩ
Input Capacitance	C_i	—	1.4	—	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	±15	—	—	±15	—	—	±15	—	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±12	±13	—	±11	±13	—	V
Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2.0$ k) ($V_O = \pm 10$ V, $R_L = 10$ k)	A_{VOL}	50 —	200 —	—	20 —	200 —	—	— 20	— 200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	—	70	90	—	60	90	—	dB
Supply Voltage Rejection ($R_S \leq 10$ k)	PSR	—	30	150	—	30	150	—	30	—	µV/V
Output Voltage Swing ($R_S \leq 10$ k) ($R_S \leq 2.0$ k)	V_O	±12 ±10	±14 ±13	—	±12 ±10	±14 ±13	—	±11 ±9.0	±14 ±13	—	V
Output Short Circuit Current	I_{SC}	—	20	—	—	20	—	—	20	—	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.0	—	2.3	5.6	—	2.3	8.0	mA
Power Consumption	PC	—	70	150	—	70	170	—	70	240	mW
Transient Response (Unity Gain) ($V_I = 20$ mV, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Rise Time ($V_I = 20$ mV, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Overshoot ($V_I = 10$ V, $R_L \geq 2.0$ kΩ, $C_L \leq 100$ pF) Slew Rate	t_{TLH} os SR	—	0.3 15 0.5	—	—	0.3 15 0.5	—	—	0.3 15 0.5	—	µs % V/µs

ELECTRICAL CHARACTERISTICS — Note 1. ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = T_{high}$ to T_{low} , unless otherwise noted.)*

Characteristics	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	—	1.0	6.0	—	—	7.5	—	—	12	mV
Input Offset Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ$ to $+70^\circ\text{C}$)	I_{IO}	—	7.0 85 —	200 500 —	—	—	—	—	—	—	nA
Input Bias Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ$ to $+70^\circ\text{C}$)	I_{IB}	—	30 300 —	500 1500 —	—	—	—	—	—	—	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	—	—	—	—	—	—	V
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	—	—	—	—	—	—	—	dB
Supply Voltage Rejection ($R_S \leq 10$ k)	PSR	—	30	150	—	—	—	—	—	—	µV/V
Output Voltage Swing ($R_S \leq 10$ k) ($R_S \leq 2$ k)	V_O	±12 ±10	±14 ±13	—	±12 ±10	±14 ±13	—	±9.0	±13	—	V
Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 2$ k) ($V_O = \pm 10$ V, $R_L = 10$ k)	A_{VOL}	25 —	—	—	15 —	—	—	—	—	—	V/mV
Supply Currents (Both Amplifiers) ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	I_D	—	—	4.5 6.0	—	—	—	—	—	—	mA
Power Consumption ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	PC	—	—	135 180	—	—	—	—	—	—	mW

 $T_{low} = -55^\circ\text{C}$ for MC1558 $T_{high} = +125^\circ\text{C}$ for MC1558

0°C for MC1458

+70°C for MC1458

NOTE: 1. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

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Figure 1. Burst Noise versus Source Resistance

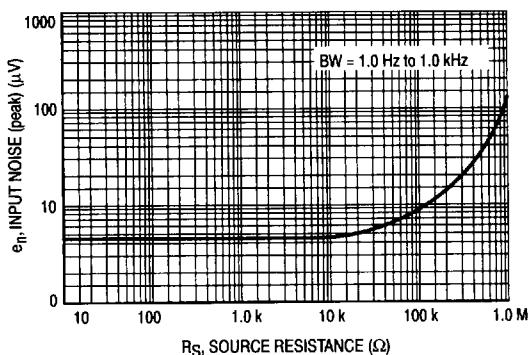


Figure 2. RMS Noise versus Source Resistance

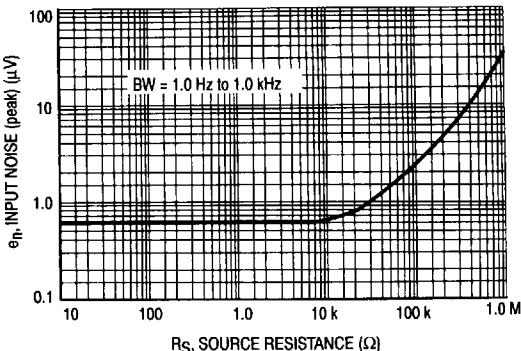


Figure 3. Output Noise versus Source Resistance

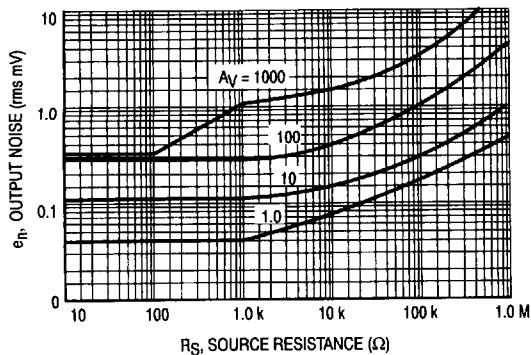


Figure 4. Spectral Noise Density

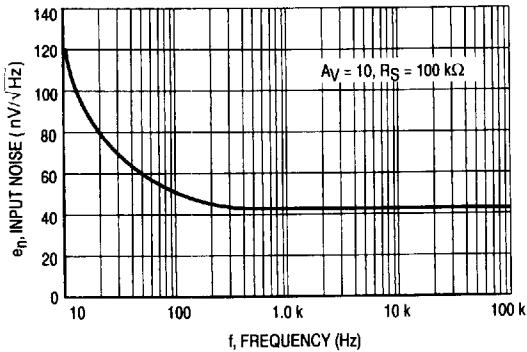
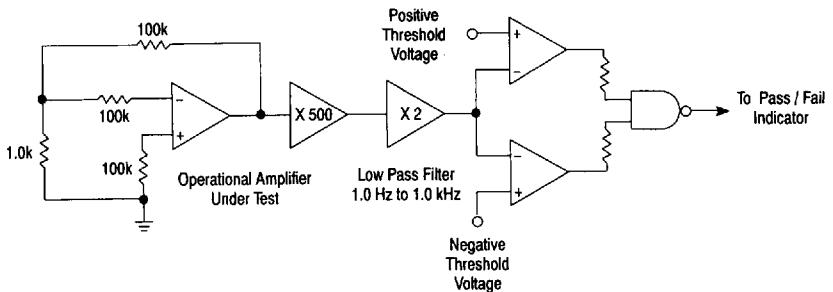


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μ V peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier.

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**Figure 6. Power Bandwidth
(Large Signal Swing versus Frequency)**

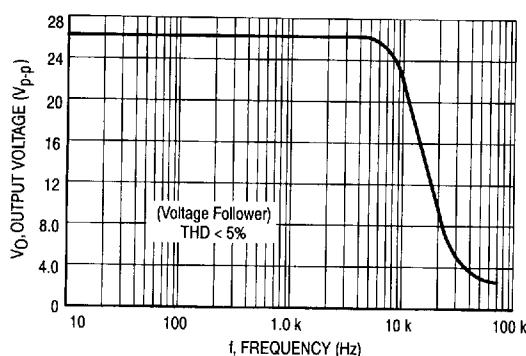
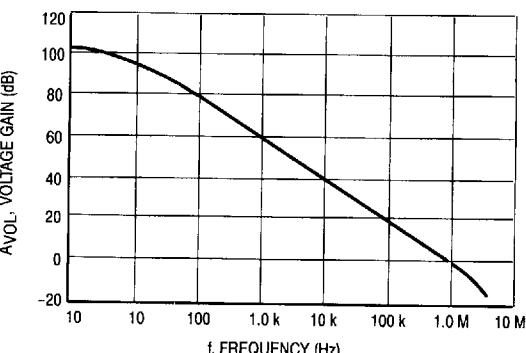
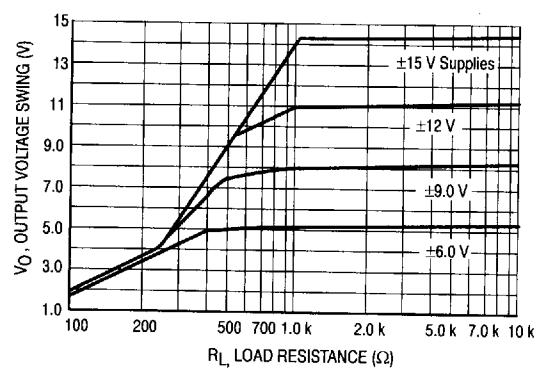


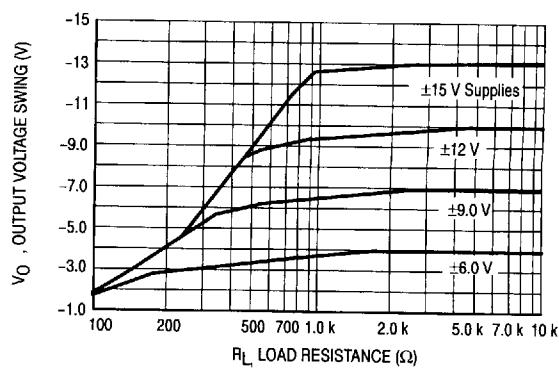
Figure 7. Open-Loop Frequency Response



**Figure 8. Positive Output Voltage Swing
versus Load Resistance**



**Figure 9. Negative Output Voltage Swing
versus Load Resistance**



**Figure 10. Output Voltage Swing versus
Load Resistance (Single Supply Operation)**

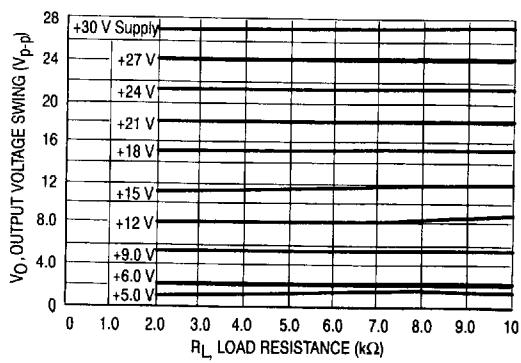
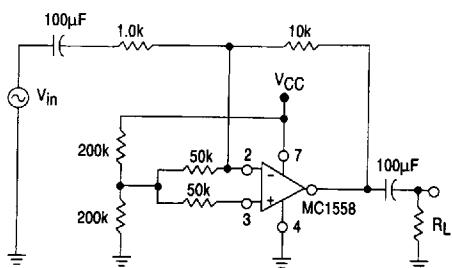


Figure 11. Single Supply Inverting Amplifier



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Figure 12. Noninverting Pulse Response

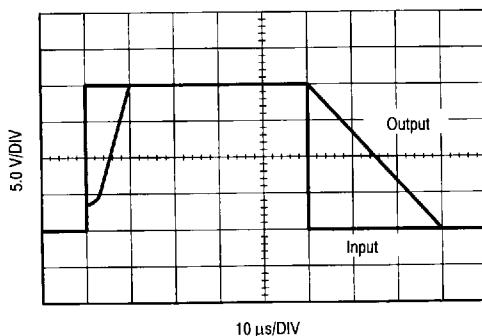


Figure 13. Transient Response Test Circuit

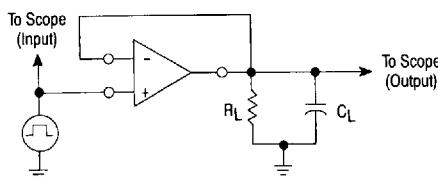


Figure 14. Open-Loop Voltage Gain versus Supply Voltage

